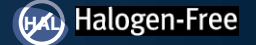


EPC2010C – Enhancement Mode Power Transistor

 V_{DS} , 200 V $R_{DS(on)}$, 25 m Ω I_D , 22 A

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings

PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	200	V
I_D	Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 5.3$)	22	A
	Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	90	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics

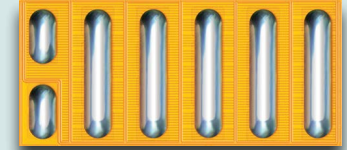
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.1	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	2.7	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	56	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$, $I_D = 200 \mu\text{A}$	200			V
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0 \text{ V}$, $V_{DS} = 160 \text{ V}$		50	150	μA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$		1	3	mA
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$		50	150	μA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 3 \text{ mA}$	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$, $I_D = 12 \text{ A}$		18	25	m Ω
V_{SD}	Source-Drain Forward Voltage	$I_S = 0.5 \text{ A}$, $V_{GS} = 0 \text{ V}$		1.7		V

All measurements were done with substrate connected to source.



EPC2010C eGaN® FETs are supplied only in passivated die form with solder bars

Applications

- High Speed DC-DC conversion
- Class D Audio
- Lidar

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra Low Q_G
- Ultra Small Footprint



Dynamic Characteristics ($T_j = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$		380	540	pF
C_{OSS}	Output Capacitance			240	320	
C_{RSS}	Reverse Transfer Capacitance			1.8	2.7	
R_G	Gate Resistance		0.4			Ω
Q_G	Total Gate Charge	$V_{DS} = 100\text{ V}, I_D = 12\text{ A}, V_{GS} = 5\text{ V}$		3.7	5.3	nC
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 100\text{ V}, I_D = 12\text{ A}$		1.3		
Q_{GD}	Gate-to-Drain Charge			0.7	1.3	
$Q_{G(TH)}$	Gate Charge at Threshold			0.9		
Q_{OSS}	Output Charge	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$		40	52	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate connected to source.

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Figure 1: Typical Output Characteristics at 25°C

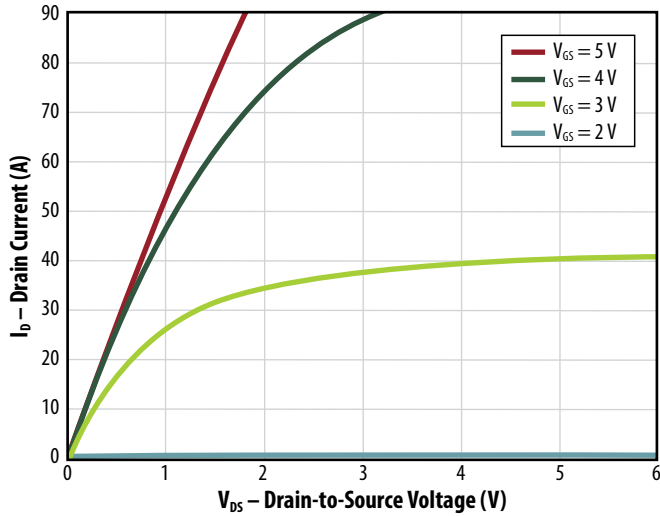


Figure 2: Transfer Characteristics

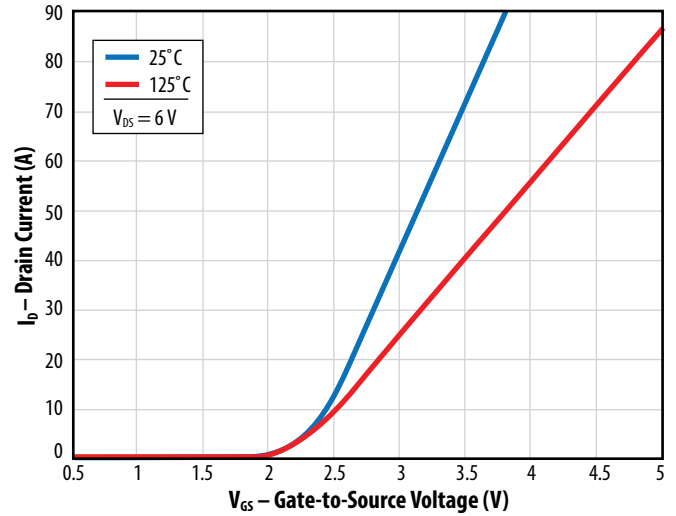


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Current

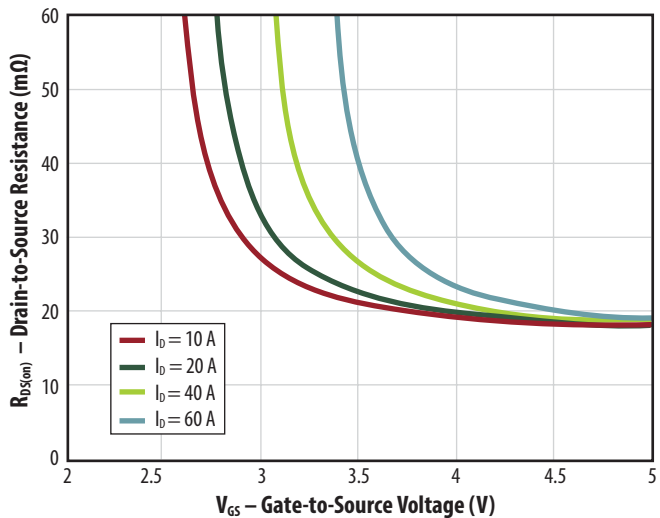


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

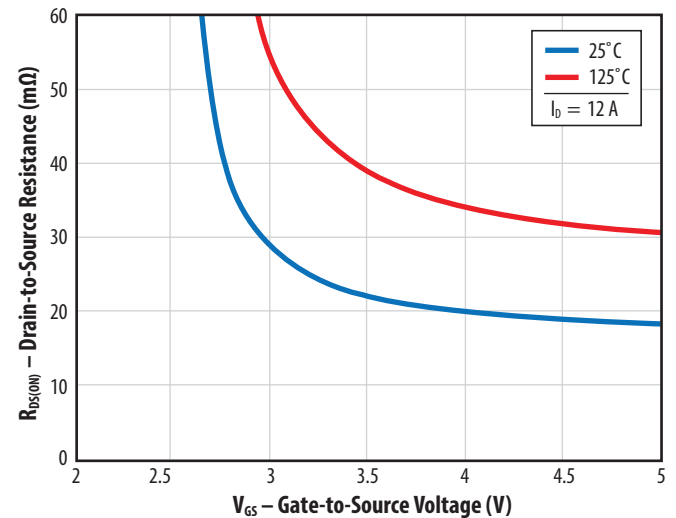


Figure 5a: Capacitance Linear Scale

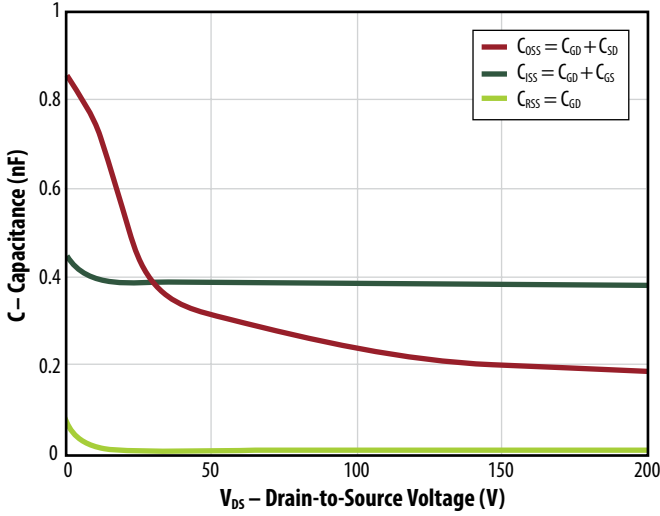


Figure 5b: Capacitance Log Scale

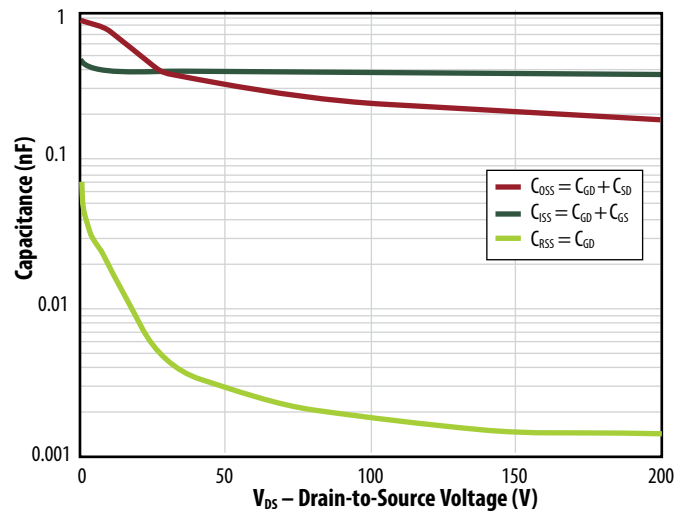


Figure 6: Gate Charge

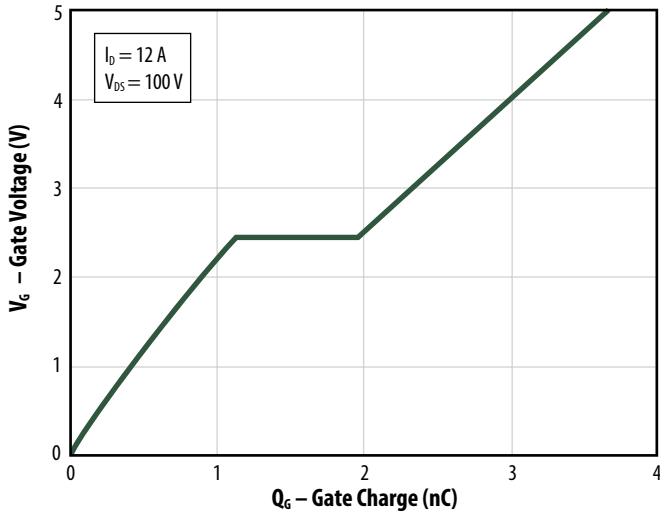


Figure 7: Reverse Drain-Source Characteristics

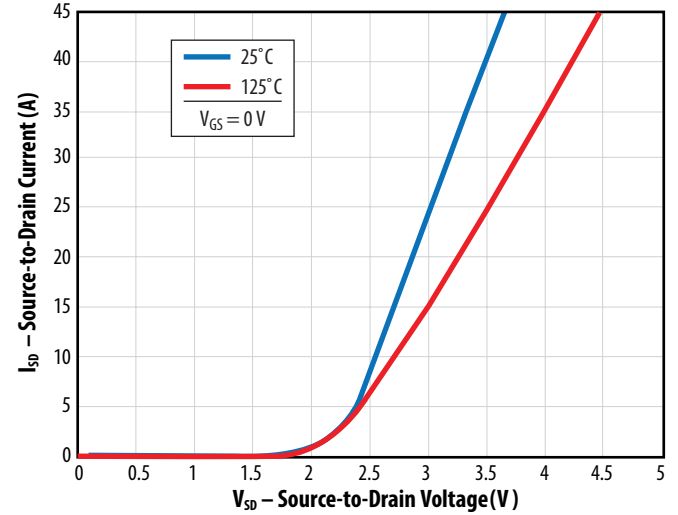


Figure 8: Normalized On Resistance vs. Temperature

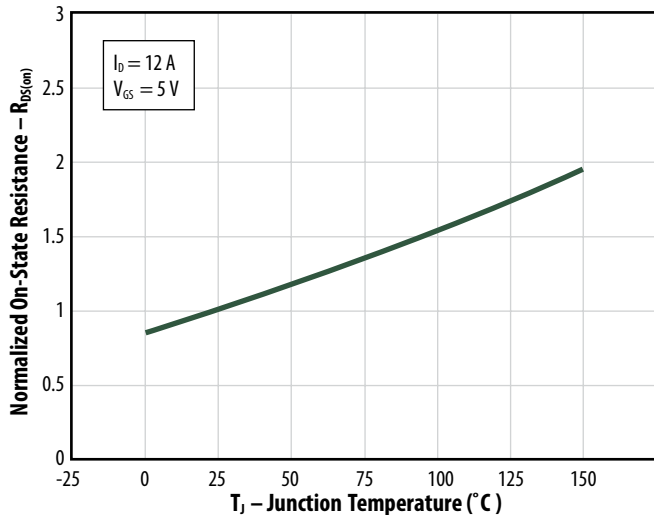


Figure 9: Normalized Threshold Voltage vs. Temperature

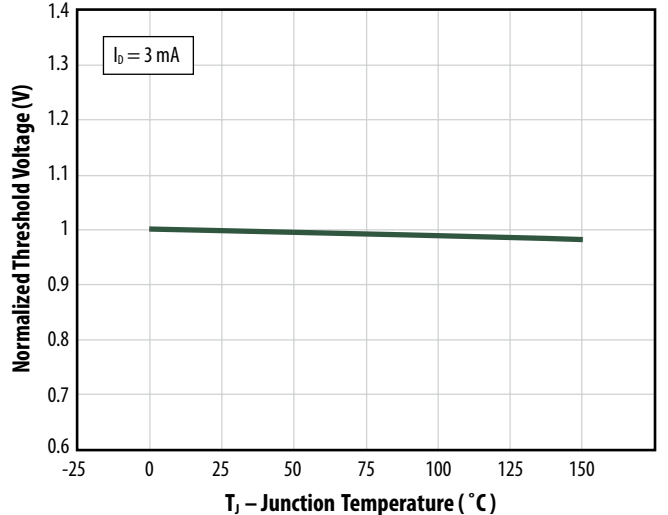


Figure 10: Gate Current

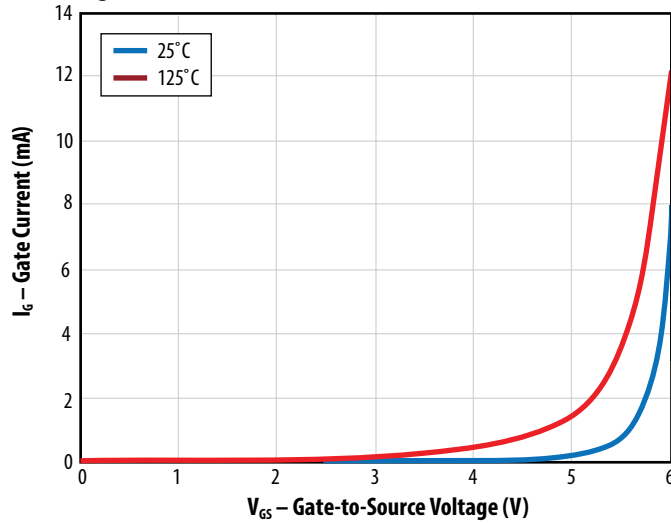


Figure 11: Transient Thermal Response Curves

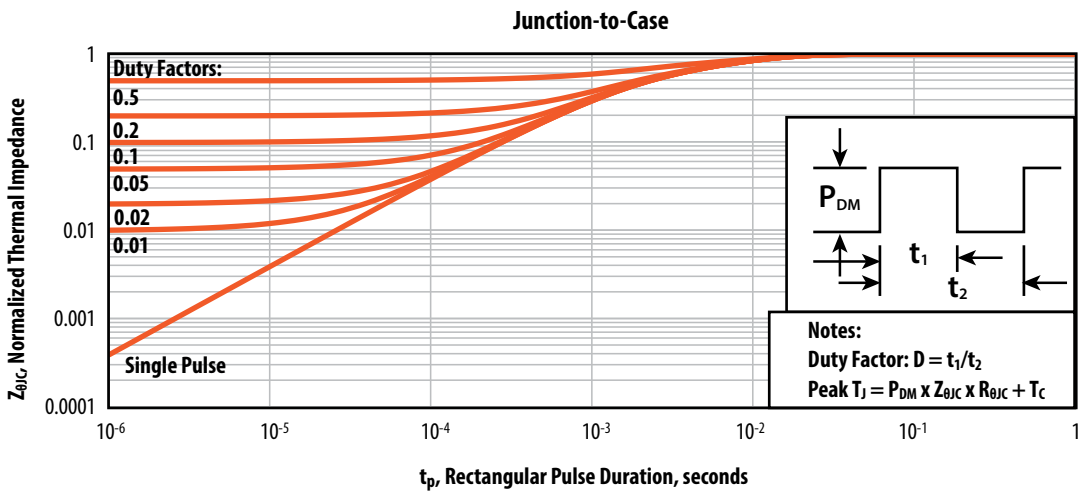
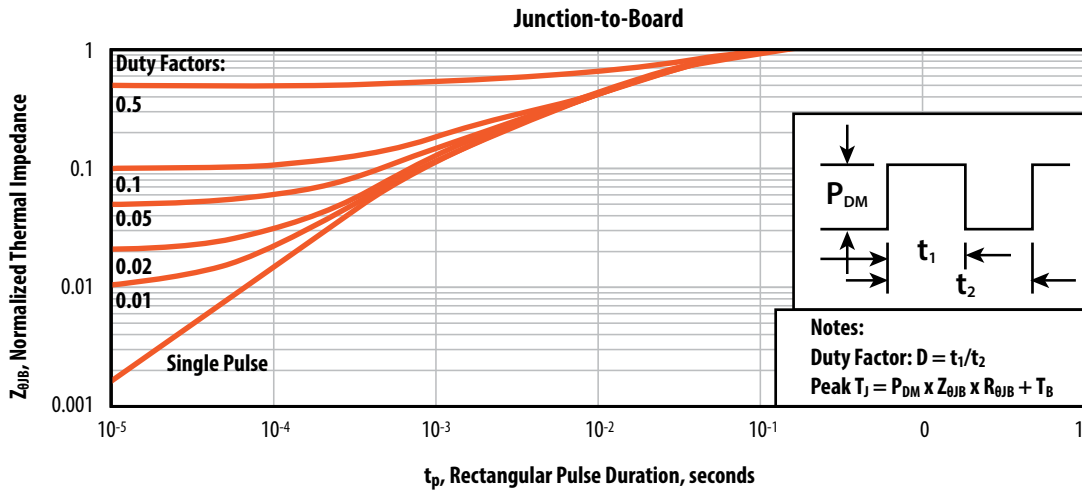
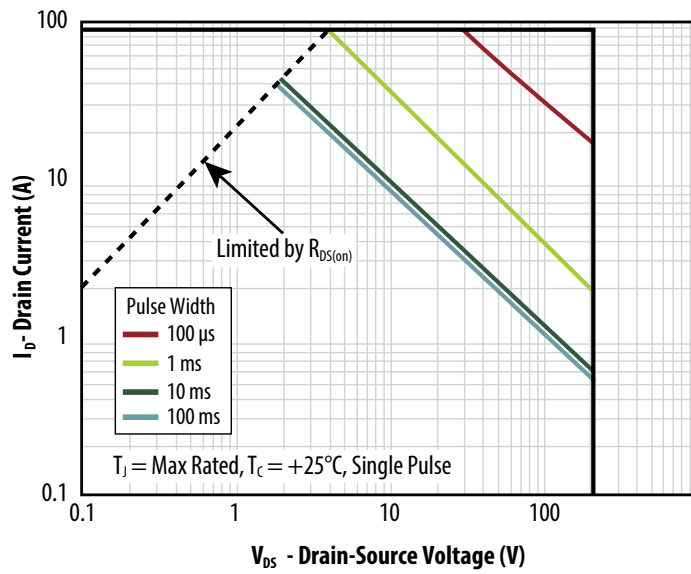
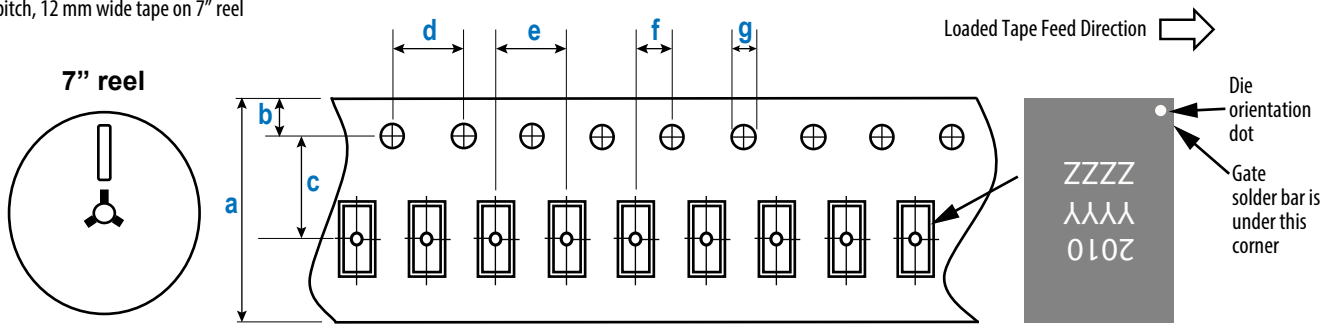


Figure 12: Safe Operating Area



TAPE AND REEL CONFIGURATION

4 mm pitch, 12 mm wide tape on 7" reel



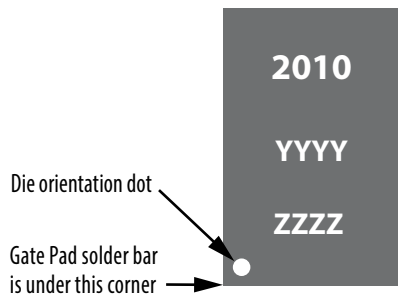
Die is placed into pocket solder bar side down (face side down)

EPC2010 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/ JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

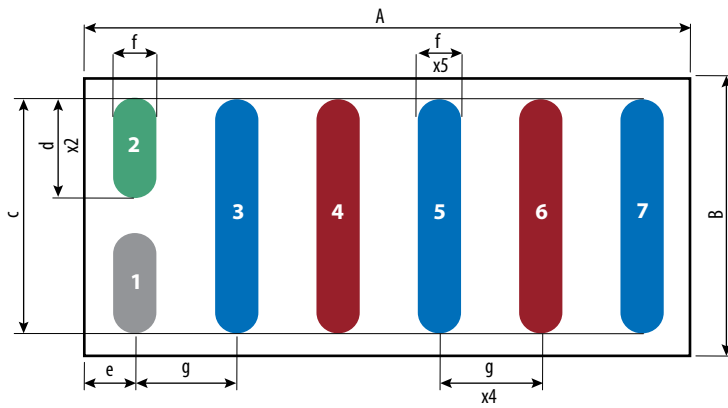
DIE MARKINGS



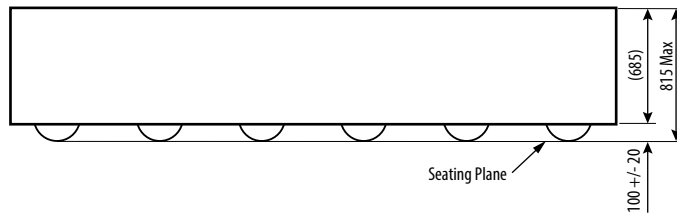
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2010C	2010	YYYY	ZZZZ

DIE OUTLINE

Solder Bar View



Side View



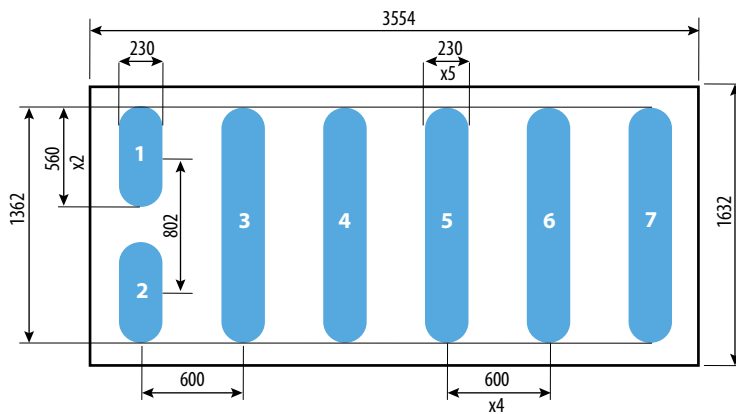
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	3524	3554	3584
B	1602	1632	1662
c	1379	1382	1385
d	577	580	583
e	262	277	292
f	245	250	255
g	600	600	600

Pad no. 1 is Gate;
 Pads no. 3, 5, 7 are Drain;
 Pads no. 4, 6 are Source;
 Pad no. 2 is Substrate.*

*Substrate pin should be connected to Source

RECOMMENDED LAND PATTERN

(units in μm)



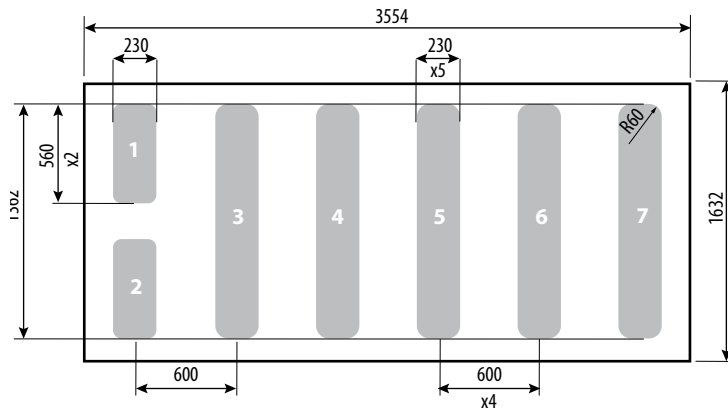
The land pattern is solder mask defined.

Pad no. 1 is Gate;
 Pads no. 3, 5, 7 are Drain;
 Pads no. 4, 6 are Source;
 Pad no. 2 is Substrate.*

*Substrate pin should be connected to Source

RECOMMENDED STENCIL DRAWING

(units in μm)



Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, opening per drawing. The corner has a radius of R60.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Additional assembly resources available at <https://www.epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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