TPS65086x Design Guide

This document is meant to be used as a guide for designers to ensure the proper design of the TPS65086x PMIC. The TPS65086x is an analog chip containing several power resources which each have different constraints when creating the schematic and layout. The purpose of this guide is to provide a better understanding for these constraints and, through example, give an explanation of how proper layout can be done. The guide is intended to be used with the *TPS65086x Schematic and Layout Checklist* (SLVA734).

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1 Device Description – TPS65086x

The TPS65086x is a single-chip solution power-management IC designed to support a variety of FPGAs and SOCs. The device features 3 controllers and 3 converters for high power, high efficiency rails. A sink/source LDO (VTT), 3 LDO's and 3 load switches are controlled by power-up sequence logic to provide the proper power rails, sequencing, and protection. An I^2C interface allows simple control either by an embedded controller (EC) or by a SoC. The PMIC comes in an 8 × 8 single-row QFN package with thermal pad for good thermal dissipation and ease-of-board routing.

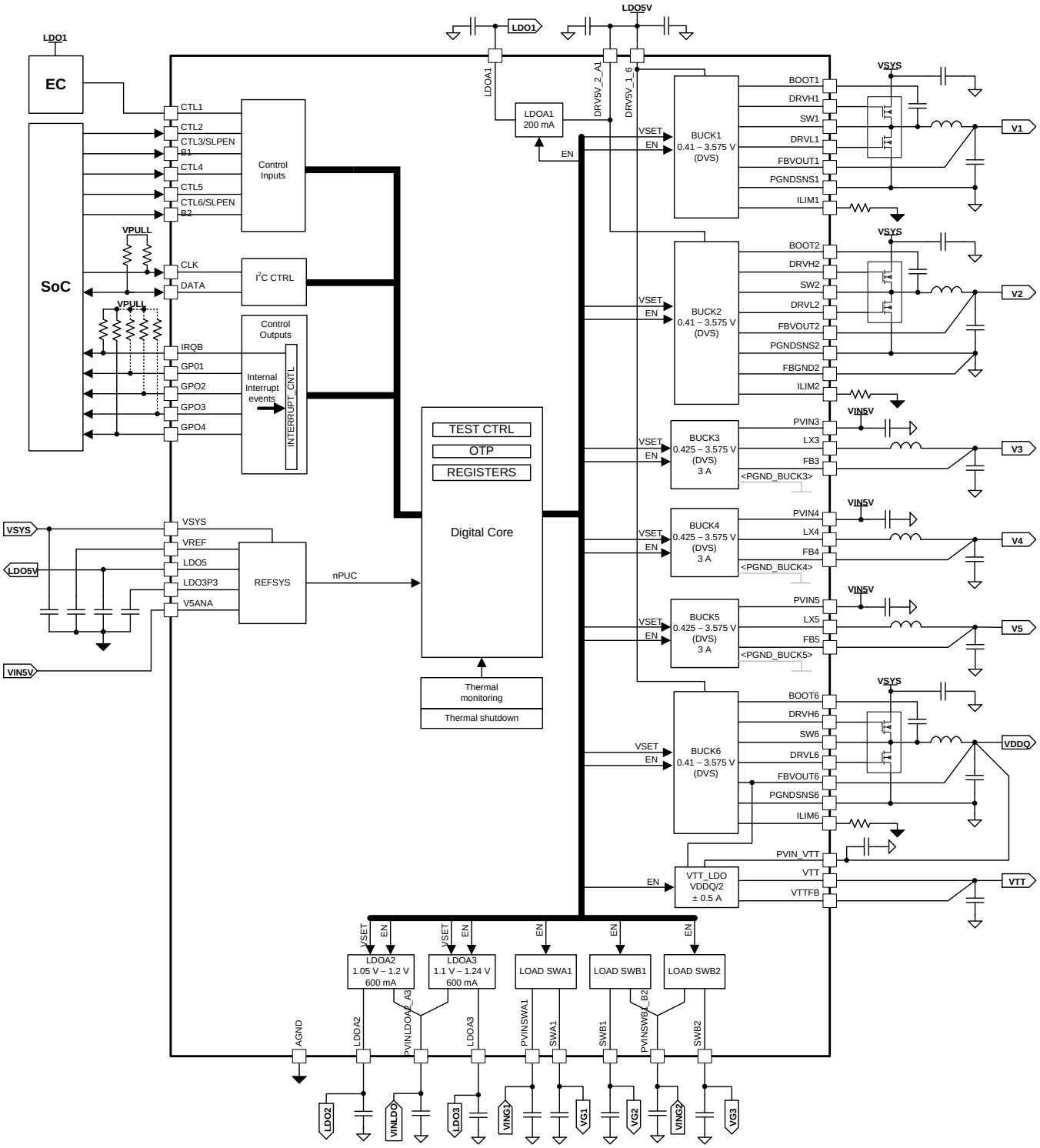


Figure 1. PMIC Functional Block Diagram

2 Schematic Guidelines

2.1 Controller Design Procedure

Designing the controller can be broken down into the following steps:

1. Design the output filter
2. Select the FETs
3. Select the bootstrap capacitor
4. Select the input capacitors
5. Set the current limits

Controllers BUCK1, BUCK2, and BUCK6 require a 5-V supply and capacitors at their corresponding DRV_x_x pins. For most applications, the DRV_x_x input should come from the LDO5P0 pin to ensure uninterrupted supply voltage; a 2.2 µF, X5R, 20%, 10-V, or similar capacitor must be used for decoupling.

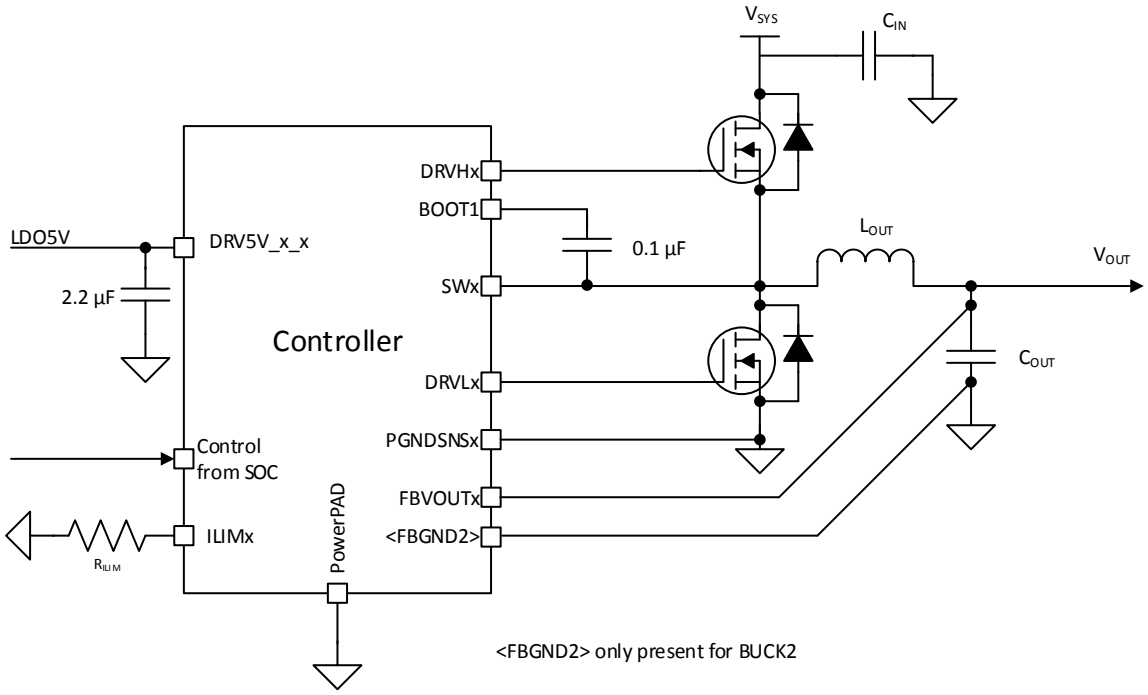


Figure 2. Controller Diagram

2.1.1 Selecting the Inductor

Placement of an inductor is required between the external FETs and the output capacitors. Together, the inductor and output capacitors make the double-pole that contributes to stability. In addition, the inductor is directly responsible for the output ripple, efficiency, and transient performance. As the inductance used increases the ripple current decreases, which typically results in an increased efficiency. However, with an increase in inductance used, the transient performance decreases. Finally, the inductor selected must be rated for appropriate saturation current, core losses, and DC resistance (DCR).

Equation 1 shows the calculation for the recommended inductance for the controller.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times Iout_{MAX} \times K_{IND}} \quad (1)$$

where

- V_{OUT} is the typical output voltage
- V_{IN} is the typical input voltage
- f_{SW} is the typical switching frequency
- $Iout_{MAX}$ is the maximum load current
- K_{IND} is the ratio of $I_{Lripple}$ to the $I_{out(max)}$. For this application, TI recommends that K_{IND} is set to a value from 0.2 to 0.4.

With the chosen inductance value, the peak current for the inductor in steady state operation, $I_{L(max)}$, can be calculated using Equation 2. The rated saturation current of the inductor must be higher than the $I_{L(max)}$ current.

$$I_{LMAX} = Iout_{MAX} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{SW} \times L} \quad (2)$$

2.1.2 Selecting the Output Capacitors

TI recommends using ceramic capacitors with low ESR values to provide the lowest output voltage ripple. The output capacitor requires an X7R or an X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. Due to the DCAP2 architecture, all output capacitors can be ceramic.

At light load currents, the controller operates in PFM mode, and the output voltage ripple is dependent on the output-capacitor value and the PFM peak inductor current. Higher output-capacitor values minimize the voltage ripple in PFM mode. To achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC bias voltage.

TI recommends the use of small ceramic capacitors placed between the inductor and load with many vias to the PGND plane for the output capacitors of the BUCK controllers. This solution typically provides the smallest and lowest cost solution available for DCAP2 controllers.

The selection of the output capacitor is typically driven by the output transient response. Equation 3 provides a rough estimate of the minimum required capacitance to ensure proper transient response. Because the transient response is significantly affected by the board layout, some experimentation is expected in order to confirm that values derived in this section are applicable to any particular use case. Equation 3 is not meant to be an absolute requirement, but rather a rough starting point.

$$C_{OUT} > \frac{I_{TRAN(max)}^{2} \times L}{V_{OUT} \times V_{OVER}} \quad (3)$$

where

- $I_{TRAN(max)}$ is the maximum load current step
- L is the chosen inductance
- V_{OUT} is the minimum programmed output voltage
- V_{OVER} is the maximum allowable overshoot from programmed voltage

In cases where the transient current change is very low, the DC stability may become important. Equation 4 approximates the amount of capacitance necessary to maintain DC stability. Again, this is provided as a starting point; actual values will vary on a board-to-board case.

$$C_{OUT} > \frac{V_{OUT} \times 50\ \mu s}{V_{IN} \times f_{SW} \times L} \quad (4)$$

where

- V_{OUT} is the maximum programmed output voltage
- 50 µs is based on internal ramp setup
- V_{IN} is the minimum input voltage
- f_{SW} is the typical switching frequency
- L is the chosen inductance

It is necessary to choose the maximum value between Equation 3 and Equation 4.

2.1.3 Selecting the FETs

This controller is designed to drive two NMOS FETs. Typically, lower R_{DSON} values are better for improving the overall efficiency of the controller. However, as the R_{DSON} for the low-side FET decreases, the minimum current limit increases; therefore, ensure selection of the appropriate values for the FETs, inductor, output capacitors, and current limit resistor. The Texas Instruments' CSD87381P and CSD87588N devices are recommended for the controllers, depending on the required maximum current. Switching and DC losses can vary across FETs, and as such each FET should have a power dissipation specification that meets or exceeds the total losses from the expected load conditions.

2.1.4 Bootstrap Capacitor

To ensure the internal high-side gate drivers are supplied with a stable low-noise supply voltage, a capacitor must be connected between the SWx pins and the respective BOOTx pins. TI recommends placing ceramic capacitors with the value of 0.1 µF for the controllers.

TI recommends reserving a small resistor in series with the bootstrap capacitor during prototype development in case the turnon and turnoff of the FETs must be slowed to reduce voltage ringing on the switch node, which is a common practice for controller design.

2.1.5 Setting the Current Limit

The buck controllers (BUCK1, BUCK2, and BUCK6) have inductor-valley current-limit architecture and the current limit is programmable by an external resistor at the ILIMx pin. Equation 5 shows the calculation for a desired resistor value, depending on specific application conditions. I_{LIMREF} is the current source out of the ILIMx pin that is typically 50 µA, and R_{DSON} is the maximum channel resistance of the low-side FET. The scaling factor is 1.3 to take into account all errors and temperature variations of R_{DSON}, I_{LIMREF}, and R_{ILIM}. Finally, 8 is another scaling factor associated with I_{LIMREF}.

$$R_{ILIM} = \frac{R_{DSON} \times 8 \times 1.3 \times (I_{LIM} - \frac{I_{ripple,min}}{2})}{I_{LIMREF}} \quad (5)$$

where

- I_{LIM} is target current limit. An appropriate margin should be allowed when one determines I_{LIM} from maximum output DC load current.
- $I_{ripple,min}$ is minimum peak-to-peak inductor ripple current for a given V_{OUT}

$$I_{ripple,min} = \frac{V_{out}(v_{in,min} - V_{out})}{L_{max} \times V_{in,min} \times f_{sw,max}} \quad (6)$$

where

- L_{max} is maximum inductance
- $f_{sw,max}$ is maximum switching frequency
- $V_{in,min}$ minimum input voltage to the external power stage

2.1.6 Selecting the Input Capacitors

Due to the nature of the switching controller with a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and also for minimizing the interference with other circuits caused by high input-voltage spikes. For the controller, a typical 2.2 µF capacitor can be used for the DRV5V_x_x pin to handle the transients on the driver. For the FET input, 10 µF of input capacitance (after derating) is recommended for most applications. To achieve the low ESR requirement, a ceramic capacitor is recommended. However, the voltage rating and DC-bias characteristic of ceramic capacitors must be considered. For better input-voltage filtering, the input capacitor can be increased without any limit.

NOTE: Use the correct value for the ceramic capacitor capacitance after derating to achieve the recommended input capacitance.

TI recommends placing a ceramic capacitor as close as possible to the FET across the respective VSYS and PGND pins of the FETs. Previously validated capacitor solutions for the controllers include two Murata GRM21BR61E226ME44: 22-µF, 0805, 25-V, ±20% ceramic capacitors in parallel. Similar capacitors may also be used.

2.2 Converter Design Procedure

Designing the converter has only two steps: design the output filter and select the input capacitors.

The converter must be supplied by a 5-V source. Figure 3 shows a diagram of the converter.

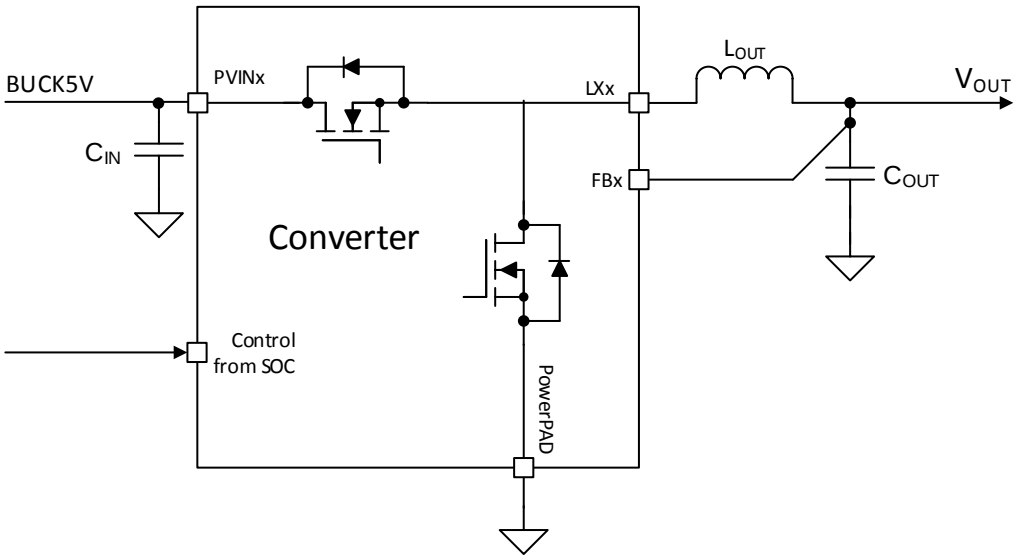


Figure 3. Converter Diagram

2.2.1 Selecting the Inductor

It is required that an inductor be placed between the external FETs and the output capacitors. Together, the inductor and output capacitors form a double pole in the control loop that contributes to stability. In addition, the inductor is directly responsible for the output ripple, efficiency, and transient performance. As the inductance used increases, the ripple current decreases; this typically results in an increase in efficiency. However, with an increase in inductance used, the transient performance decreases. Finally, the inductor selected must be rated for appropriate saturation current, core losses, and DC resistance (DCR).

NOTE: Internal parameters for the converters are optimized for a 0.47 µH inductor, however it is possible to use other inductor values as long as they are chosen carefully and thoroughly validated.

Equation 7 shows the calculation for the recommended inductance for the converter.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times Iout_{MAX} \times K_{IND}}$$

where

- V_{OUT} is the typical output voltage
- V_{IN} is the typical input voltage
- f_{SW} is the typical switching frequency
- $Iout_{MAX}$ is the maximum load current
- K_{IND} is the ratio of $I_{Lripple}$ to the $I_{out(max)}$. For this application, TI recommends that K_{IND} is set to a value from 0.2 to 0.4. (7)

With the chosen inductance value and the peak current for the inductor in steady state operation, $I_{L(MAX)}$ can be calculated using Equation 8. The rated saturation current of the inductor must be higher than the $I_{L(MAX)}$ current.

$$I_{LMAX} = Iout_{MAX} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{SW} \times L} \quad (8)$$

2.2.2 Selecting the Output Capacitors

Ceramic capacitors with low ESR values are recommended because they provide the lowest output voltage ripple. The output capacitor requires either an X7R or X5R rating. Y5V and Z5U capacitors, aside from the wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents, the converter operates in PFM mode and the output voltage ripple is dependent on the output-capacitor value and the PFM peak inductor current. Higher output-capacitor values minimize the voltage ripple in PFM mode. To achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC-bias voltage.

For the output capacitors of the BUCK converters, TI recommends placing small ceramic capacitors between the inductor and load with many vias to the PGND plane. This solution typically provides the smallest and lowest-cost solution available for DCAP2 controllers.

The output capacitance must equal or exceed the minimum capacitance listed in the datasheet for BUCK3, BUCK4, and BUCK5 (assuming quality layout techniques are followed).

2.2.3 Selecting the Input Capacitors

Due to the nature of the switching converter with a pulsating input current, a low ESR input capacitor is required for best input-voltage filtering and for minimizing the interference with other circuits caused by high input-voltage spikes. For the PVINx pin, 2.5 µF of input capacitance (after derating) is required for most applications. A ceramic capacitor is recommended to achieve the low ESR requirement. However, the voltage rating and DC-bias characteristic of ceramic capacitors must be considered. The input capacitor can be increased without any limit for better input-voltage filtering.

NOTE: Use the correct value for the ceramic capacitor capacitance after derating to achieve the recommended input capacitance.

A ceramic capacitor placed as close as possible to the FET, across the respective VSYS and PGND pins of the FETs is recommended. Previously validated capacitor solutions for the converters include one Samsung CL05A106MP5NUNC: 10-µF, 0402, 10-V, ±20% ceramic capacitor. Similar capacitors may be used.

2.3 LDO Design Procedure

The VTT LDO must handle the fast load transients from the DDR memory for termination. Therefore, it is recommended to use ceramic capacitors to maintain a high amount of capacitance with low ESR on the VTT LDO outputs and inputs.

The remaining LDOs must have input and output capacitors chosen based on the values in the datasheet.

3 Layout Guidelines

3.1 PCB Build Up

Before the layout is started, the PCB build up is needed to have a good strategy of what signals to place on each layer. There is a lot of theory to go through if a good and proper design is the goal; some of the theories are conflicting, so a complete foolproof strategy is not possible. Hence, the design of the PCB has trade-offs, and the strategy is important to get the best possible design even with the compromises. The recommendations in this document refer to a 6-layer PCB stackup with the TPS65086x device implemented. Designing with a minimum of 6 layers is a great general-purpose guideline for constructing a board with low electromagnetic interference (EMI). Additional layers may be incorporated into the PCB if needed, but they are not required to achieve an efficient design because all necessary routing for the TPS65086x can be accomplished in 6 layers. If complex designs warrant the need for more layers, the designer must always strive to preserve symmetry by using even numbered layer counts, as this helps prevent board warping during the fabrication process. Figure 4 shows the EVM board stack-up from top to bottom.

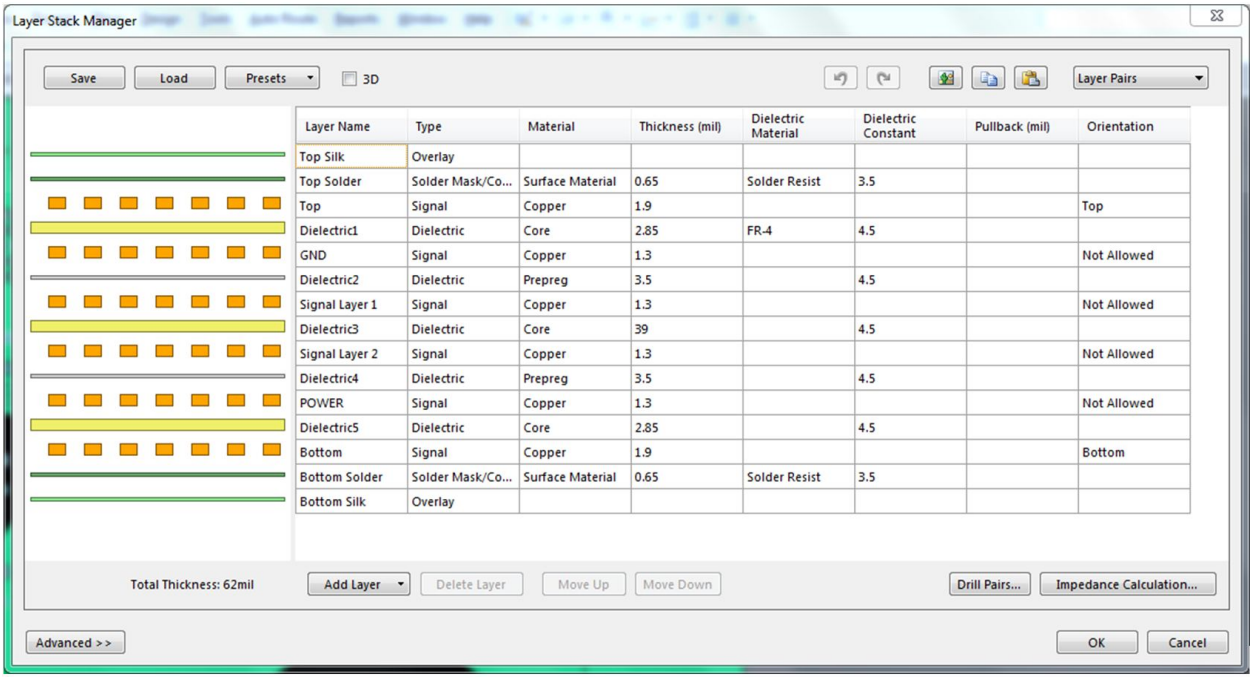


Figure 4. EVM Board Stackup

3.1.1 PCB Strategy

When defining the PCB build-up, there are a number of considerations to take into account. All of the options are related to cost and there will be tradeoffs between the cost and the options chosen. Figure 5 shows the TPS65086x device package and pin locations.

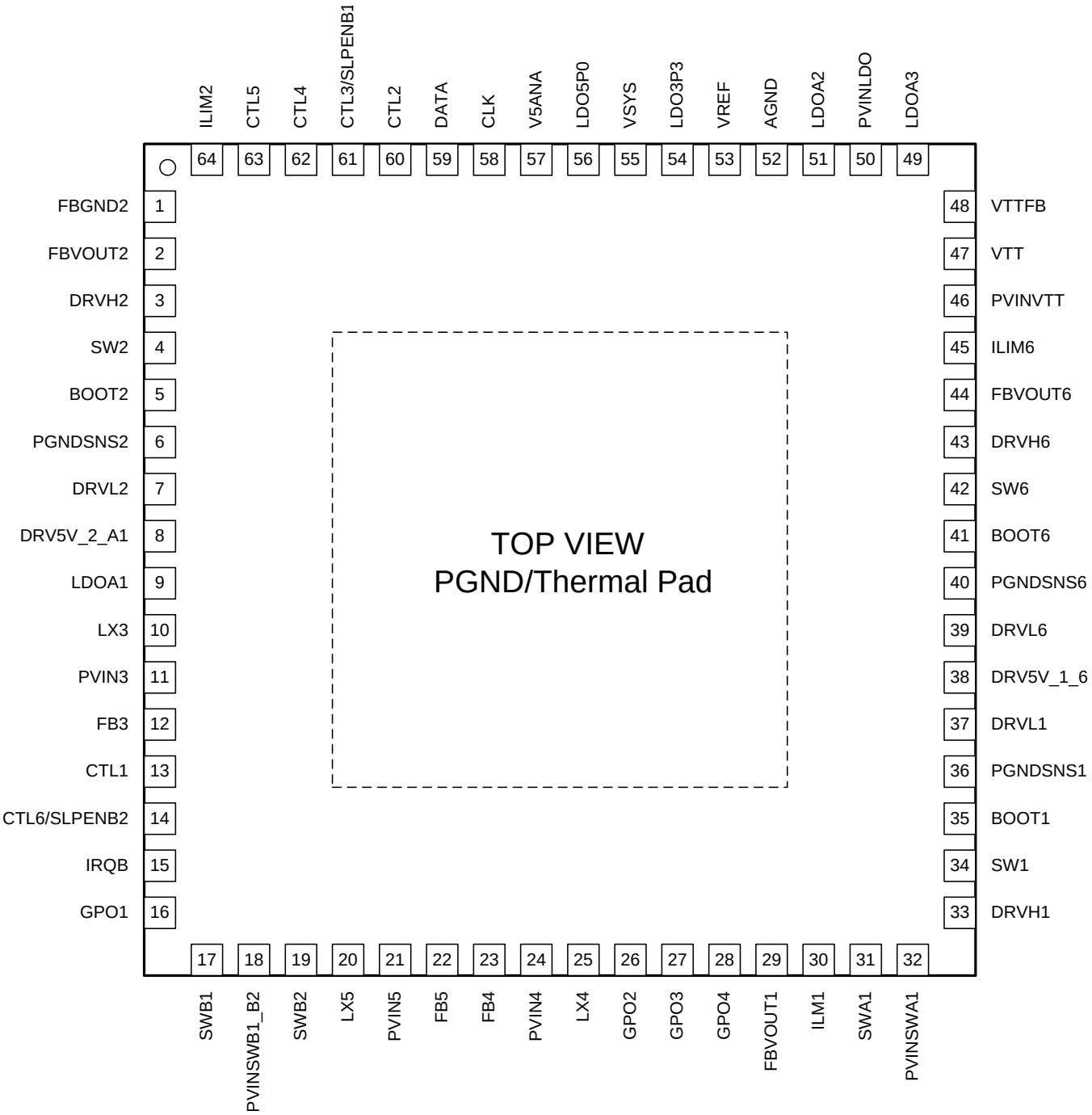


Figure 5. Device Package and Pin Locations

3.1.2 Layer Definition

Before starting the layout, a routing strategy needs to be defined by considering the physical location of specific signals.

Sensitive signals can be affected by aggressive signals which are routed close to them.

For instance, the ground loop of high-power consumption devices should not surround sensitive signals which are prone to EMI.

In Figure 6, signals are placed in the ground loop (layers 3, 4, and 5); this is not recommended. The signals in the ground loop are affected by the flux generated by the current in the loop. This must be avoided, especially when dealing with sensitive signals such as the reference voltage, and so forth.

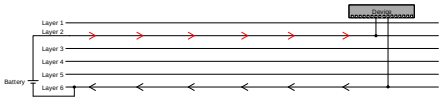


Figure 6. Example of Poor Ground Loop

The supply line and the ground path are both crucial. The supplies must be placed and calculated so that their flux does not affect any sensitive signals. The ground plane must be solid, especially close to the supply trace; if this is not considered, the risk for noise pollution increases. Moreover, no sensitive signals should be in parallel with the supply line and the corresponding ground path. As Figure 7 shows, the problem is solved by choosing other layers for supply and ground, with no signal layer between the ground loop. Some concerns still must be considered.

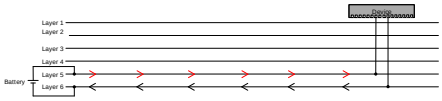


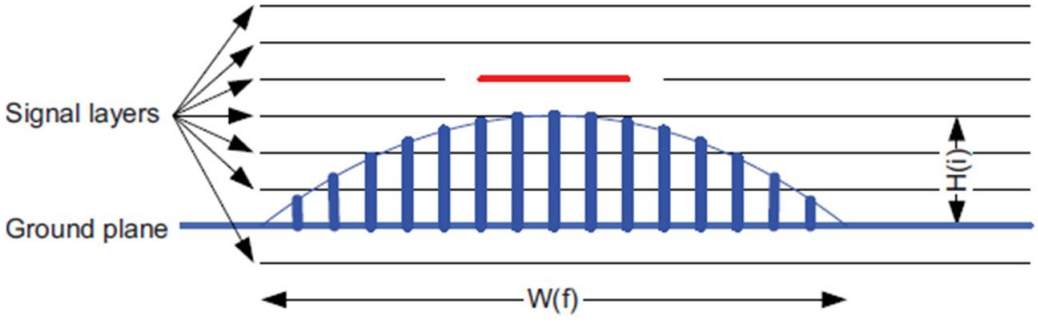
Figure 7. Example of Improved Ground Loop

The reason for not routing sensitive signals in parallel with the supply line and corresponding ground path is due to capacitive coupling across layers; the flux generated in either supply path or in ground path affects the neighboring layers. For high frequency, the current in the ground path approaches the one of the supply path. Figure 8 shows the flux in the ground path. This flux “cloud” is affected by frequency and current level.

The width of the flux is determined by the frequency; high frequency and the flux cloud will be very concentrated in parallel with the supply path.

The height is controlled mostly by the current level; higher current is equal to higher flux density and, therefore, can impact other layers.

For both the frequency and the current, the transition period is important. During this phase, the current shifts state and issues can arise due to the current change.



Note: The red trace is the supply track.

Figure 8. Frequency and Current Impact on Ground Plane

3.1.3 Signal Grouping

Critical signals for layout are classified as following:

- Sensitive signals
  - Reference
  - Voltage sense
  - SMPS feedbacks
- Power switching (aggressive signals)
  - Switching node of SMPS
  - VSYS to controllers/converters
  - Noisy grounds
- Power passive output lines (IR drops to be considered)
  - Output of LDOs
  - Output of switches
- Ground of DC-DC power (short, wide traces)
- Quiet GNDs
  - AGND (VREF)
  - LDO GND
  - Load Switch GND
  - ILIM GND
  - Limit resistivity between all grounds

Details about signal connections are provided in the *TPS65086x Schematic and Layout Checklist* (SLVA734).

3.1.4 Ground Strategy

There are several ground strategies which have advantages and drawbacks; the following strategy is advised. Use solid ground planes to decrease the resistance path and thus avoid voltage discrepancies. Do not use too many mechanical vias side-by-side which could obstruct the current flux in the ground plane. A good practice is to check the integrity of the ground planes at the end of PCB design by turning off all layers except the grounds.

3.1.4.1 Grounds Classification

Grounds can be classified as follows:

- Clean grounds
  - AGND (VREF)
  - ILIM GND
- Noisy grounds
  - Controller GND
  - Converter GND
- Nonaggressive grounds
  - LDO GND
  - Load Switch GND

Noisy grounds should not be connected to any other grounds on the top layer. All grounds should be merged in grounds planes, making sure that big enough via are used to connect power grounds to ground planes.

3.1.4.2 Clean Grounds

AGND and ILIM GND are reference grounds which should be protected from noisy signals.

3.2 External Components Choice

Placement of external components has to be done with engineering skills. The placement is expected to be affected by the mechanical dimension, and hereby also the placement of the TPS65086x device. The distance to the supplied devices (for example, the processor) must be considered when determining placement of the TPS65086x. The placement has requirements to both placement of external components and also to the possibility to route power lines from the integrated PMU to power consuming devices such as processors.

3.2.1 Placement Overview

In the following placement recommendations, the EVM board can be a reference regarding good part placement. Figure 9 shows the EVM component placement.

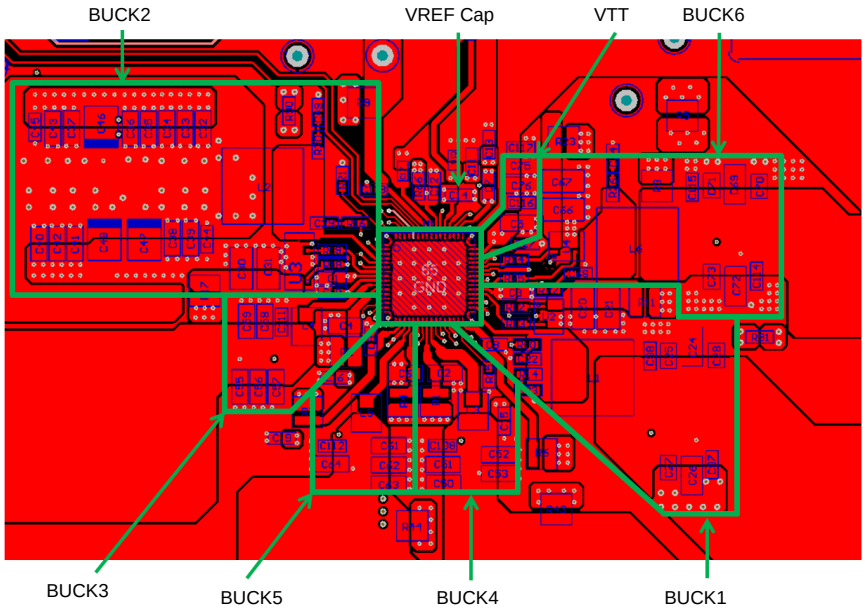


Figure 9. EVM Overall Layout

3.3 PCB General Layout Check List

- All inductors, input/output caps and FETs for the converters and controller should be on the same board layer as the IC.
- Place feedback connection points near the output capacitors and minimize the control feedback loop as much as possible to achieve the best regulation performance.
- Bootstrap capacitors should be placed near the IC from the SWx trace to the BOOTx pins.
- DRVLx signals must be routed on the same layer as the IC and the FETs and minimize the length and parasitic inductance of the trace as much as possible.
- The internal reference regulators must have their input and output caps close to the IC pins.

3.3.1 Controller

TPS65086x controllers have bootstrapped drivers optimized to drive external power FETs, thereby offer higher load current capability. Ideally external power FETs are placed close to the controller to achieve optimum performance and avoid EMI concerns.

The bootstrap capacitor should be placed close to the IC rather than near the FET, though other components, such as the input capacitors, will take a higher priority.

Controllers can be used to drive far end loads, if the end application accommodates PCB routing with lower trace parasitics and any potential EMI concerns. This requires good PCB routing and signal return paths need to be provided below the signals for minimum loop area.

- Input capacitors to the FET must be placed as close as possible to the FET, with excellent connections to both the VSYS plane and GND plane.
- SW trace needs to be routed below DRVH and ensure small return loop for minimum EMI.
- PGND needs to be routed below DRVL and ensure small return loop for minimum EMI.

NOTE: This is not PGNDSNS, but an actual PGND connection to the PowerPAD from the FET GND, typically through a second layer PGND plane.

- This routing is recommended but not required when not driving far end loads

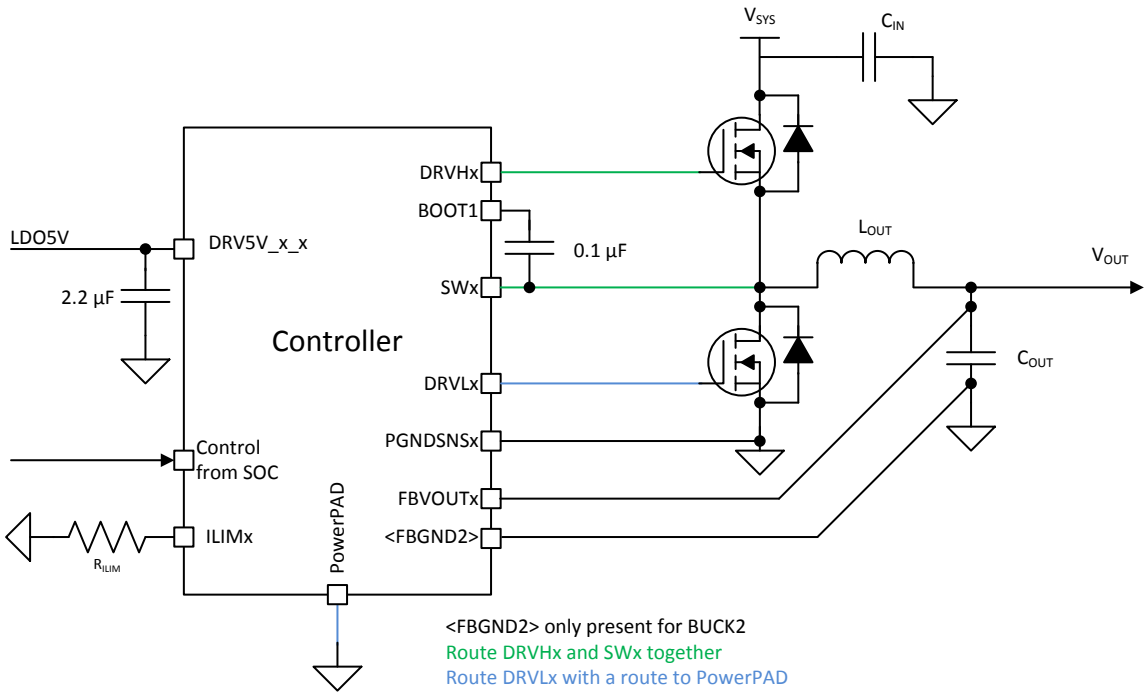


Figure 10. Schematic Example of Controller Layout

Limitations on length are set by parasitic inductance (approximately 8 nH, but will vary by application). By simulation, a 10-mil trace can support a max length of 1 in, 20-mil trace can support up to 3.5 in potentially. The addition of a damping resistor can improve performance at long length.

For the FET layout, the CSD87381P datasheet (SLPS405) has a good section regarding proper implementation. The primary concern here is the input capacitor must be as close as possible across the VIN and PGND pins of the FET. There need to be plenty of vias connecting these two planes on the top layer to their respective planes in the layer stack.

For the PGNDSNS node, it needs to be connected as close as possible to the FET PGND pad but out of the main current path to avoid any excess IR drop. Additionally, insure that the trace does not merge with the power GND plane at any point. This will require keep outs on the vias.

Output capacitor placement will vary based on requirements. For optimum load transient performance, it is recommended to place them near the load. Additionally, the output path to the load should be short and wide to minimize parasitics. It is not recommended to route the controller outputs long distances. If there are EMI concerns, capacitors can be placed near the inductor to reduce EMI on the output node, though SW node typically dominates.

Figure 11 shows an example from the EVM.

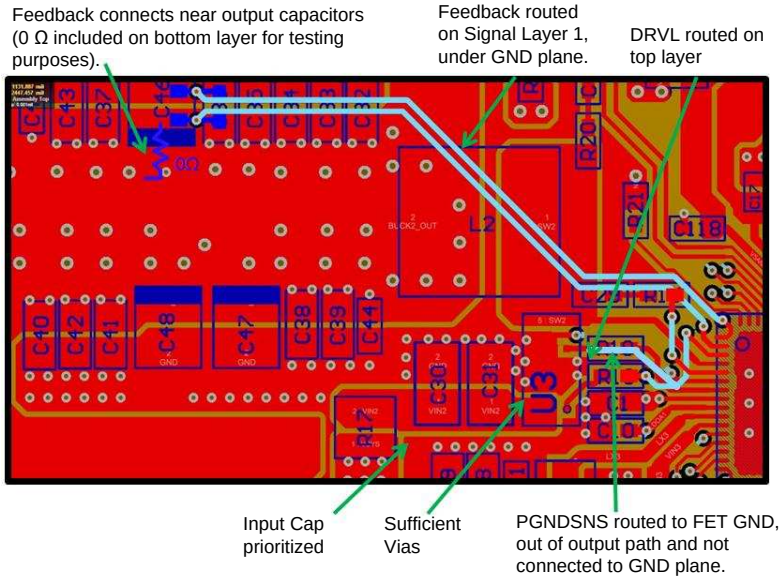


Figure 11. EVM Layout of Controllers

3.3.2 Converter

As for all switching power supplies, the board layout is an important step in the design. High-speed operation of the TPS65086x device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, low impedance ground path. Therefore, use wide and short traces for the main current paths along PVINx, LXx, and the PowerPAD.

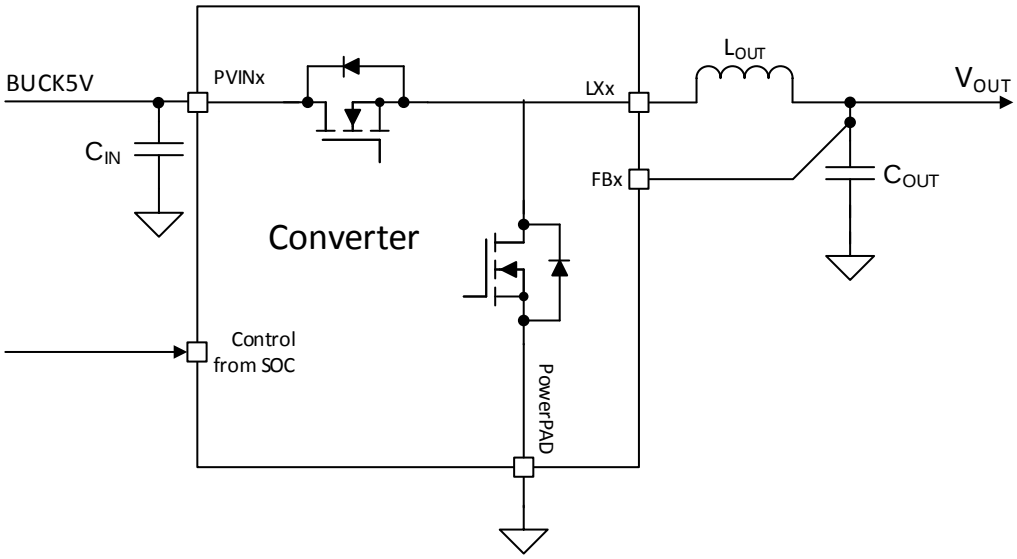


Figure 12. Schematic Example of Converter Layout

The input capacitors and inductor should be routed as close as possible to the IC with sufficiently wide and short traces. The load should be as close to the IC as possible.

Output capacitor placement will vary based on requirements. For optimum load transient performance, it is recommended to place them near the load. Additionally, the output path to the load should be short and wide to minimize parasitics. It is not recommended to route the converter outputs long distances. If there are EMI concerns, capacitors can be placed near the inductor to reduce EMI on the output node, though SW node typically dominates.

The output voltage sense line (FBx) should be connected to the center of the output capacitors and routed in a manner to minimize control loop area while also avoiding noisy nets (the SW node, for example). Its trace should be small and placed in a way where no signals can affect the voltage level, as that is used to adjust the output voltage from the BUCK converter.

The same output capacitor strategy can be used here as with the controllers.

Ideally, the sense line should not be routed on the same layer as switched lines, but on a lower layer isolated from switched lines by a ground plane, as shown in Figure 13.

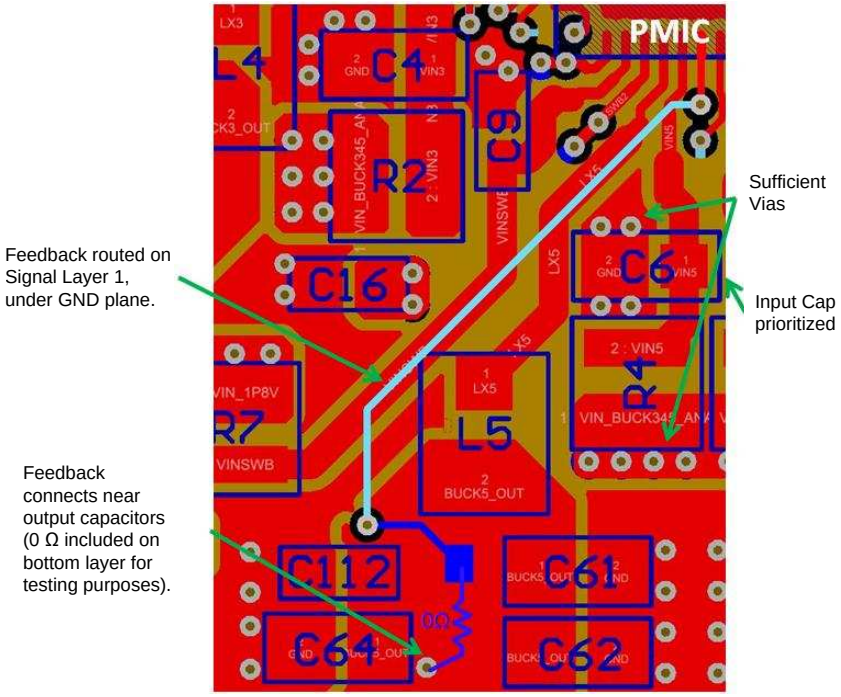


Figure 13. Example Converter Routing

3.3.3 Reference Voltage Routing

The reference voltage needs connection to an external capacitor (100 nF). Avoid aggressors signal surrounding the trace to the capacitor. The trace can be small due to low current on the reference.

The reference voltage requires a clean ground. Hence, the AGND ground is used as the ground connection for its filter capacitor. The AGND pin must be connected to a dedicated ground island. A dedicated ground island is connected to main ground in one point (with a via, shrunken ground plane, or shunt resistor). The ground island is located on the top layer.

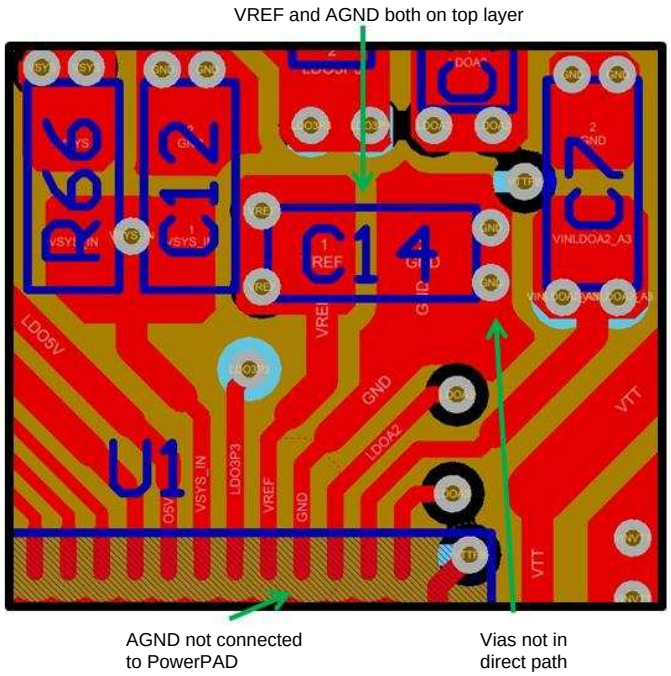


Figure 14. V_{REF} Layout

3.3.4 I^2C Interfaces

Interfaces can be aggressors due to high frequency; up to 1 MHz for I^2C. Avoid critical signals close to I^2C nets, or use large spacing between sensible signals (3x weight).

IMPORTANT NOTICE

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