ARM Cortex® -M4

32-bit Microcontroller

NuMicro™ Family
M451 Series Product Brief

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

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1 GENERAL DESCRIPTION

The NuMicro™ M451 series 32-bit microcontrollers are embedded with ARM® Cortex®-M4F core for industrial control and applications which need rich communication interfaces and high computing power.

The ARM® Cortex®-M4F core within NuMicro™ M451 series can run up to 72 MHz and support DSP extensions and Floating Point Unit (FPU) function. The NuMicro™ M451 series also supports 256/128 Kbytes embedded Flash, 32 Kbytes embedded SRAM and plenty of peripheral devices, such as USB OTG/Device, Timers, Watchdog Timers, RTC, PDMA, EBI, UART, Smart Card interface, SPI, I^2S, I^2C, CAN, PWM Timer, GPIO, 12-bit ADC, 12-bit DAC, touch key sensor, analog comparator, temperature sensor, Low voltage reset and Brown-out Detector.

Product Line	USB	CAN	UART	I^2C	I^2S	SPI	PWM	ADC	DAC	RTC
M453	●	●	●	●	●	●	●	●	●	●
M452	●	--	●	●	●	●	●	●	●	●
M451	--	--	●	●	●	●	●	●	●	●
M451M (M051 Pin Compatible)	--	--	●	●	●	●	●	●	●	--

Table 2.1-1 Key Features Support Table

The NuMicro™ M451 series is suitable for a wide range of applications such as:

- Industrial Automation
- PLCs
- Inverters
- Home Automation
- Security Alarm System
- Power Metering
- Portable Data Collector
- Portable RFID Reader
- System Supervisors
- Smart Card Reader
- Printer
- Bar Code Scanner
- Motor Control
- Digital Power

2 FEATURES

2.1 NuMicro™ M451 Features

- Core
  - ARM® Cortex®-M4F core running up to 72 MHz
  - Supports DSP extension with hardware divider
  - Supports IEEE 754 compliant Floating-point Unit (FPU)
  - Supports Memory Protection Unit (MPU)
  - One 24-bit system timer
  - Supports Low Power Sleep mode by WFI and WFE instructions
  - Single-cycle 32-bit hardware multiplier
  - Supports programmable 16 level priorities of Nested Vectored Interrupt Controller (NVIC)
  - Supports programmable mask-able interrupts
- Built-in LDO for wide operating voltage ranged from 2.5V to 5.5V
- Flash Memory
  - Supports 40/72/128/256 KB application ROM (APROM)
  - Supports 4 KB Flash for loader (LDROM)
  - Supports Data Flash with configurable memory size
  - Supports In-System-Programming (ISP), In-Application-Programming (IAP) update embedded flash memory
  - Supports 2 KB page erase for all embedded flash
- Boot Loader
  - 16 KB embedded ROM
  - Supports Nuvoton native In-System-Programming (ISP) for UART0, SPI0, I^2C0, CAN[*1] and USB[*2]
  - Supports direct boot from Boot Loader by pin selection
- SRAM Memory
  - 32/16 KB embedded SRAM
  - 16/8 KB with hardware parity check
  - Supports byte-, half-word- and word-access
  - Supports exception (NMI) generated once a parity check error occurs
  - Supports PDMA mode
- PDMA (Peripheral DMA)
  - Supports 12/8 independent configurable channels for automatic data transfer between memories and peripherals
  - Supports Normal and Scatter-Gather Transfer modes
  - Supports two types of priorities modes: Fixed-priority and Round-robin modes
  - Supports byte-, half-word- and word-access
  - Auto increment of the source and destination address
  - Supports single and burst transfer type
- Clock Control
  - Built-in 22.1184 MHz internal high speed RC oscillator (HIRC) for system operation (variation < 2% at -40˚C ~ +105˚C)
  - Built-in 10 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation
  - Built-in 4~20 MHz external high speed crystal oscillator (HXT) for precise timing operation
  - Built-in 32.768 kHz external low speed crystal oscillator (LXT) for RTC function and low-power system operation
  - Supports one PLL up to 144 MHz for high performance system operation, sourced

from HIRC and HXT
- Supports clock failure detection for high/low speed external crystal oscillator
- Supports exception (NMI) generated once a clock failure detected
- Supports clock output

● GPIO
- Four I/O modes
- TTL/Schmitt trigger input selectable
- I/O pin configured as interrupt source with edge/level trigger setting
- Supports high driver and high sink current I/O (up to 20 mA at 5V)
- Supports software selectable slew rate control
- Supports 5V-tolerance function
- Supports up to 85/55/42 GPIOs for LQFP100/64/48 respectively

● Timer
- Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
- Independent clock source for each timer
- Provides One-shot, Periodic, Toggle and Continuous Counting operation modes
- Supports event counting function to count the event from external pin
- Supports input capture function to capture or reset counter value

● Watchdog Timer
- Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT
- 8 selectable time-out period from 1.6ms ~ 26.0sec (depending on clock source)
- Able to wake up from Power-down or Idle mode
- Interrupt or reset selectable on watchdog time-out

● Window Watchdog Timer
- Supports multiple clock sources from HCLK/2048 (default selection) and LIRC
- Window set by 6-bit counter with 11-bit prescale
- Able to wake up from Power-down or Idle mode
- Interrupt or reset selectable on time-out

● RTC
- Supports external power pin V_{BAT}
- Supports software compensation by setting frequency compensate register (FCR)
- Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
- Supports Alarm registers (second, minute, hour, day, month, year)
- Selectable 12-hour or 24-hour mode
- Automatic leap year recognition
- Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports wake-up function
- Supports 80 bytes spare registers
- Programmable spare register erase function
- Supports 32KHz Oscillator gain control
- Supports tamper detection function

● PWM
- Supports up to 12 independent PWM outputs with 16-bit resolution
- Supports maximum clock frequency up to 144MHz
- Supports 12-bit clock prescale
- Supports one-shot or auto-reload counter operation mode
- Supports up, down or up-down PWM counter type
- Supports synchronous function
- Supports dead time with maximum divided 12-bit prescale
- Supports brake function source from pin, comparator output and system safety events
- Supports PWM auto recovery function after brake condition removed

- Supports mask function and tri-state output for each PWM pin
- Supports PWM events interrupt
- Supports trigger EADC/DAC start conversion
- Supports up to 12 independent input capture channels with rising/falling capture and with counter reload option
- Supports capture counter with 16-bit resolution
- Supports capture interrupt
- Supports capture PDMA mode

● UART

- Supports up to four UARTs – UART0, UART1, UART2 and UART3
- Supports 16-byte FIFOs with programmable level trigger
- Supports auto flow control (CTS and RTS)
- Supports IrDA (SIR) function
- Supports RS-485 9-bit mode and direction control
- UART0 and UART1 support LIN function
- Programmable baud-rate generator up to 1/16 system clock
- Supports wake-up function
- Supports PDMA mode

● Smart Card Interface

- One set of ISO-7816-3 port
- Compliant to ISO-7816-3 T=0, T=1
- Separate receive / transmit 4 bytes entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 266 ETU)
- A 24-bit and two 8 bit time-out counters for Answer to Request (ATR) and waiting times processing
- Supports auto inverse convention function
- Supports stop clock level and clock stop (clock keep) function
- Supports transmitter and receiver error retry and error limit function
- Supports hardware activation/deactivation sequence process
- Supports hardware warm reset sequence process
- Supports hardware auto deactivation sequence when detect the card is removal
- Supports UART function

● SPI

- Supports one set of SPI Quad controller – SPI0
- Supports Master or Slave mode operation
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transfer word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports the byte reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA mode
- Supports 3-wired, no slave select signal, bi-direction interface
- Master up to 32 MHz, and Slave up to 16 MHz (when chip works at V_{DD} = 5V)

● SPI/ I^2S

- Supports up to two sets of SPI controllers – SPI1 and SPI2
- Supports Master or Slave mode operation
- Configurable bit length of a transfer word from 8 to 32-bit
- Provides separate 4-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence

- Supports the byte reorder function
- Supports Byte or Word Suspend mode
- Supports 3-wire, no slave select signal, bi-direction interface
- Master mode up to 36 MHz and Slave mode up to 18 MHz (when chip works at V_{DD} = 5V)
- Supports up to two sets of I^2S by SPI controllers – SPI1 and SPI2
- Interface with external audio CODEC
- Supports Master and Slave mode
- Capable of handling 8-, 16-, 24- and 32-bit word sizes
- Supports mono and stereo audio data
- Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
- Each provides two 4-word FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Each supports two PDMA requests, one for transmitting and the other for receiving

● I^2C

- Supports up to two sets of I^2C devices
- Supports Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Programmable clocks allow versatile rate control
- Supports multiple address recognition (four slave address with mask option)
- Supports SMBus and PMBus
- Supports speed up to 1Mbps
- Supports multi-address Power-down wake-up function

● CAN 2.0

- Supports up to one set of CAN controller
- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1M bit/s
- Each supports 32 Message Objects
- Each Message Object has its own identifier mask
- Programmable FIFO mode (concatenation of Message Object)
- Supports interrupts
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications
- Supports power-down wake-up function

● USB 2.0 FS Controller

- Supports one set of USB 2.0 FS OTG (M45xG/M45xE Only)
- FS Host compatible with Open HCI 1.0 specification (M45xG/M45xE Only)
- Compliant to USB specification version 2.0
- OTG compliant with USB OTG Supplement 1.3 (M45xG/M45xE Only)
- On-chip USB Transceiver
- Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
- Auto suspend function when no bus signaling for 3 ms
- Provides 8 programmable endpoints
- Supports 512 Bytes internal SRAM as USB buffer
- Provides remote wake-up capability
- On-chip 5V to 3.3V LDO for USB PHY

- EBI
  - Supports two dedicated external chip select pins for each memory block
  - Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out
  - Supports 8-/16-bit data width
  - Supports byte write in 16-bit data width mode
  - Supports PDMA mode
  - Supports Address/Data multiplexed Mode
  - Supports Timing parameters individual adjustment for each memory block
- EADC
  - Analog input voltage range: 0~ V_{REF} (Max to AV_{DD})
  - Supports single 12-bit SAR ADC conversion
  - 12-bit resolution and 10-bit accuracy is guaranteed
  - Up to 1MSPS conversion rate at 5.0V
  - Up to 16 external single-ended analog input channels
  - Up to 8 differential analog input pairs
  - Supports single ADC interrupt
  - Supports external V_{REF} pin
  - Support internal reference voltages from Band-gap and Voltage divider
  - An A/D conversion can be triggered by Software enable, External pin, Timer 0~3 overflow pulse trigger and PWM trigger
  - Supports 3 internal channels for V_{BAT}, band-gap VBG input and Temperature sensor input
  - Supports PDMA transfer
- DAC
  - Supports a 12-bit voltage type DAC
  - Rail to rail settle time 8us
  - External reference voltage V_{REF}
  - Max. output voltage AV_{DD} -0.2V at buffer mode
  - Conversion started by software enable or PDMA trigger
  - Supports PDMA mode
- Touch Key (M45xG/M45xE Only)
  - Supports up to 16 touch keys
  - Supports programmable sensitivity adjustment for each channel
  - Supports programmable scan speed for different applications
  - Supports any key Wake-up for low-power applications
  - Supports manual/one-time or periodic key-scan initiation
  - Supports programmable interrupt options for automatic key-scan and interrupt generation
- Analog Comparator
  - Up to two rail-to-rail analog comparators
  - Supports a multiplexed I/O pin at positive node.
  - Supports I/O pins, band-gap, Voltage divider and DAC output at negative node
  - Supports programmable speed and power consumption
  - Interrupts generated when compare results change (Interrupt event condition is programmable)
  - Supports Power-down Wake-up
  - Supports triggers for break events and cycle-by-cycle control for PWM
- Cyclic Redundancy Calculation Unit
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - Programmable initial value
  - Supports programmable order reverse setting for input data and CRC checksum

- Supports programmable 1's complement setting for input data and CRC checksum.
- Supports 8-/16-/32-bit of data width
- Interrupt generated once checksum error occurs

- Voltage Adjustable Interface
  - Supports user Configurable 1.8~5.5V I/O Interface with a dedicated power input (V_{DDIO})
  - Supports UART1, SPI0, SPI1, I^2C1 or I^2C0 interface
- Supports 96-bit Unique ID (UID)
- Supports 128-bit Unique Customer ID (UCID)
- One built-in temperature sensor with 1℃ resolution
- Brown-out detector
  - With 4 levels: 4.4 V/ 3.7 V/ 2.7 V/ 2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 2.0 V
- Operating Temperature: -40℃~105℃
- Packages
  - All Green package (RoHS)
  - LQFP 100-pin (14mm x 14mm)
  - LQFP 64-pin (10mm x 10mm)
  - LQFP 64-pin (7mm x 7mm)
  - LQFP 48-pin (7mm x 7mm)

Note:
*1: For optional part numbers which support CAN
*2: For optional part numbers which support USB

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ M451 Selection Guide

3.1.1 NuMicro™ M451 Naming Rule

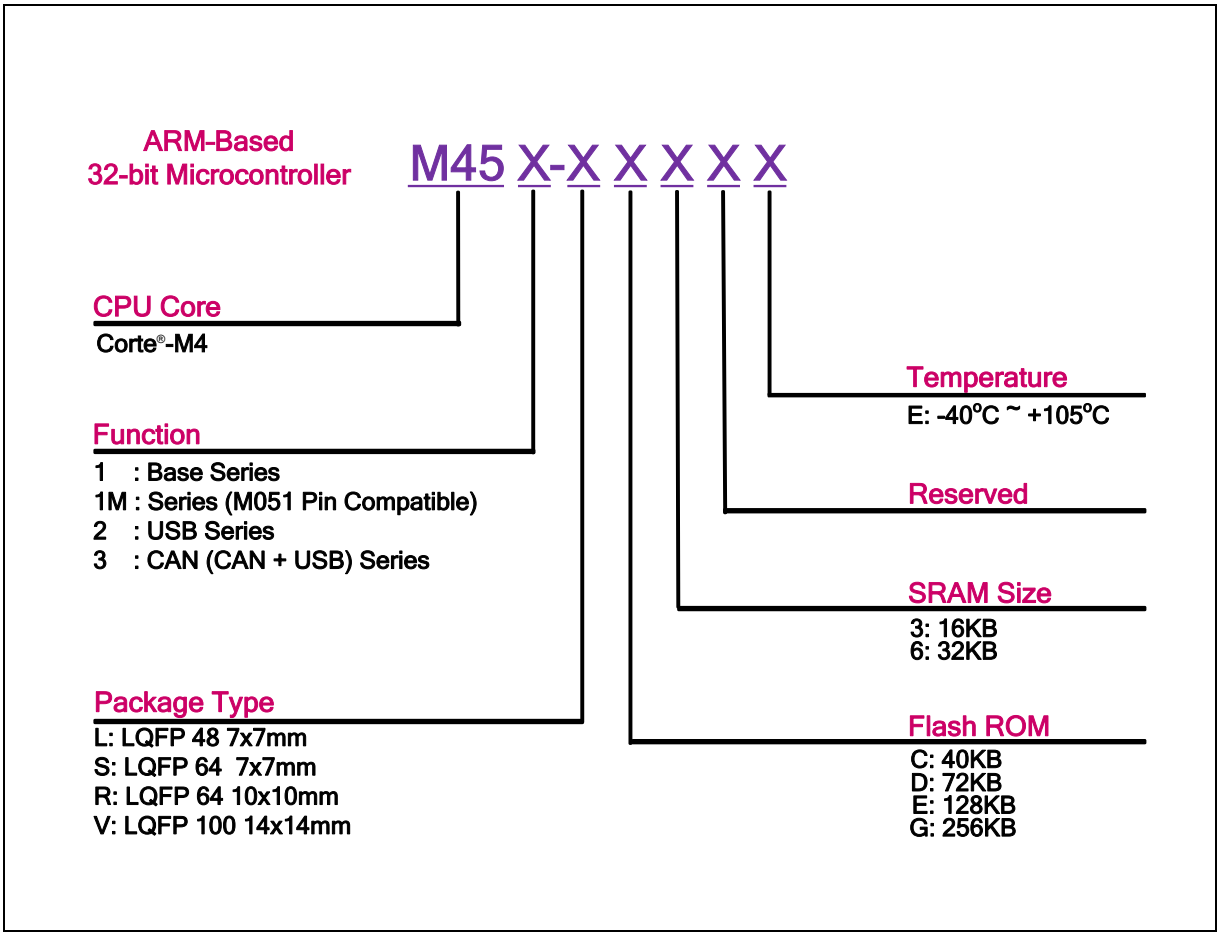


Figure 3.1-1 NuMicro™ M451 Selection Code

In this document, M45xG means the part numbers which include 256 KB Flash, M45xE means the part numbers which include 128 KB Flash, M45xD means the part numbers which include 72 KB Flash, M45xC means the part numbers which include 40 KB Flash.

3.1.2 NuMicro™ M451 Base Series Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP Loader ROM (KB)	I/O	Timer	Connectivity						I^2S	USB	PWM	Analog Comp.	DAC (12-Bit)	ADC (12-Bit)	Touch Key	RTC	ICP/ISPI/AP	Package
						UART*	SC* (ISO-7816)	SPI	I^2C	CAN	LIN										
M451LG6AE	256	32	4	39	4	3+1	1	3	2	--	2	2	--	12	2	√	8-ch	6	√	√	LQFP 48
M451LE6AE	128	32	4	39	4	3+1	1	3	2	--	2	2	--	12	2	√	8-ch	6	√	√	LQFP 48
M451RG6AE	256	32	4	53	4	4+1	1	3	2	--	2	2	--	12	2	√	12-ch	11	√	√	LQFP 64
M451RE6AE	128	32	4	53	4	4+1	1	3	2	--	2	2	--	12	2	√	12-ch	11	√	√	LQFP 64
M451VG6AE	256	32	4	85	4	4+1	1	3	2	--	2	2	--	12	2	√	16-ch	16	√	√	LQFP 100
M451VE6AE	128	32	4	85	4	4+1	1	3	2	--	2	2	--	12	2	√	16-ch	16	√	√	LQFP 100
M451LD3AE	72	16	4	39	4	4+1	1	2	2	--	2	1	--	12	2	√	10-ch	--	√	√	LQFP 48
M451LC3AE	40	16	4	39	4	4+1	1	2	2	--	2	1	--	12	2	√	10-ch	--	√	√	LQFP 48
M451RD3AE	72	16	4	53	4	4+1	1	2	2	--	2	1	--	12	2	√	16-ch	--	√	√	LQFP 64
M451RC3AE	40	16	4	53	4	4+1	1	2	2	--	2	1	--	12	2	√	16-ch	--	√	√	LQFP 64

*Marked in this table (4+1) means 4 UART + 1 SC UART

*SC (ISO-7816) supports full duplex UART mode

3.1.3 NuMicro™ M451M Series (M051 Pin Compatible) Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP Loader ROM (KB)	I/O	Timer	Connectivity						I²S	USB	PWM	Analog Comp.	DAC (12-Bit)	ADC (12-Bit)	Touch Key	RTC	ICP/ISPI/AP	Package
						UART*	SC* (ISO-7816)	SPI	I²C	CAN	LIN										
M451MLG6AE	256	32	4	42	4	3+1	1	3	2	--	2	2	--	12	2	√	9-ch	10	--	√	LQFP 48
M451MLE6AE	128	32	4	42	4	3+1	1	3	2	--	2	2	--	12	2	√	9-ch	10	--	√	LQFP 48
M451MLD3AE	72	16	4	42	4	4+1	1	2	2	--	2	1	--	12	2	√	11-ch	--	--	√	LQFP 48
M451MLC3AE	40	16	4	42	4	4+1	1	2	2	--	2	1	--	12	2	√	11-ch	--	--	√	LQFP 48
M451MSD3AE	72	16	4	55	4	4+1	1	2	2	--	2	1	--	12	2	√	13-ch	--	--	√	LQFP 64
M451MSC3AE	40	16	4	55	4	4+1	1	2	2	--	2	1	--	12	2	√	13-ch	--	--	√	LQFP 64

*Marked in this table (4+1) means 4 UART + 1 SC UART

*SC (ISO-7816) supports full duplex UART mode

3.1.4 NuMicro™ M452 USB Series Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP Loader ROM (KB)	I/O	Timer	Connectivity						I²S	USB	PWM	Analog Comp.	DAC (12-Bit)	ADC (12-Bit)	Touch Key	RTC	ICP/ISPI/AP	Package
						UART*	SC* (ISO-7816)	SPI	I²C	CAN	LIN										
M452LG6AE	256	32	4	34	4	3+1	1	3	2	--	2	2	OTG	10	2	√	8-ch	6	√	√	LQFP 48
M452LE6AE	128	32	4	34	4	3+1	1	3	2	--	2	2	OTG	10	2	√	8-ch	6	√	√	LQFP 48
M452RG6AE	256	32	4	48	4	4+1	1	3	2	--	2	2	OTG	12	2	√	12-ch	11	√	√	LQFP 64
M452RE6AE	128	32	4	48	4	4+1	1	3	2	--	2	2	OTG	12	2	√	12-ch	11	√	√	LQFP 64
M452LD3AE	72	16	4	35	4	4+1	1	2	2	--	2	1	Device	10	2	√	10-ch	--	√	√	LQFP 48
M452LC3AE	40	16	4	35	4	4+1	1	2	2	--	2	1	Device	10	2	√	10-ch	--	√	√	LQFP 48
M452RD3AE	72	16	4	49	4	4+1	1	2	2	--	2	1	Device	12	2	√	16-ch,	--	√	√	LQFP 64

*Marked in this table (4+1) means 4 UART + 1 SC UART

*SC (ISO-7816) supports full duplex UART mode

3.1.5 NuMicro™ M453 CAN Series (CAN+USB) Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP Loader ROM (KB)	I/O	Timer	Connectivity						I^2S	USB	PWM	Analog Comp.	DAC (12-Bit)	ADC (12-Bit)	Touch Key	RTC	ICP/ISPI/AP	Package
						UART*	SC* (ISO-7816)	SPI	I^2C	CAN	LIN										
M453LG6AE	256	32	4	34	4	3+1	1	3	2	√	2	2	OTG	10	2	1	8-ch	6	√	√	LQFP 48
M453LE6AE	128	32	4	34	4	3+1	1	3	2	√	2	2	OTG	10	2	1	8-ch	6	√	√	LQFP 48
M453RG6AE	256	32	4	48	4	4+1	1	3	2	√	2	2	OTG	12	2	1	12-ch	11	√	√	LQFP 64
M453RE6AE	128	32	4	48	4	4+1	1	3	2	√	2	2	OTG	12	2	1	12-ch	11	√	√	LQFP 64
M453VG6AE	256	32	4	80	4	4+1	1	3	2	√	2	2	OTG	12	2	1	16-ch	16	√	√	LQFP 100
M453VE6AE	128	32	4	80	4	4+1	1	3	2	√	2	2	OTG	12	2	1	16-ch	16	√	√	LQFP 100
M453LD3AE	72	16	4	35	4	4+1	1	2	2	√	2	1	Device	10	2	1	10-ch	--	√	√	LQFP 48
M453LC3AE	40	16	4	35	4	4+1	1	2	2	√	2	1	Device	10	2	1	10-ch	--	√	√	LQFP 48
M453RD3AE	72	16	4	49	4	4+1	1	2	2	√	2	1	Device	12	2	1	16-ch,	--	√	√	LQFP 64
M453VD3AE	72	16	4	72	4	4+1	1	2	2	√	2	1	Device	12	2	1	16-ch	--	√	√	LQFP 100

*Marked in this table (4+1) means 4 UART + 1 SC UART

*SC (ISO-7816) supports full duplex UART mode

3.2 Pin Configuration

3.2.1 NuMicro™ M451 Base Series LQFP48 Pin Diagram

Corresponding Part Number: M451LG6AE, M451LE6AE, M451LD3AE, M451LC3AE

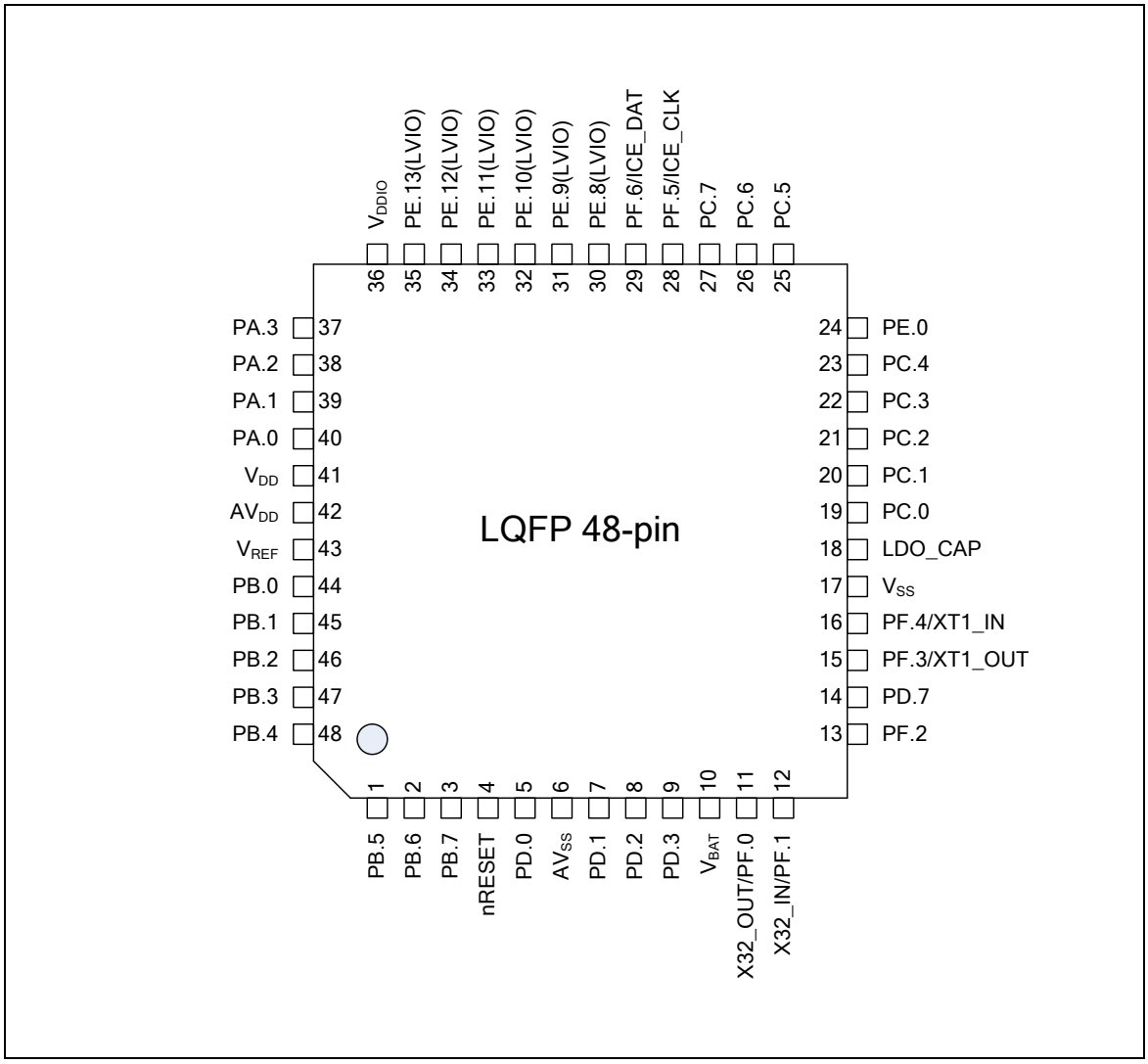


Figure 3.2-1 NuMicro™ M451 Base Series LQFP 48-pin Diagram

3.2.2 NuMicro™ M451 Base Series LQFP64 Pin Diagram

Corresponding Part Number: M451RG6AE, M451RE6AE, M451RD3AE, M451RC3AE

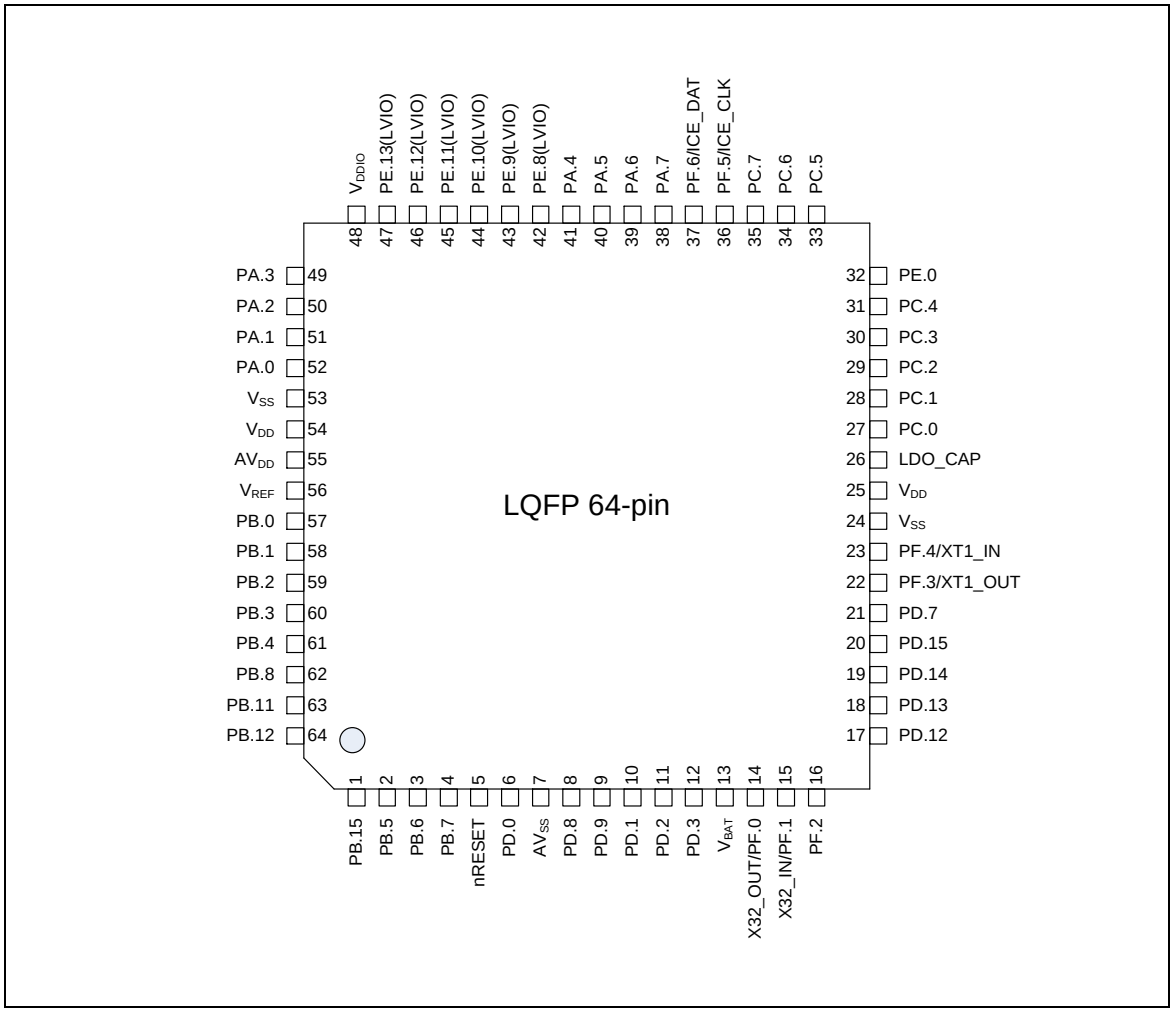


Figure 3.2-2 NuMicro™ M451 Base Series LQFP 64-pin Diagram

3.2.3 NuMicro™ M451 Base Series LQFP100 Pin Diagram

Corresponding Part Number: M451VG6AE, M451VE6AE

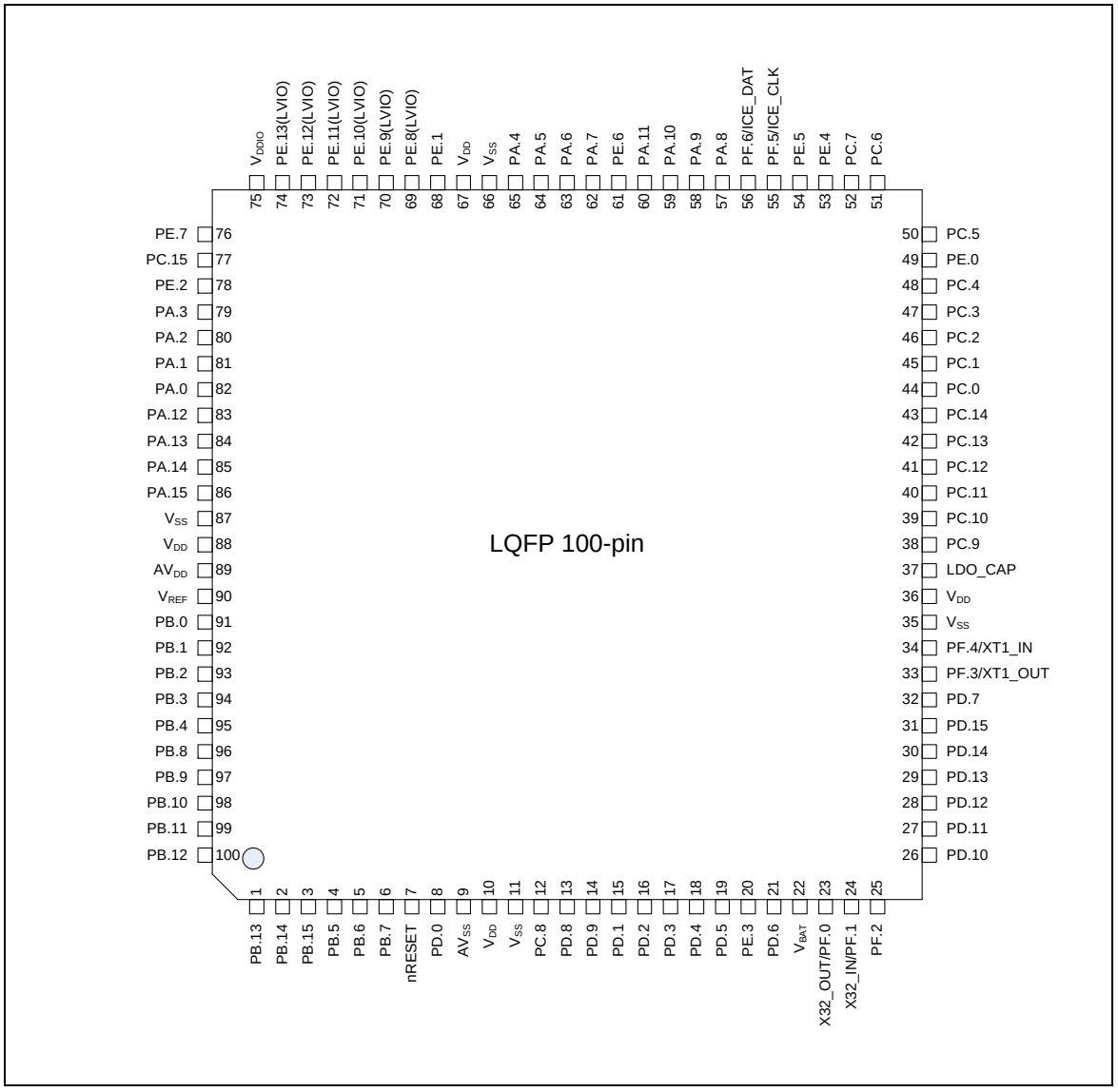


Figure 3.2-3 NuMicro™ M451 Base Series LQFP 100-pin Diagram

3.2.4 NuMicro™ M451M Series (M051 Pin Compatible) LQFP48 Pin Diagram

Corresponding Part Number: M451MLG6AE, M451MLE6AE, M451MLD3AE, M451MLC3AE

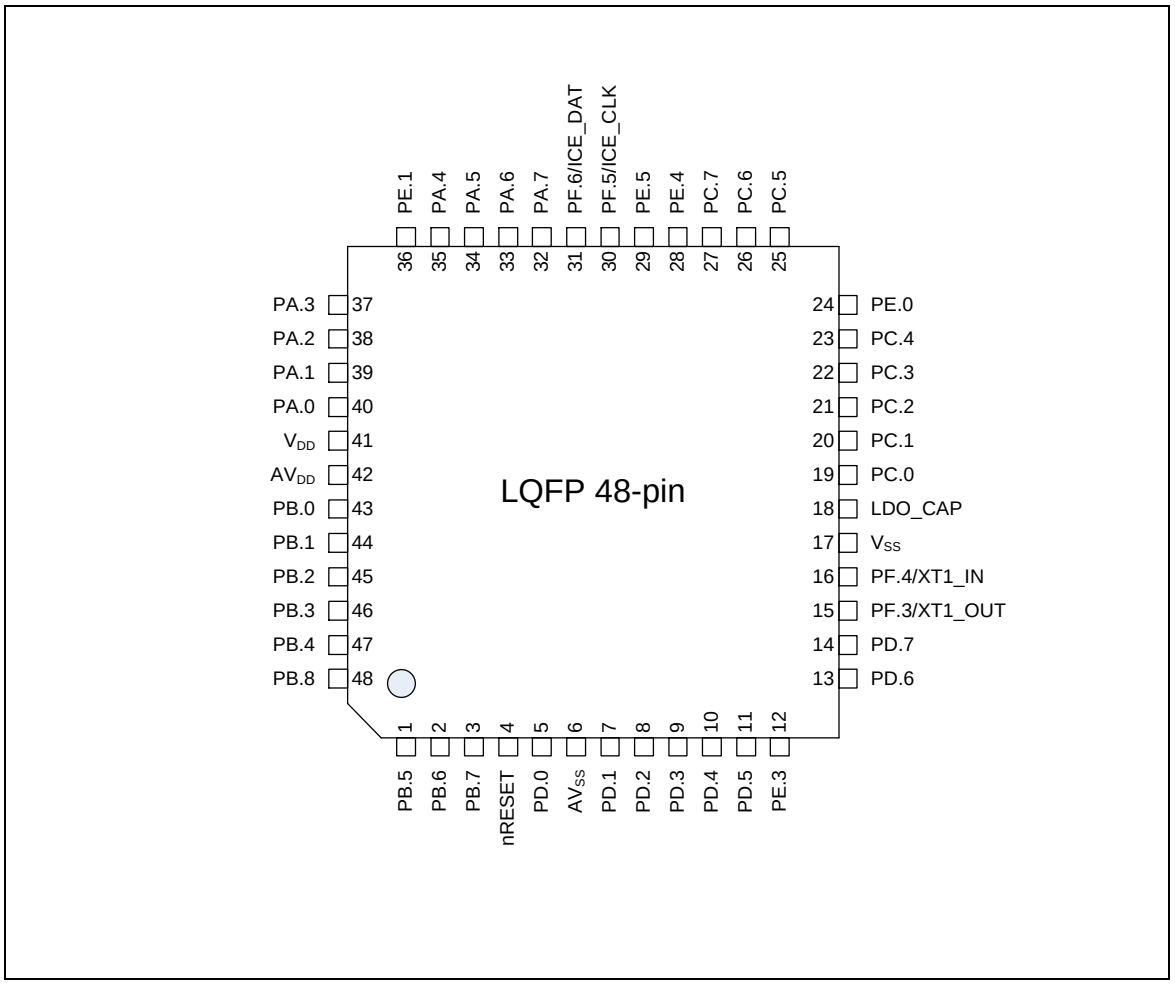


Figure 3.2-4 NuMicro™ M451M Base Series (Pin Compatible with M051) LQFP 48-pin Diagram

3.2.5 NuMicro™ M451M Series (M058S Pin Compatible) LQFP64 Pin Diagram

Corresponding Part Number: M451MSD3AE, M451MSC3AE

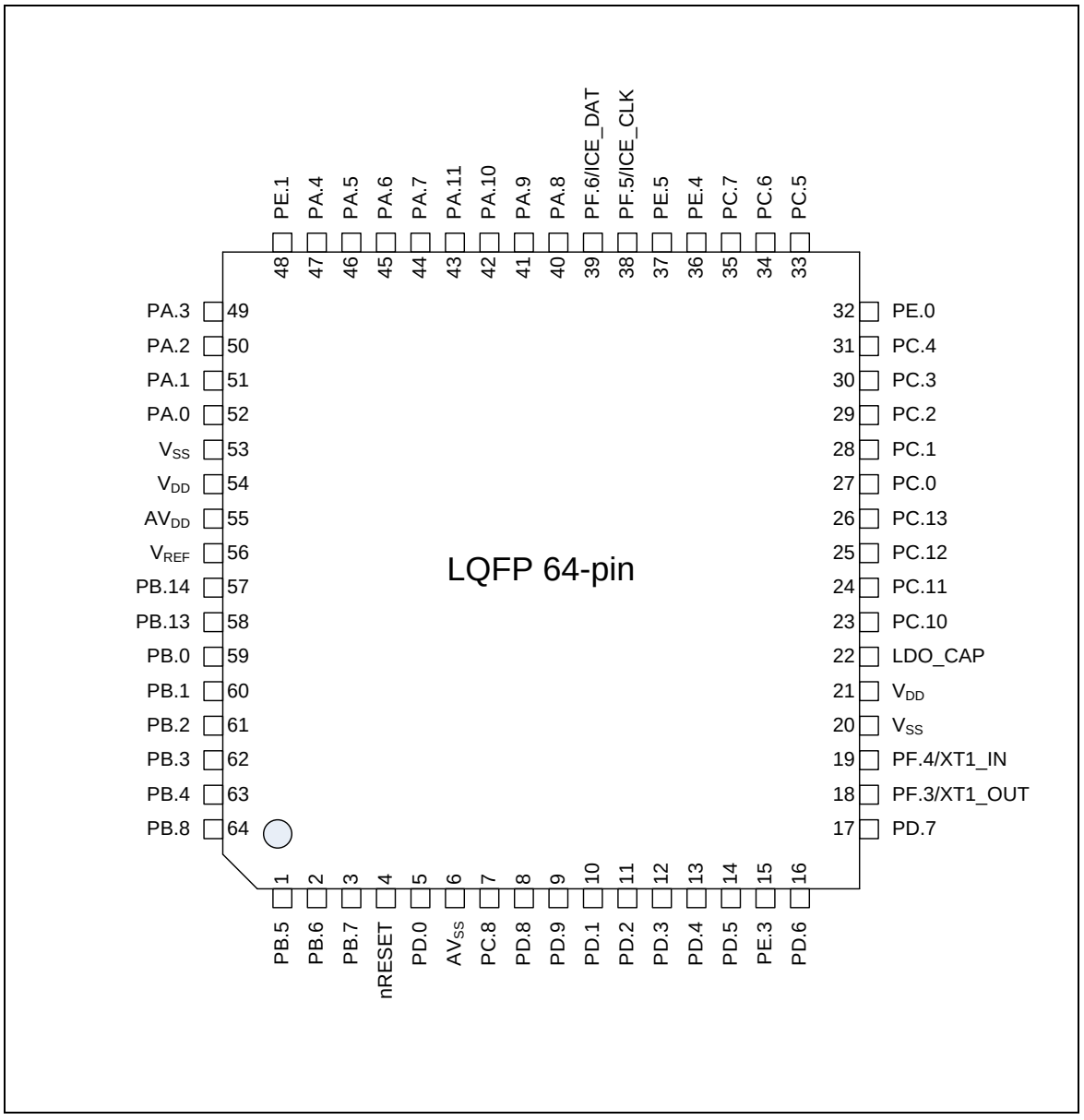


Figure 3.2-5 NuMicro™ M451M Base Series (Pin Compatible with M058S) LQFP 64-pin Diagram

3.2.6 NuMicro™ M452 USB Series LQFP48 Pin Diagram

Corresponding Part Number: M452LG6AE, M452LE6AE

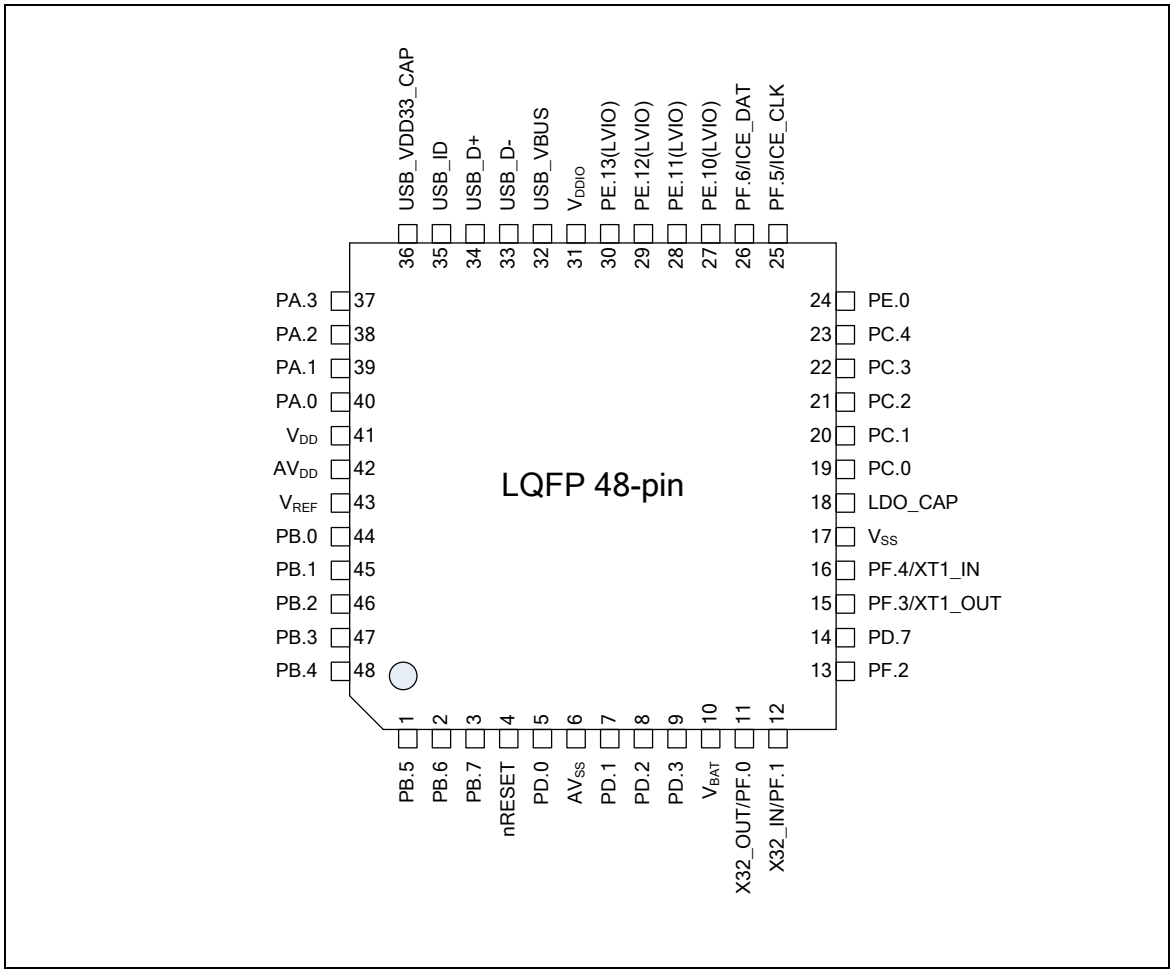


Figure 3.2-6 NuMicro™ M451 USB Series LQFP 48-pin Diagram (M452LG/M452LE Device Only)

Corresponding Part Number: M452LD3AE, M452LC3AE

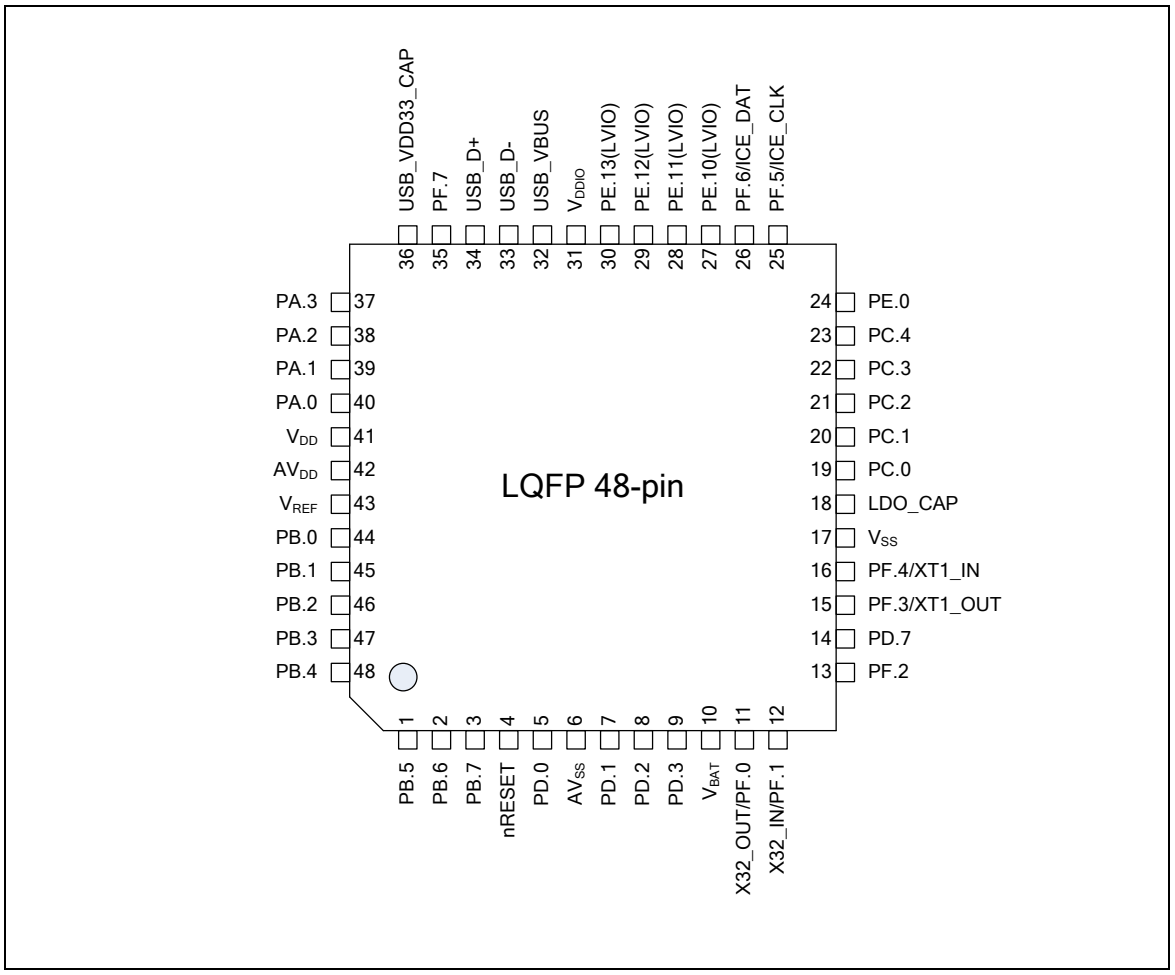


Figure 3.2-7 NuMicro™ M451 USB Series LQFP 48-pin Diagram (M452LD/M452LC Device Only)

3.2.7 NuMicro™ M452 USB Series LQFP64 Pin Diagram

Corresponding Part Number: M452RG6AE, M452RE6AE

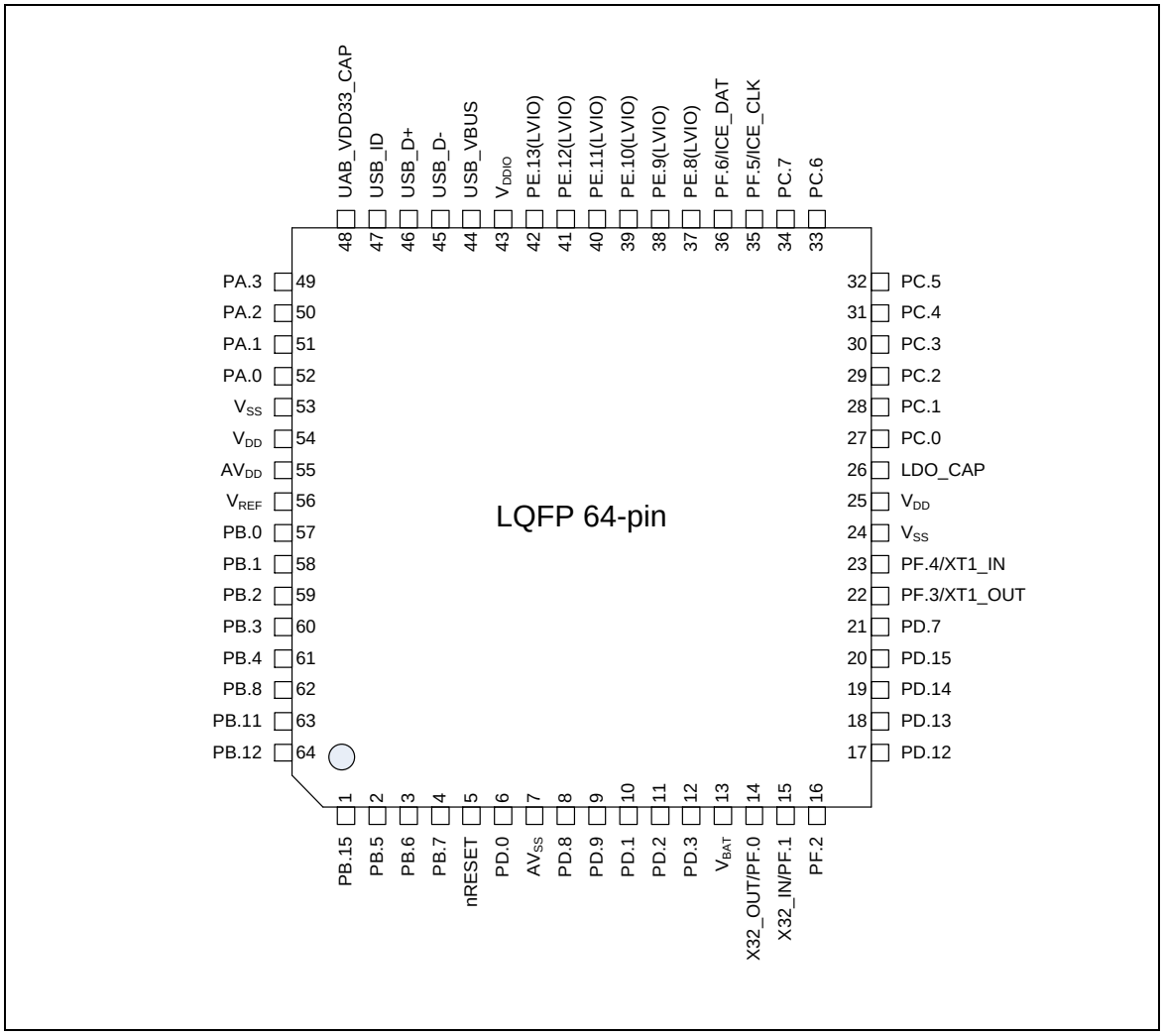


Figure 3.2-8 NuMicro™ M451 USB Series LQFP 64-pin Diagram (M452RG/M452RE Device Only)

Corresponding Part Number:M452RD3AE

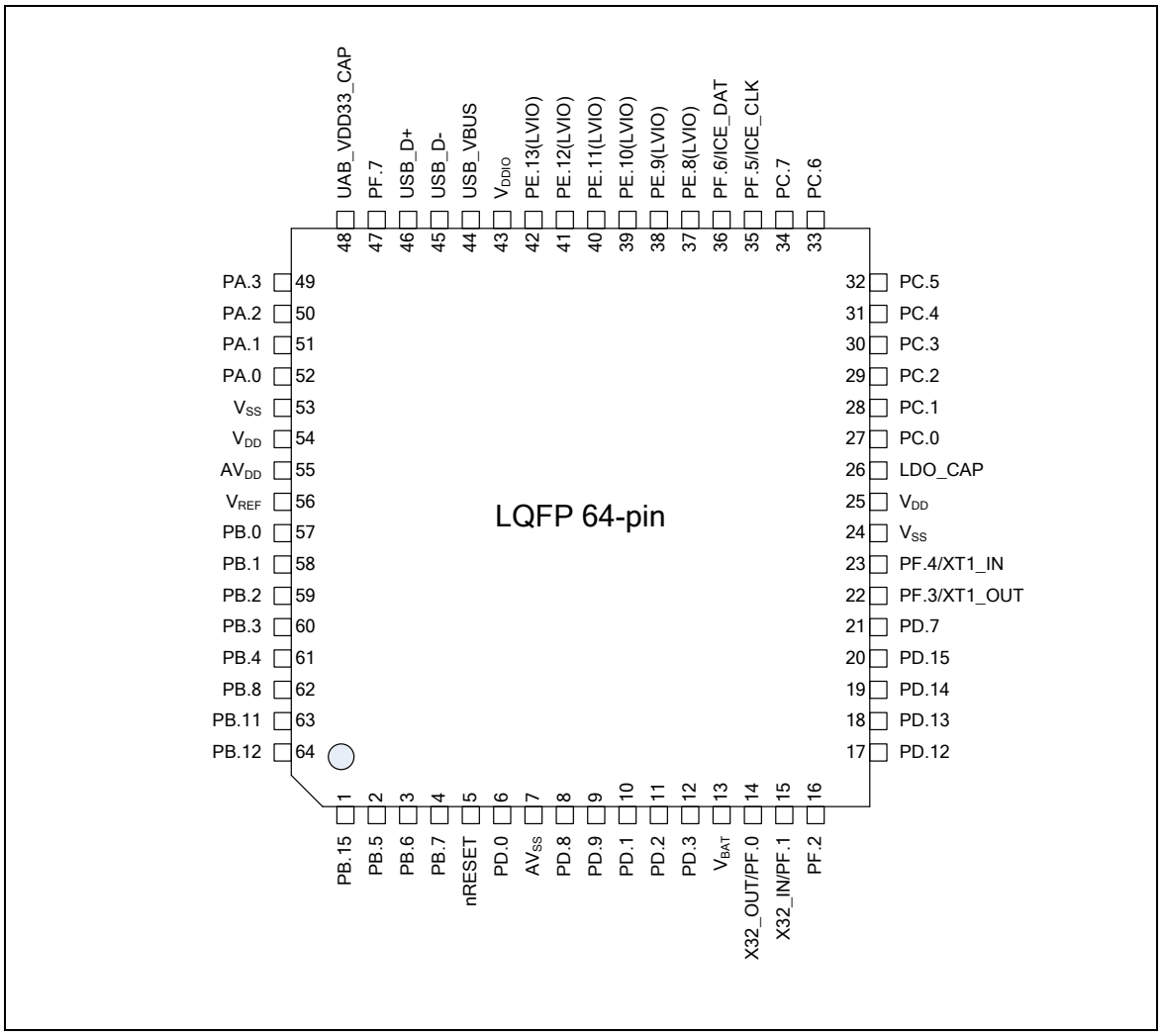


Figure 3.2-9 NuMicro™ M451 USB Series LQFP 64-pin Diagram (M452RD Device Only)

3.2.8 NuMicro™ M453 CAN Series (CAN+USB) LQFP48 Pin Diagram

Corresponding Part Number: M453LG6AE, M453LE6AE

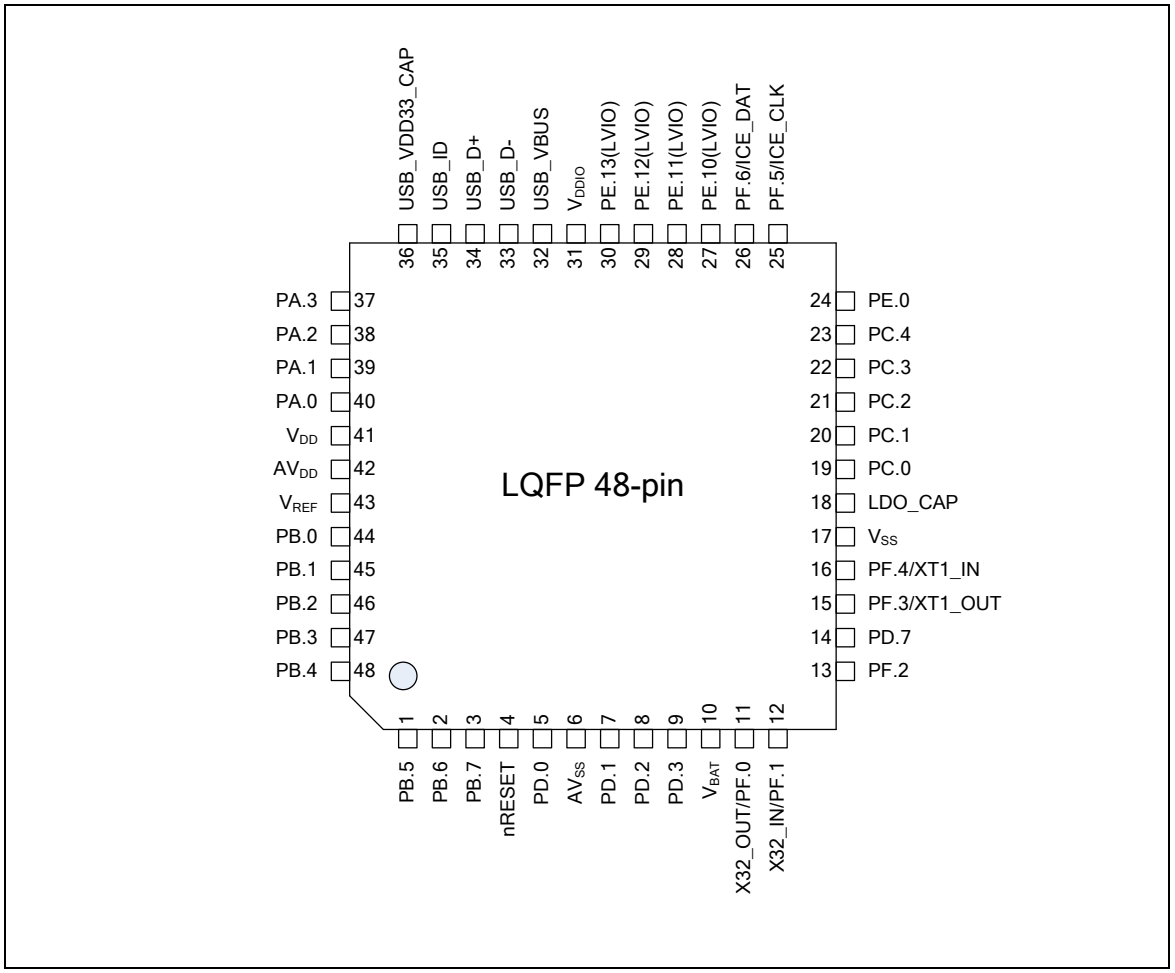


Figure 3.2-10 NuMicro™ M451 CAN Series (CAN+USB) LQFP 48-pin Diagram (M453LG/M453LE Device Only)

Corresponding Part Number: M453LD3AE, M453LC3AE

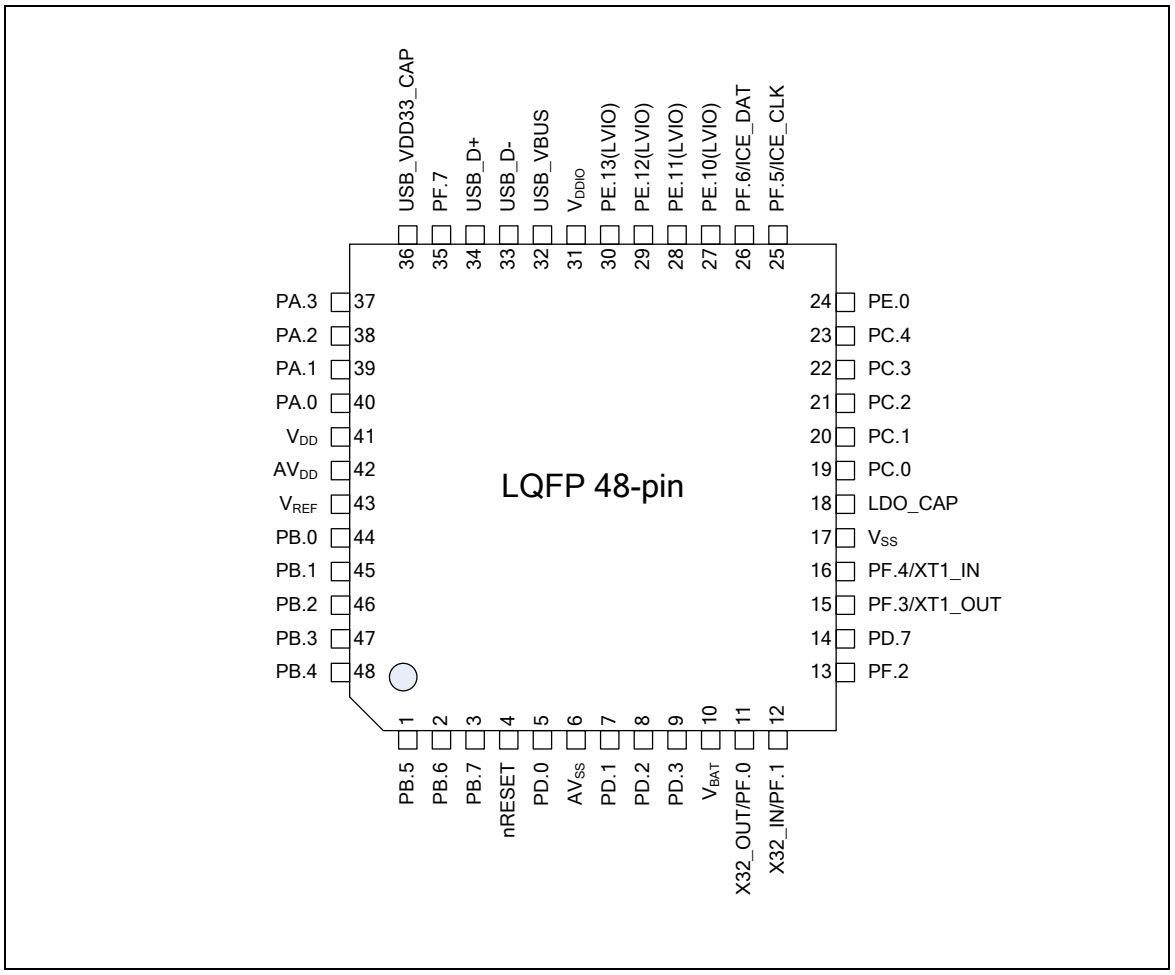


Figure 3.2-11 NuMicro™ M451 CAN Series (CAN+USB) LQFP 48-pin Diagram (M453LD/M453LC Device Only)

3.2.9 NuMicro™ M453 CAN Series (CAN+USB) LQFP64 Pin Diagram

Corresponding Part Number: M453RG6AE, M453RE6AE

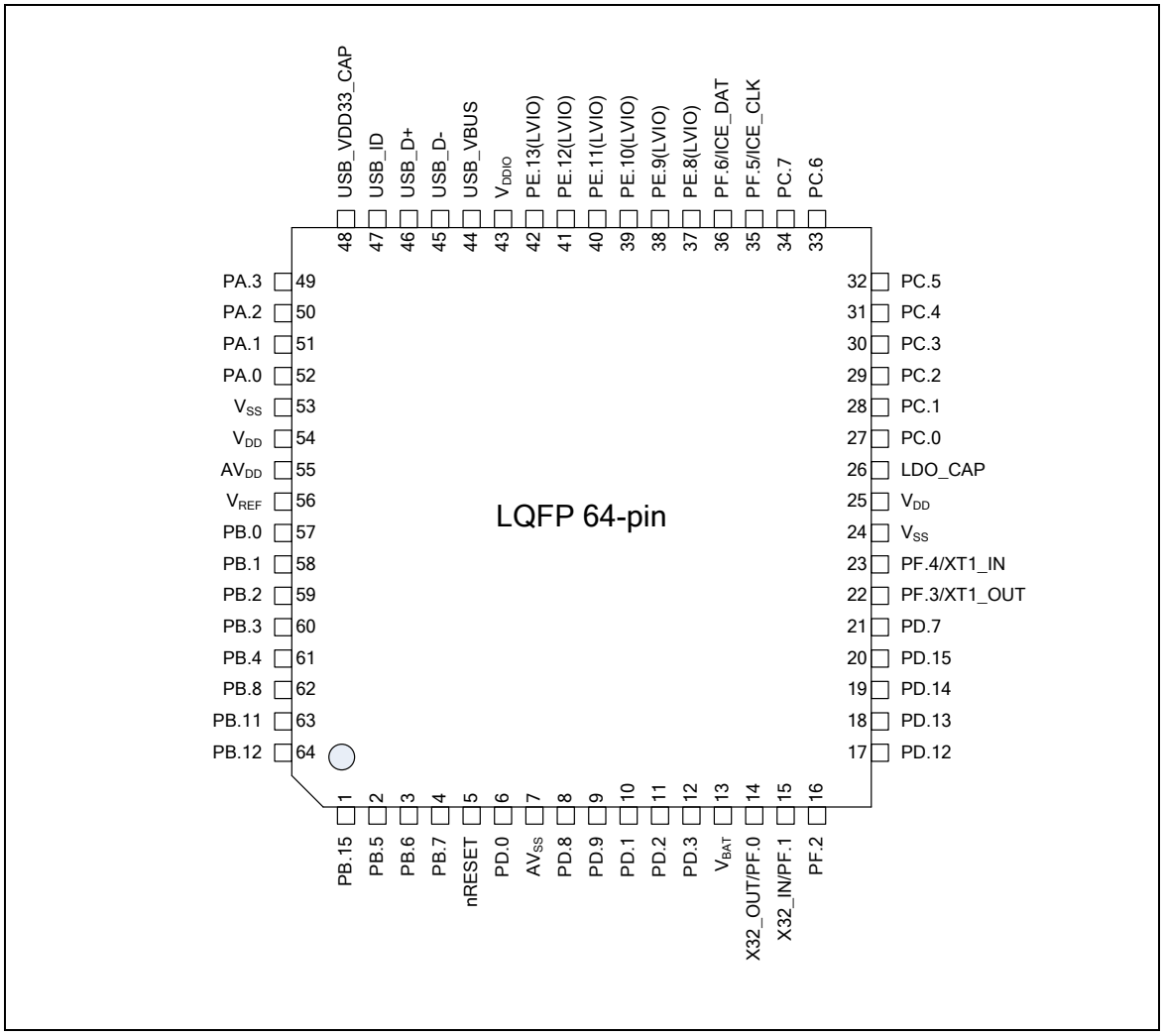


Figure 3.2-12 NuMicro™ M451 CAN Series (CAN+USB) LQFP 64-pin Diagram (M453RG/M453RE Device Only)

Corresponding Part Number: M453RD3AE

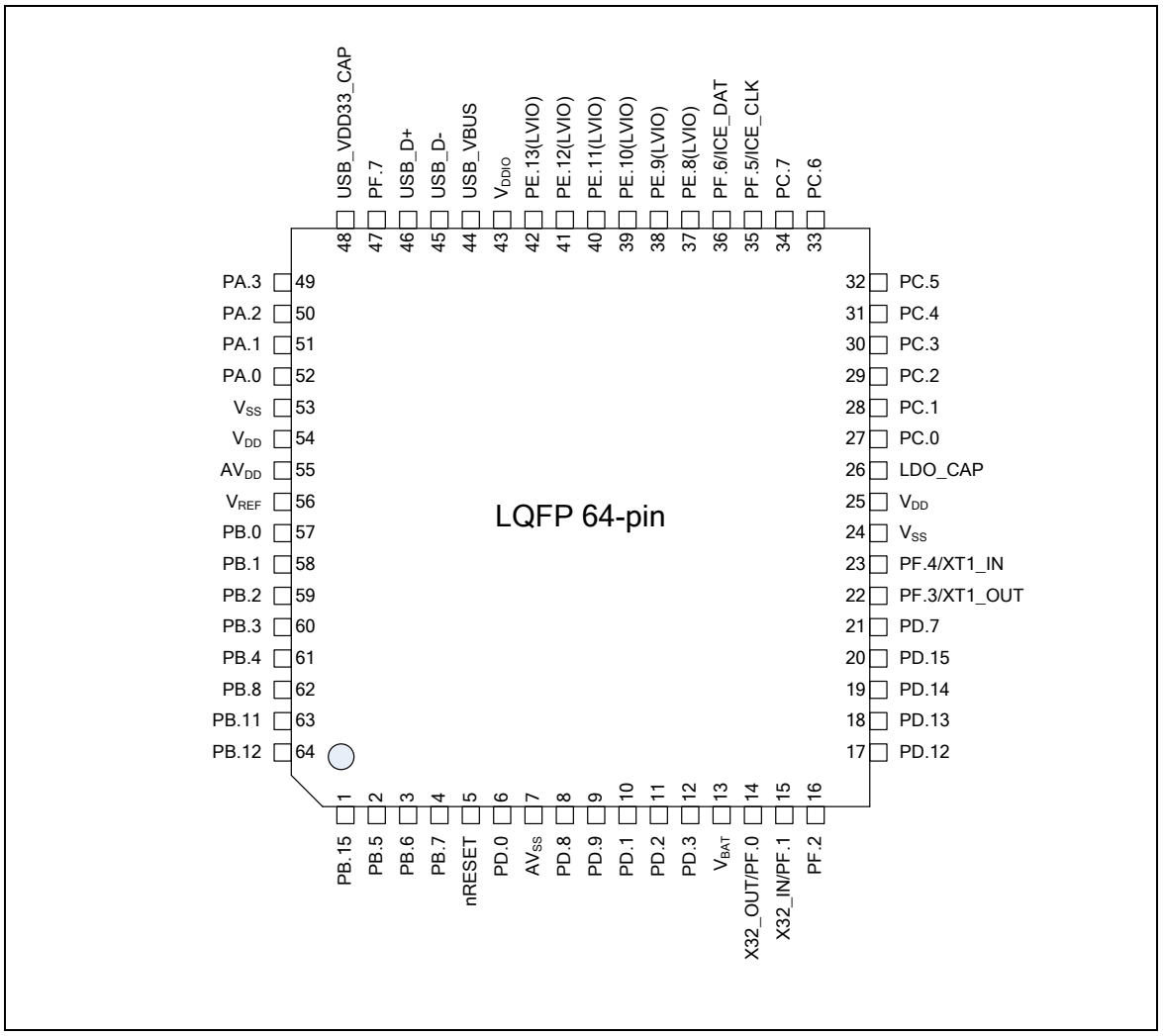


Figure 3.2-13 NuMicro™ M451 CAN Series (CAN+USB) LQFP 64-pin Diagram (M453RD Device Only)

3.2.10 NuMicro™ M453 CAN Series (CAN+USB) LQFP100 Pin Diagram

Corresponding Part Number: M453VG6AE, M453VE6AE

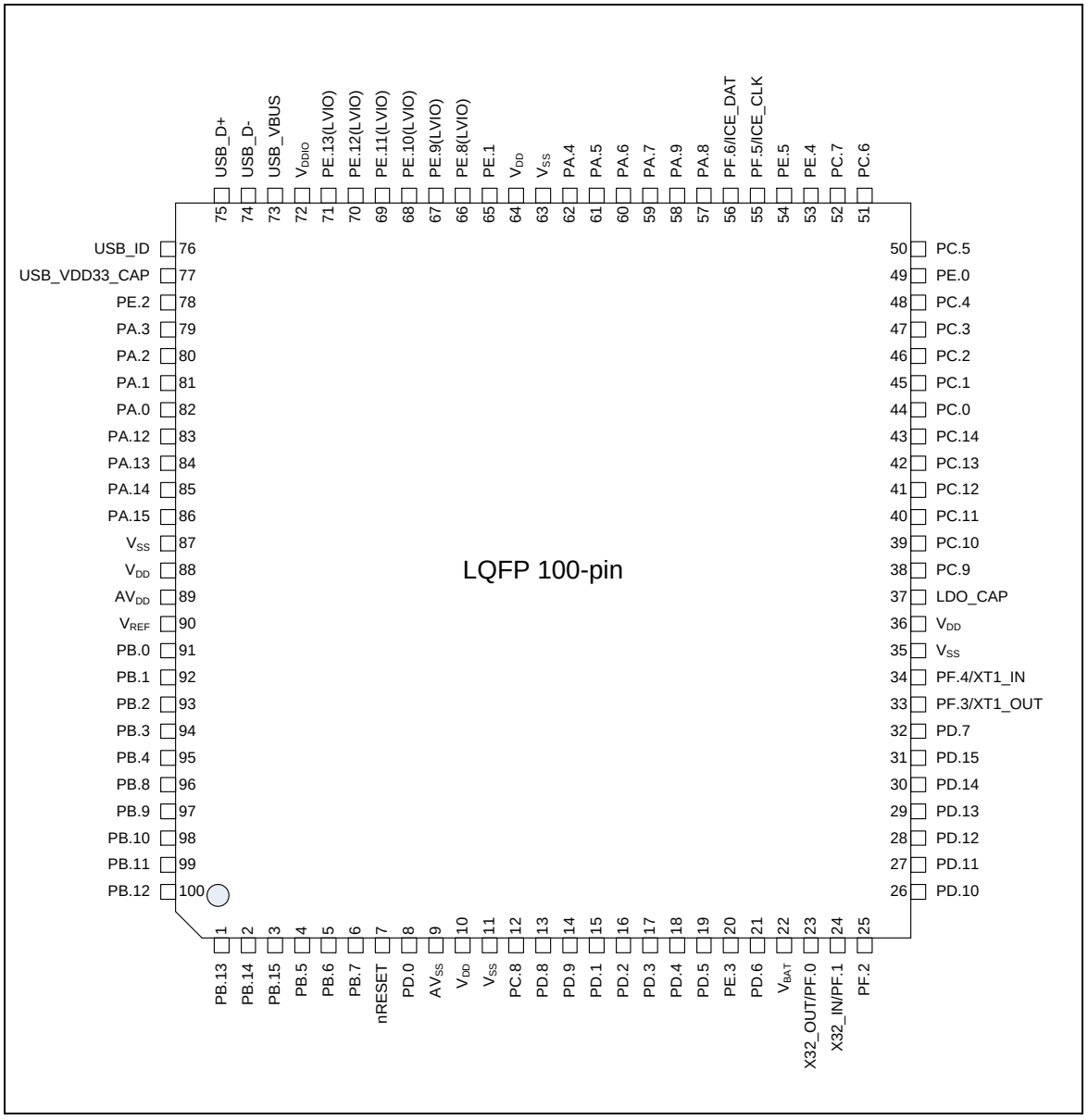


Figure 3.2-14 NuMicro™ M451 CAN Series (CAN+USB) LQFP 100-pin Diagram (M453VG/M453VE Device Only)

Corresponding Part Number: M453VD3AE

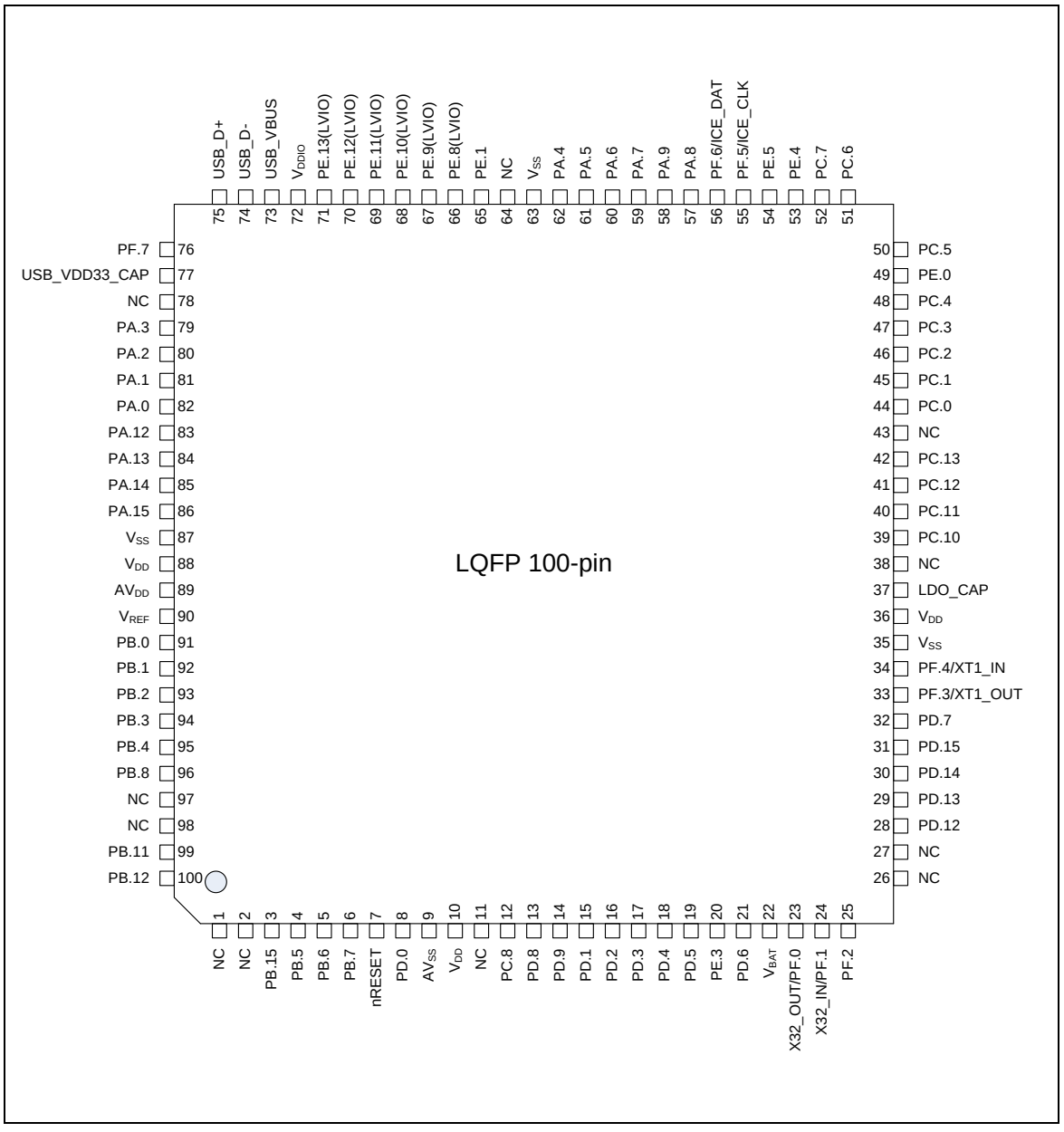


Figure 3.2-15 NuMicro™ M451 CAN Series (CAN+USB) LQFP 100-pin Diagram (M453VD Device Only)

4 BLOCK DIAGRAM

4.1 NuMicro™ M451 Block Diagram

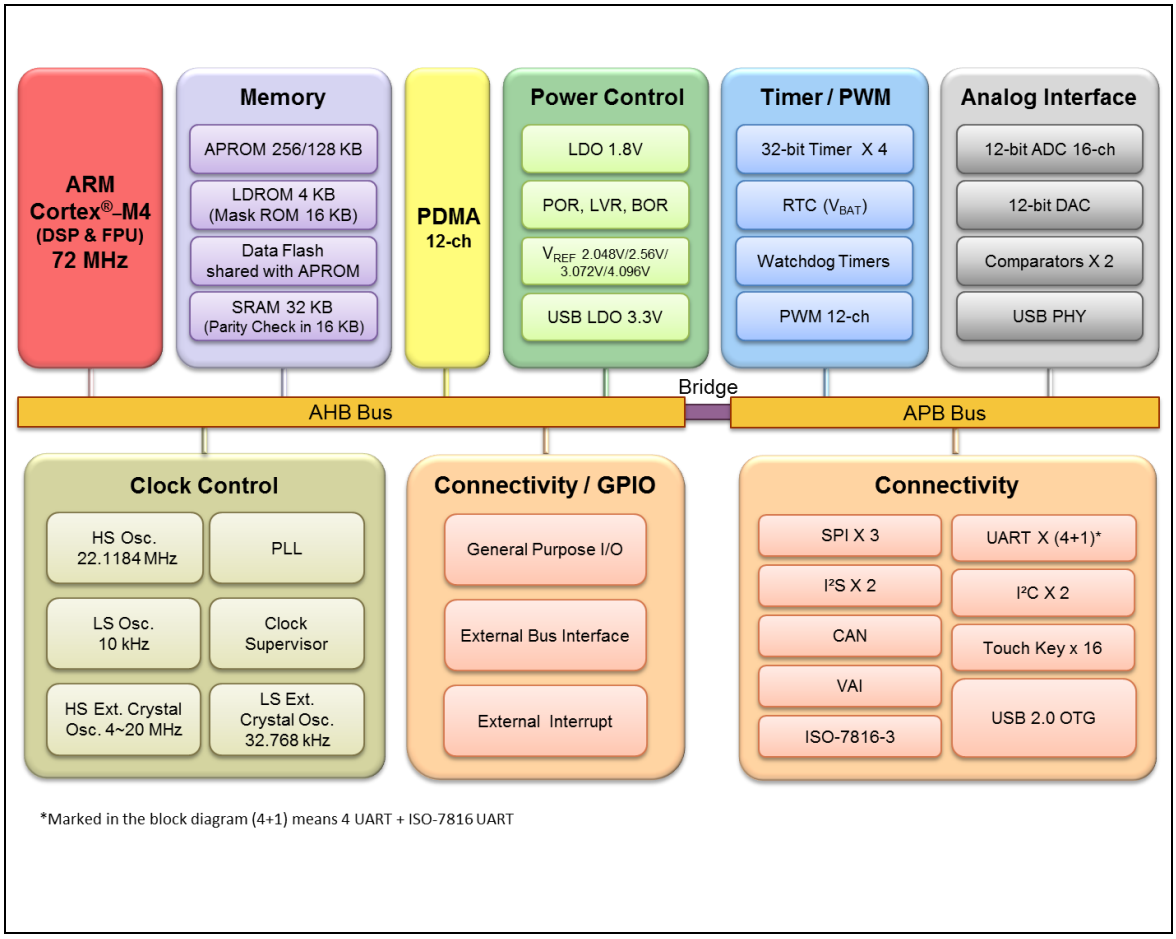


Figure 4.1-1 NuMicro™ M45xG/M45xE Block Diagram

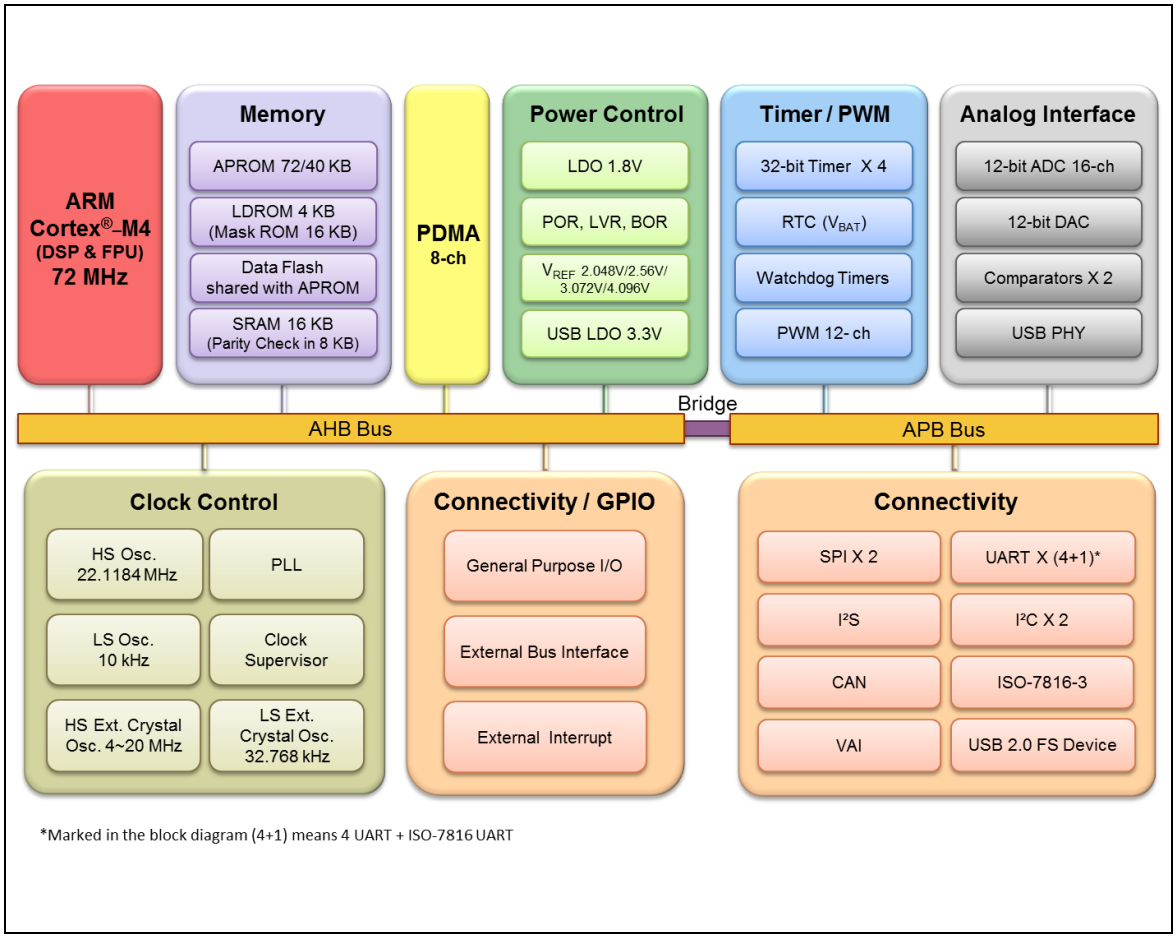
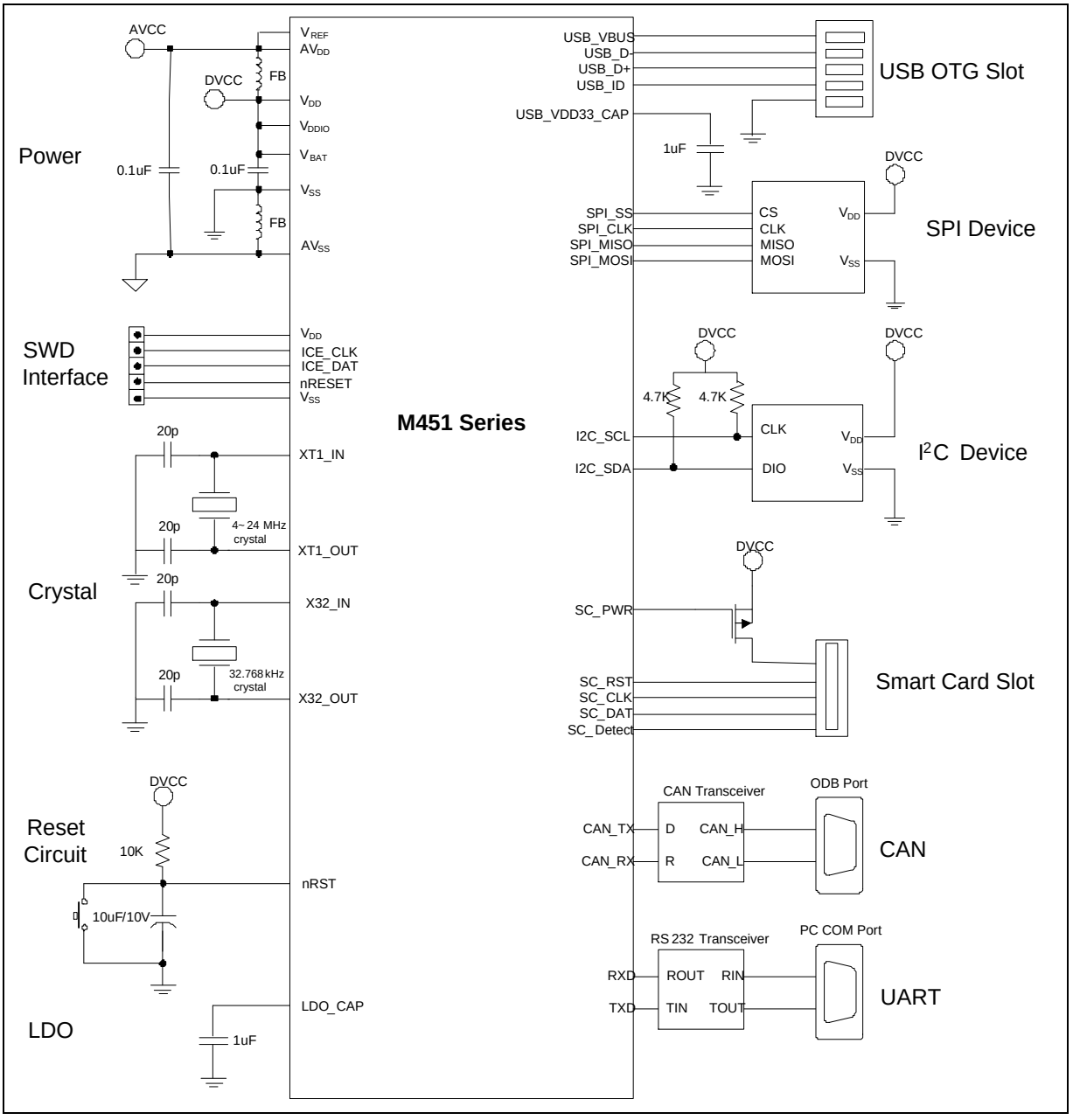


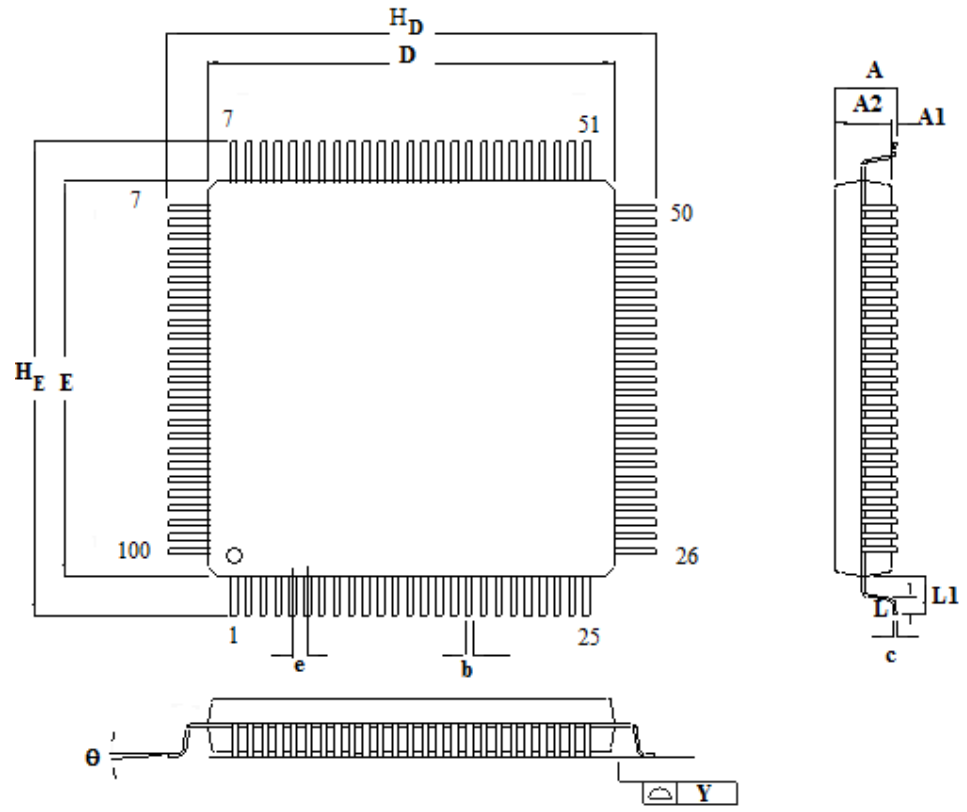
Figure 4.1-2 NuMicro™ M45xD/M45xC Block Diagram

5 APPLICATION CIRCUIT



6 PACKAGE DIMENSIONS

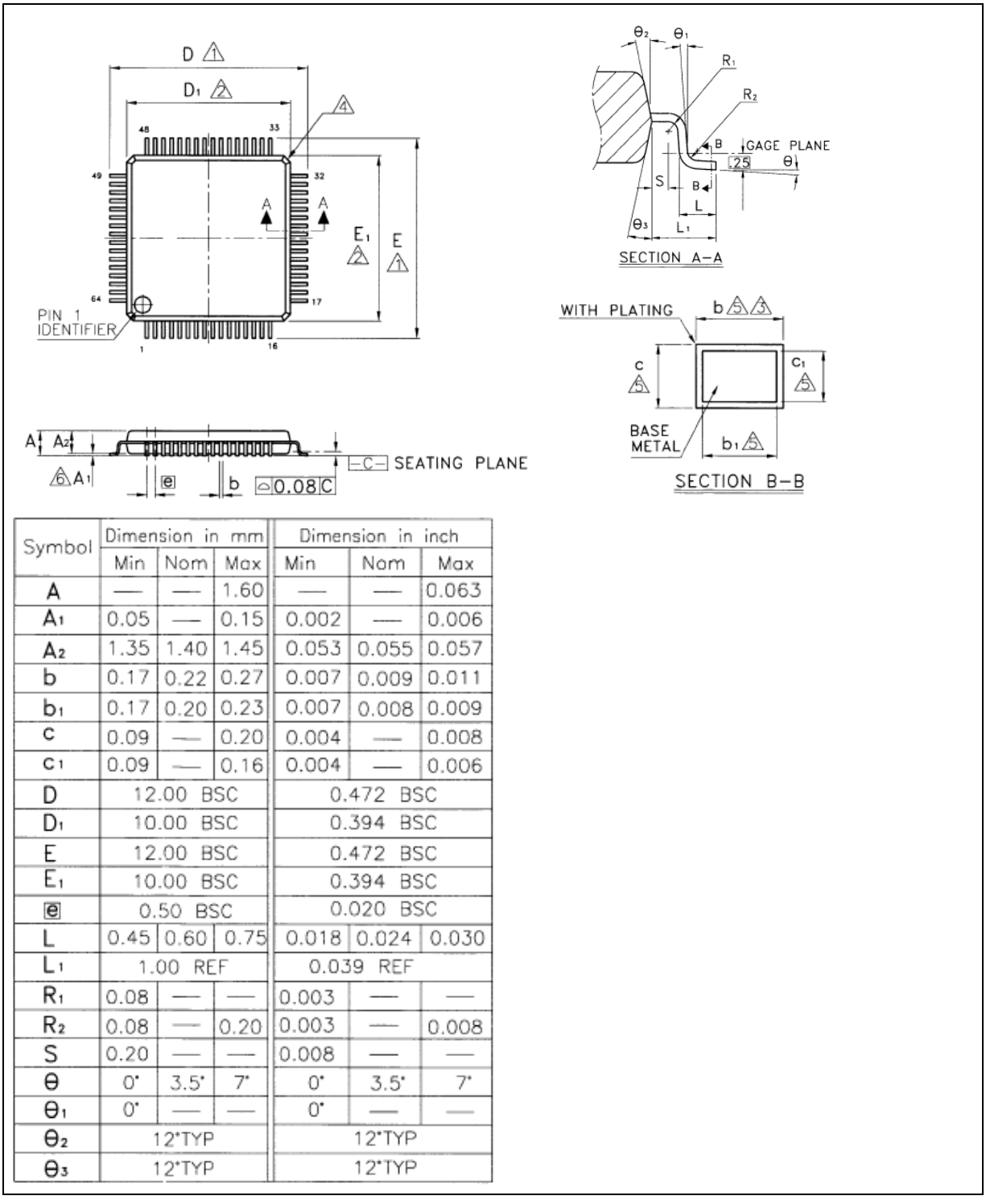
6.1 LQFP 100L (14x14x1.4 mm footprint 2.0 mm)



Controlling Dimension : Millimeters

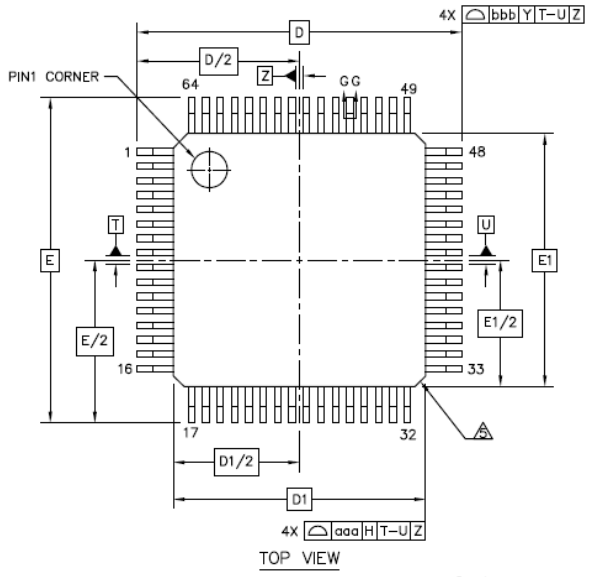
SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	-
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.10	0.15	0.20
D	13.90	14.00	14.10
E	13.90	14.00	14.10
e	-	0.50	-
HD	15.80	16.00	16.20
HE	15.80	16.00	16.20
L	0.45	0.60	0.75
L1	-	1	-
y	-	-	0.10
θ	0°	-	7°

6.2 LQFP 64L (10x10x1.4 mm footprint 2.0 mm)

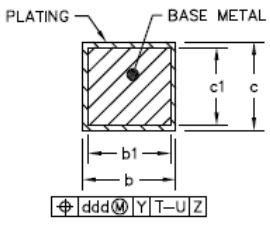


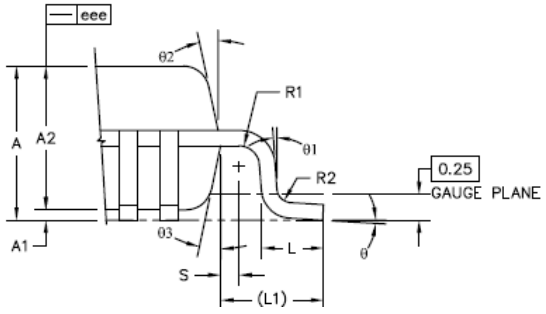
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	12.00 BSC			0.472 BSC		
D_1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E_1	10.00 BSC			0.394 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	12°TYP			12°TYP		
θ_3	12°TYP			12°TYP		

6.3 LQFP 64L (7x7x1.4 mm footprint 2.0 mm)

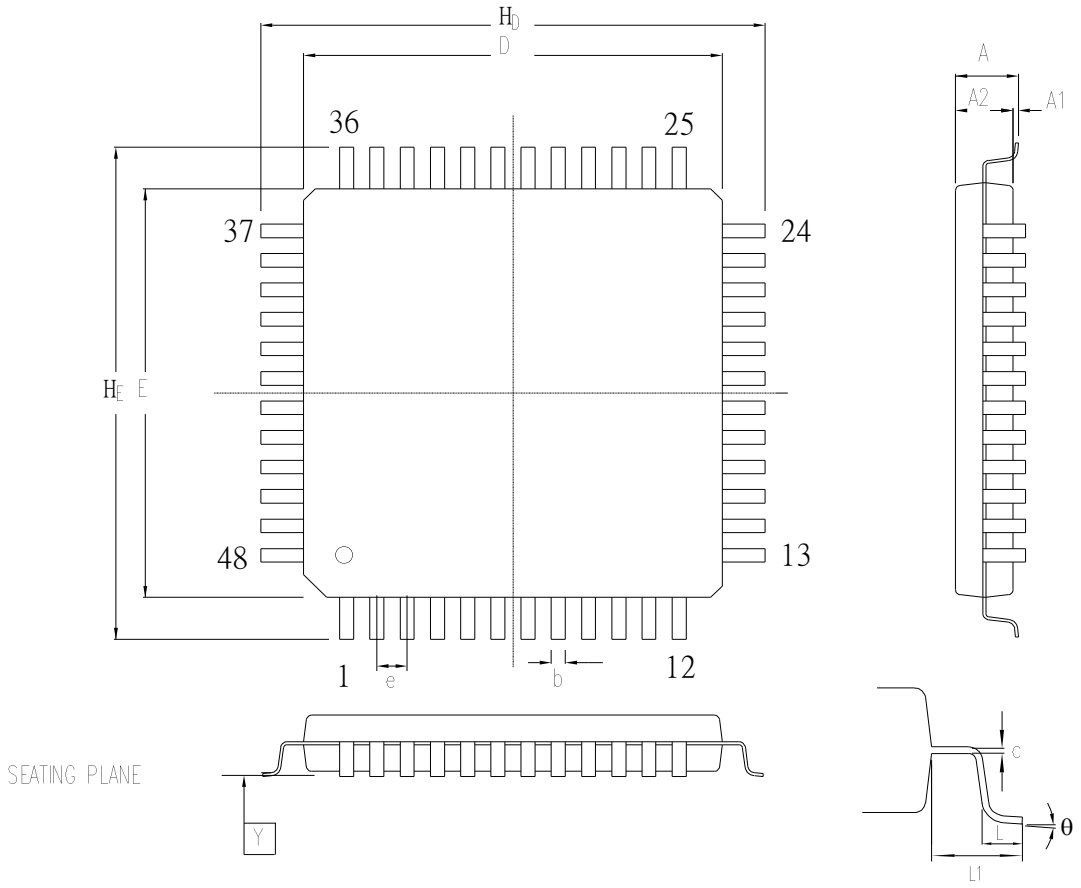


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		





6.4 LQFP 48L (7x7x1.4mm^2 Footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7

7 REVISION HISTORY

Date	Revision	Description
2014.08.22	1.00	Preliminary version.
2015.3.30	1.01	1. Updated document format. 2. Revised maximum clock of HXT from 24 MHz to 20 MHz.. 3. Revised M451 selection guide in section 3.1.
2015.5.11	2.00	1. Added new part number for M45xD/M45xC and the description about the difference with M45xG/M45xE.
2015.5.21	2.01	1. Revised M451 selection guide in section 3.1.

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All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.