PMI

JM38510/13501/13502

ULTRA-LOW OFFSET VOLTAGE OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

T-79-06-10

FEATURES

- Low V_{OS} 25μV
- Low V_{OS} Drift ..... 0.6μV/°C
- Low Noise ..... 0.6μV_{p-p}
- Wide Supply Voltage Range ..... ±4.5V to ±20V

ORDERING INFORMATION

JAN SLASH SHEET	PMI DEVICE
JM38510/13501BGC	OP07AJ1/38510
JM38510/13501BGA	OP07AJ5/38510
JM38510/13501SGA	OP07SAJ5/38510
JM38510/13501BPB	OP07AZ2/38510
JM38510/13501BPA	OP07AZ5/38510
JM38510/13501SPA	OP07SAZ5/38510
JM38510/13502BGC	OP07J1/38510
JM38510/13502BGA	OP07J5/38510
JM38510/13502SGA	OP07SJ5/38510
JM38510/13502BPB	OP07Z2/38510
JM38510/13502BPA	OP07Z5/38510
JM38510/13502SPA	OP07SZ5/38510

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a monolithic, low offset voltage, internally-compensated operational amplifier as specified in MIL-M-38510/135 for device type 01 and 02. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/135 for Class B and Class S processed devices.

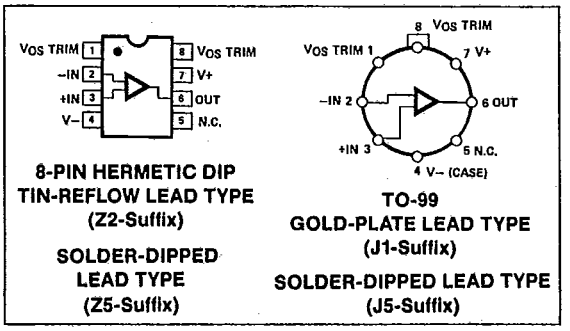
GENERIC CROSS-REFERENCE INFORMATION

This cross-reference information is presented for the convenience of the user. The generic-industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

MILITARY DEVICE TYPE	GENERIC-INDUSTRY TYPE
01	OP07A
02	OP07

For an 883-processed device with improved electrical specifications, review the OP-07 data sheet.

PIN CONNECTIONS



8-PIN HERMETIC DIP
TIN-REFLOW LEAD TYPE
(Z2-Suffix)

SOLDER-DIPPED LEAD TYPE
(Z5-Suffix)

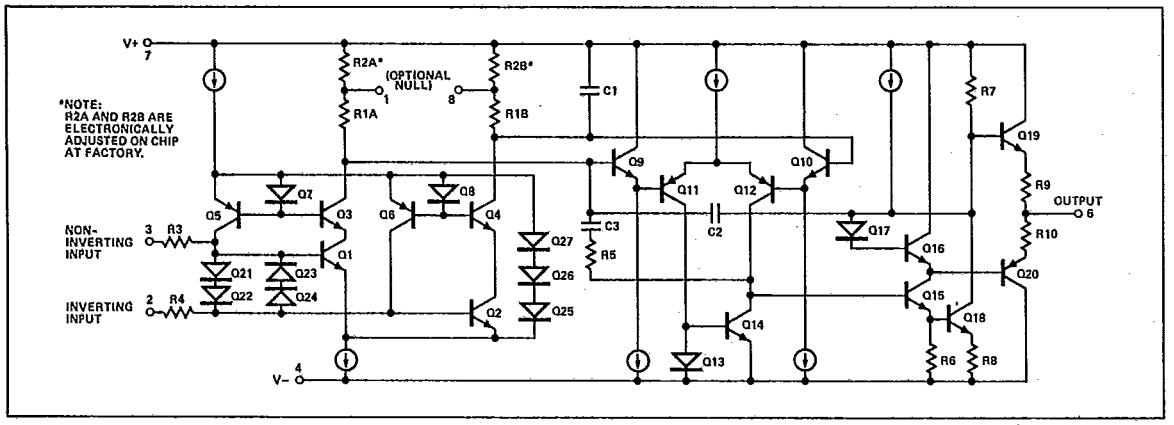
TO-99
GOLD-PLATE LEAD TYPE
(J1-Suffix)

SOLDER-DIPPED LEAD TYPE
(J5-Suffix)

POWER AND THERMAL CHARACTERISTICS

Case Outline	Package	Maximum Allowable Power Dissipation	Maximum θ_{JC}	Maximum θ_{JA}
P	Dual-In-Line	208mW @ T_A = 125°C	50°C/W	120°C/W
G	8-Lead CAN	167mW @ T_A = 125°C	40°C/W	150°C/W

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) ..... ±22V
Input Voltage Range (V_{IN}) ..... $\pm V_{CC}$
Differential Input Voltage Range ..... ±30V
Output Short-Circuit Duration (Note 1)
Lead Temperature (Soldering, 60 sec) ..... +300°C
Storage Temperature Range ..... −65°C to +150°C
Junction Temperature (T_J) ..... +150°C
Maximum Power Dissipation (P_D) (Note 2) 500mW

NOTES:
1. Output may be shorted to ground indefinitely at $V_S = \pm 15V$, $T_A = 25°C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.
2. Maximum power dissipation versus ambient temperature.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... ±4.5V to ±20V
Ambient Temperature Range ..... −55°C to +125°C

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ELECTRICAL CHARACTERISTICS at $\pm 4.5V \le V_{CC} \le \pm 20V$ and $-55°C \le T_A \le 125°C$, $R_S = 50\Omega$ unnulled, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS MIN	01 LIMITS MAX	02 LIMITS MIN	02 LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$T_A = 25°C$ (Notes 1, 2)	−25 −60	25 60	−75 −200	75 200	µV
Input Offset Voltage Temperature Sensitivity	$\Delta V_{IO}/\Delta T$	(Note 1)	−0.6	0.6	−1.3	1.3	µV/°C
Input Bias Current	$+I_{IB}$	$T_A = 25°C$ (Note 1)	−2 −4	2 4	−3 −6	3 6	nA
	$-I_{IB}$	$T_A = 25°C$ (Note 1)	−2 −4	2 4	−3 −6	3 6	
Input Offset Current	I_{IO}	$T_A = 25°C$ (Note 1)	−2 −4	2 4	−2.8 −5.6	2.8 5.6	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC} = 20V$ to 5V, $-V_{CC} = -15V$ $T_A = 25°C$	—	10	—	10	µV/V
	−PSRR	$+V_{CC} = 15V$, $-V_{CC} = -20V$ to −5V $T_A = 25°C$	—	10	—	10	
	+PSRR	$+V_{CC} = 20V$ to 5V, $-V_{CC} = -15V$	—	20	—	20	
	−PSRR	$+V_{CC} = 15V$, $-V_{CC} = -20V$ to −5V	—	20	—	20	
	PSRR	$V_{CC} = \pm 4.5V$ to ±20V $T_A = 25°C$	—	10	—	10	
		$V_{CC} = \pm 4.5V$ to ±20V	—	20	—	20	

NOTES:
1. Tested at $V_{CM} = 0$, $V_{CC} = \pm 15V$.
2. Due to the inherent warm-up drift, testing shall occur no sooner than three (3) minutes after application of power.

ELECTRICAL CHARACTERISTICS at $\pm 4.5V \le V_{CC} \le \pm 20V$ and $-55°C \le T_A \le +125°C$, $R_S = 50\Omega$ unnulled, unless otherwise noted. *Continued*

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PARAMETER	SYMBOL	CONDITIONS	01 LIMITS MIN	01 LIMITS MAX	02 LIMITS MIN	02 LIMITS MAX	UNITS
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$, $T_A = +25°C$, $V_{CC} = \pm 15V$	110	–	110	–	dB
		$V_{CM} = \pm 13C$, $V_{CC} = \pm 15V$	106	–	106	–	
Adjustment for Input Offset	V_{IO} Adj (+)	$T_A = +25°C$ (Note 1)	0.5	–	0.5	–	mV
	V_{IO} Adj (–)	$T_A = +25°C$ (Note 1)	–	0.5	–	0.5	
Output Short-Circuit Current	$I_{OS(+)}$	$t \le 25ms$ (Notes 1, 3) $T_A = +25°C, +125°C$	–65	–	–65	–	mA
		$T_A = -55°C$	–70	–	–70	–	
	$I_{OS(-)}$	$t \le 25ms$ (Notes 1, 3) $T_A = +25°C, +125°C$	–	65	–	65	
		$T_A = -55°C$	–	70	–	70	
Supply Current	I_{CC}	$T_A = +25°C$	–	4	–	4	mA
		(Note 1)	–	5	–	5	
Output Voltage Swing (Minimum)	V_{OP}	$R_L = 1k\Omega$ (Note 1)	–10	10	–10	10	V
		$R_L = 2k\Omega$ (Note 1)	–12	12	–12	12	
Open-Loop Voltage Gain (Single-Ended)	A_{VS}	$T_A = +25°C$	300	–	200	–	V/mV
		(Notes 1, 2)	200	–	150	–	
Slew Rate	SR(+), SR(–)	$V_{IN} = 10V$, $T_A = +25°C$, (Note 1)	0.08	–	0.08	–	V/µs
Input Noise Voltage Density	e_n	$f_O = 10Hz$	–	18	–	18	nV/√Hz
		$f_O = 100Hz$, $T_A = +25°C$ (Note 1)	–	14	–	14	
		$f_O = 1kHz$	–	12	–	12	
Low Frequency Input Noise Voltage	e_{np-p}	$f = 0.1Hz$ to $10Hz$, $T_A = 25°C$, (Note 1)	–	0.6	–	0.6	μV_{p-p}

NOTES:
1. Tested at $V_{CM} = 0$, $V_{CC} = \pm 15V$.
2. $V_{OUT} = 0$ to $+10V$ for $A_{VS(+)}$ and $V_{OUT} = 0$ to $-10V$ for $A_{VS(-)}$, $R_L = 2k\Omega$.
3. Continuous short-circuit limits are considerably less than the indicated test limits, since maximum power dissipation cannot be exceeded.