19-1873; Rev 1; 1/11

MAXIM

8-Bit CODECs

General Description

The MAX1102/MAX1103/MAX1104 CODECs provide both an 8-bit analog-to-digital converter (ADC) and an 8-bit digital-to-analog converter (DAC) with a 4-wire logic interface. The MAX1102/MAX1103 include an onboard +2V/+4V reference, providing a well-regulated, low noise reference for both the ADC and DAC. The MAX1104 offers ratiometric conversion, with the reference internally connected to V_{DD}.

The MAX1102/MAX1103/MAX1104 are low-cost, low-power CODECs for use with microcontrollers (µCs). They allow for greater flexibility when selecting a µC. Less expensive µCs without onboard converters can be used while maintaining overall system performance.

The MAX1102 operates from a single +2.7V to +3.6V supply, the MAX1103 operates from a +4.5V to +5.5V supply, and the MAX1104 operates from a +2.7V to +5.5V supply. The MAX1102/MAX1103 incorporate a V_{DD} monitor in addition to AIN for power supply monitoring. All devices feature a low 18µA standby mode, where both data converters are disabled while the reference remains active, and three shutdown modes: ADC disabled, DAC disabled, and complete shutdown (1µA). A quick 10µs wake-up time allows the MAX1102/MAX1103/MAX1104 to cycle in and out of shutdown even during short-duration idle times.

The MAX1102/MAX1103/MAX1104 are available in a space-saving 8-pin µMAX® package.

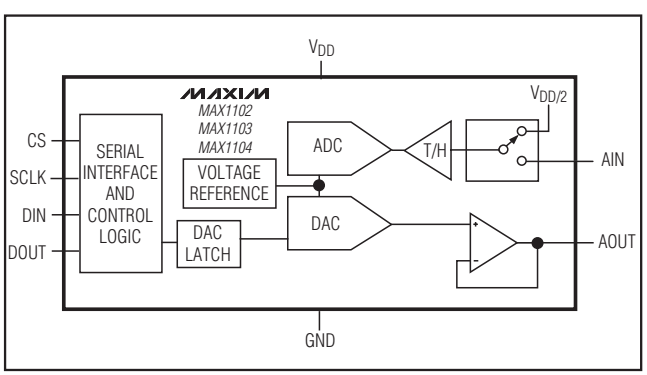
Applications

Analog I/O for Microcontrollers

Analog System Signal Supervision

Voice Recording and Playback

Functional Diagram



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SPI/QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp

Features

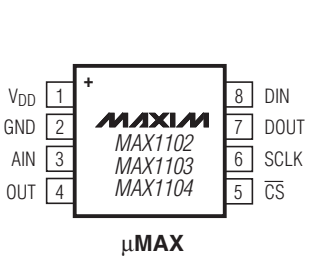
- **8-Bit ADC**
  - **±1LSB INL**
  - **Built-In Track-and-Hold**
  - **48dB of SINAD**
- **8-Bit DAC**
  - **±1LSB INL**
  - **55dB of SFDR**
- **Internal Conversion Clock**
- **Single-Supply Operation**
  - **+2.7V to +3.6V (MAX1102)**
  - **+4.5V to +5.5V (MAX1103)**
  - **+2.7V to +5.5V (MAX1104)**
- **Low Power Consumption**
  - **0.5mA at 25ksps**
  - **1µA Shutdown Mode**
- **6MHz 4-Wire SPI™, QSPI™, and MICROWIRE™ Compatible Interface**
- **Compact 8-Pin µMAX Package**
- **Internal Voltage Reference**
  - **+2V: MAX1102**
  - **+4V: MAX1103**
- **Power-Supply Monitor (MAX1102/MAX1103)**
- **Rail-to-rail DAC Output Buffer**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	REFERENCE
MAX1102EUA+	-40°C to +85°C	8 µMAX	+2V
MAX1103EUA+	-40°C to +85°C	8 µMAX	+4V
MAX1104EUA+	-40°C to +85°C	8 µMAX	V_{DD}

+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
AIN, OUT, $\overline{DOUT}$ to GND .....-0.3V to (V_{DD} + 0.3V)
DIN, SCLK, $\overline{CS}$ to GND .....-0.3V to +6V
Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 4.1mW/°C above +70°C) 330mW
Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering,10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V (MAX1102), V_{DD} = +4.5V to +5.5V (MAX1103), V_{DD} = +2.7V to +5.5V (MAX1104), f_{SCLK} = 6.0MHz (50% duty cycle), R_{OUT} = 10kΩ, C_{OUT} = 100pF, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC DC ACCURACY (Note 1)						
Resolution			8			Bits
Relative Accuracy (Note 2)	INL	All codes		±1/4	±1	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic		±1/4	±1	LSB
Offset Error					±1	LSB
Gain Error (Note 3)		MAX1102/MAX1103			±5	%
		MAX1104			±1	LSB
ADC DYNAMIC SPECIFICATIONS (f_{AIN} = 10kHz SINE WAVE. V_{AIN} = 0.9 × V_{REFp-p})						
Signal to Noise and Distortion Ratio	SINAD			48		dB
Spurious-Free Dynamic Range	SFDR			59		dB
Total Harmonic Distortion	THD			58		dB
Full-Power Bandwidth				2.5		MHz
ADC Wake-Up Time from Standby		Reference enabled (MAX1102/MAX1103)		3		µs
ADC Wake-Up Time from Full Shutdown		MAX1102/MAX11103			200	µs
		MAX1104		3		
ANALOG INPUT						
Analog Input Voltage	V_{AIN}		0		V_{REF}	V
Input Resistance	R_{IN}			10		MΩ
Input Capacitance	C_{IN}			20		pF
VOLTAGE REFERENCE						
Reference Voltage	V_{REF}	MAX1102		2		V
		MAX1103		4		
Temperature Coefficient		MAX1102/MAX1103		100		ppm/°C
CONVERSION RATE						
Conversion Time	t_{CONV}			24	36	µs
Track/Hold Acquisition Time	t_{ACQ}				3.5	µs
Internal Clock Frequency				375		kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V (MAX1102), V_{DD} = +4.5V to +5.5V (MAX1103), V_{DD} = +2.7V to +5.5V (MAX1104), f_{SCLK} = 6.0MHz (50% duty cycle), R_{OUT} = 10kΩ, C_{OUT} = 100pF, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Throughput Rate		ADC in continuous conversion mode	25			ksps
DAC DC ACCURACY						
Resolution			8			Bits
Relative Accuracy (Note 2)	INL			±1/4	±1	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic		±1/4	±1	LSB
Offset Error					±30	mV
Gain Error (Note 3)		MAX1102/MAX1103			±5	%
		MAX1104			±30	mV
DAC DYNAMIC SPECIFICATIONS (f_{OUT} = 1kHz SINE WAVE, V_{OUT} = 0.9 × V_{REFp-p})						
Spurious-Free Dynamic Range	SFDR			55		dB
Total Harmonic Distortion	THD			53		dB
Small-Signal Bandwidth				1		MHz
Full-Power Bandwidth				72		kHz
DAC Wake-Up Time from Standby (Note 4)		Reference enabled (MAX1102/MAX1103)		10		µs
DAC Wake-Up Time from Full Shutdown (Note 4)		MAX1102/MAX1103			200	µs
		MAX1104		10		
DAC OUTPUT						
Full-Scale Swing		MAX1104	0		V_{DD} - 0.1	V
Settling Time (Note 5)		Settle to within ±1/2 LSB		11		µs
Slew Rate				1.2		Vµs
Load Regulation		R_L open to 10kΩ 0 < V_{OUT} < V_{DD} - 0.1V		0.05		LSB
LOGIC INPUTS AND OUTPUTS (DIN, SLCK, $\overline{CS}$)						
Input High Voltage	V_{IH}		V_{DD} x 0.7			V
Input Low Voltage	V_{IL}				V_{DD} x 0.3	V
Input Current		V_{LOGIC} = V_{GND} or V_{DD}		±0.1	±5	µA
Digital Input Hysteresis				0.5		V
Digital Input Capacitance				15		pF
Output High Voltage	V_{OH}	I_{SOURCE} = 1.0mA	V_{DD} x 0.9			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.0mA			V_{DD} x 0.1	V
Three-State Leakage	I_{LEAK}				±5.0	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V (MAX1102), V_{DD} = +4.5V to +5.5V (MAX1103), V_{DD} = +2.7V to +5.5V (MAX1104), f_{SCLK} = 6.0MHz (50% duty cycle), R_{OUT} = 10kΩ, C_{OUT} = 100pF, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS						
Supply Voltage	V_{DD}	MAX1102	2.7		3.6	V
		MAX1103	4.5		5.5	
		MAX1104	2.7		5.5	
Supply Current	I_{CC}	ADC on (25ksps), DAC off		0.25	0.5	mA
		ADC off, DAC on (V_{DD} = +5.5V)		0.4	0.66	
Standby Current		ADC off, DAC off, clock off, reference on		18	35	µA
Full Shutdown Current		ADC off, DAC off, clock off		1		µA

TIMING CHARACTERISTICS (Figures 4a and 4b)

(V_{DD} = +2.7V to +3.6V (MAX1102), V_{DD} = +4.5V to +5.5V (MAX1103), V_{DD} = +2.7V to +5.5V (MAX1104), f_{SCLK} = 6.0MHz (50% duty cycle), R_{OUT} = 10kΩ, C_{OUT} = 100pF, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Up to Reset Complete	t9			40		µs
$\overline{CS}$ Rise-to-DOUT = High-Z	t10				40	ns
$\overline{CS}$ Fall-to-DOUT Valid	t11	R_{DOUT} = 3kΩ, C_{DOUT} = 50pF			60	ns
$\overline{CS}$ Fall-to-SCLK Rise	t3		15			ns
SCLK Fall-to-$\overline{CS}$ Rise	t8		25			ns
DIN-to-SCLK Setup Time	t4		10			ns
DIN-to-SCLK Hold Time	t5		15			ns
SCLK Fall to DOUT Valid	t6	R_{DOUT} = 3kΩ, C_{DOUT} = 50pF			78	ns
SCLK Maximum Frequency	f_{SCLK}				6	MHz
SCLK Pulse Width High	t_{CH}		60			ns
SCLK Pulse Width Low	t_{CL}		70			ns

Note 1: MAX1102/MAX1104 tested with V_{DD} = +3V. MAX1103 tested with V_{DD} = +5V.

Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the gain error and offset error have been nulled.

Note 3: Gain error calculation is referenced to the ideal FS output. Gain error for the MAX1102/MAX1103 also includes reference initial accuracy error.

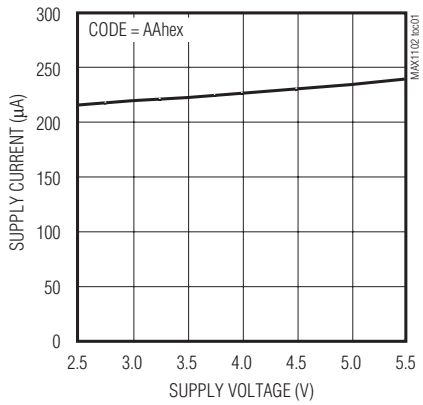
Note 4: Wake-up time is the time it takes for the DAC output to settle to within ±1/2 LSB of the FS value after a power-up command.

Note 5: Output settling time is measured by taking the DAC from code 00hex to FFhex.

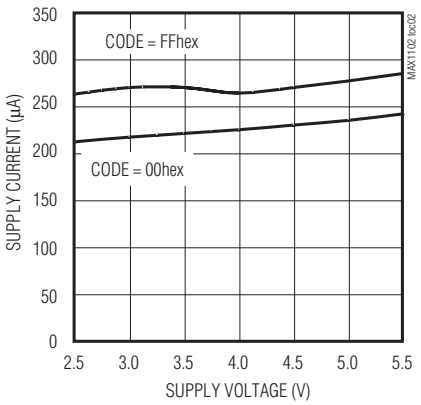
Typical Operating Characteristics

(V_{DD} = +3.0V (MAX1102), V_{DD} = +5V (MAX1103), f_{SCLK} = 6.0MHz (50% duty cycle), R_{OUT} = 10kΩ, C_{OUT} = 100pF, T_A = +25°C, unless otherwise noted.)

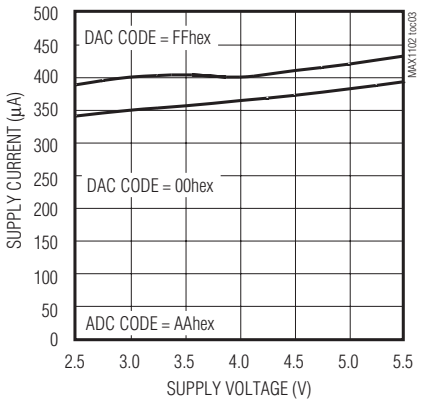
SUPPLY CURRENT vs. SUPPLY VOLTAGE (ADC ENABLED, DAC DISABLED)



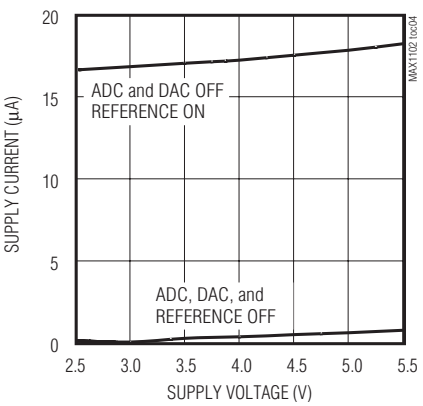
SUPPLY CURRENT vs. SUPPLY VOLTAGE (DAC ENABLED, ADC DISABLED)



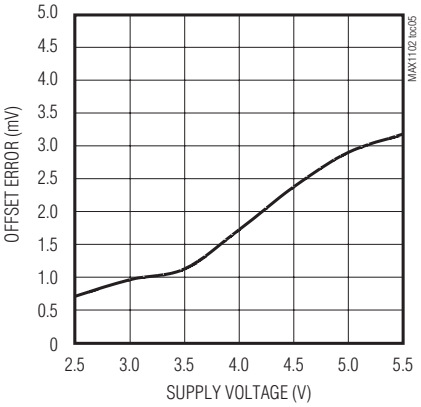
SUPPLY CURRENT vs. SUPPLY VOLTAGE (ADC ENABLED, DAC ENABLED)



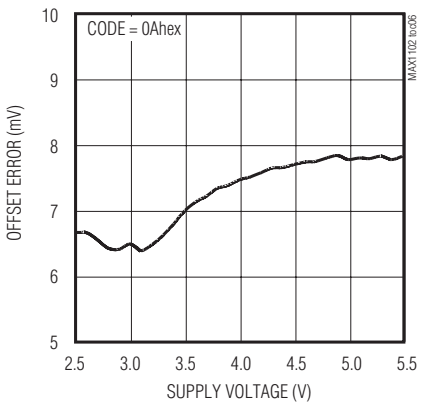
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



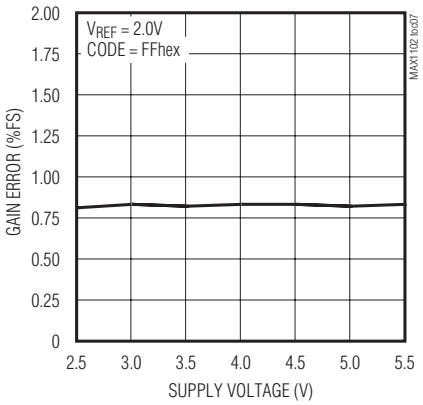
ADC OFFSET ERROR vs. SUPPLY VOLTAGE



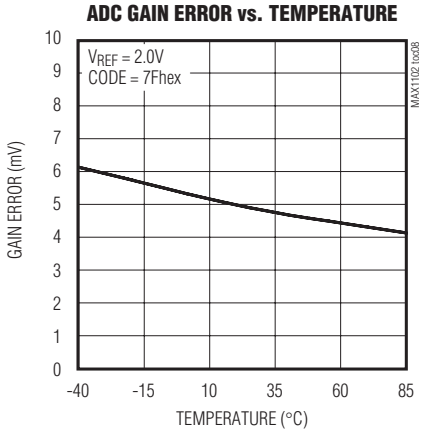
DAC OFFSET ERROR vs. SUPPLY VOLTAGE



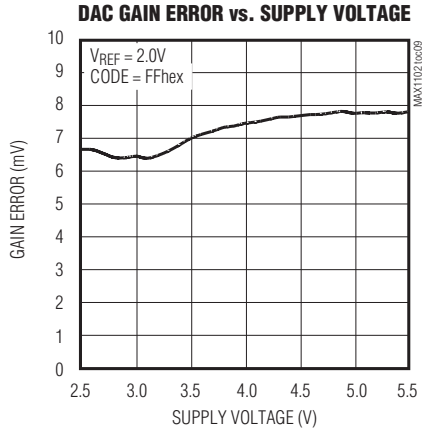
ADC GAIN ERROR vs. SUPPLY VOLTAGE



ADC GAIN ERROR vs. TEMPERATURE



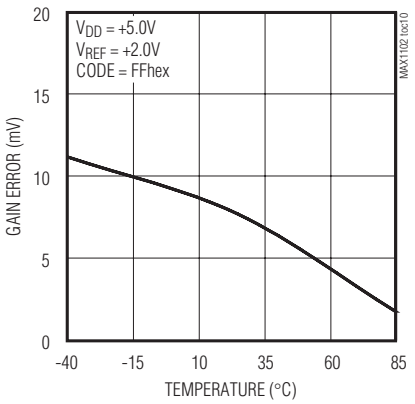
DAC GAIN ERROR vs. SUPPLY VOLTAGE



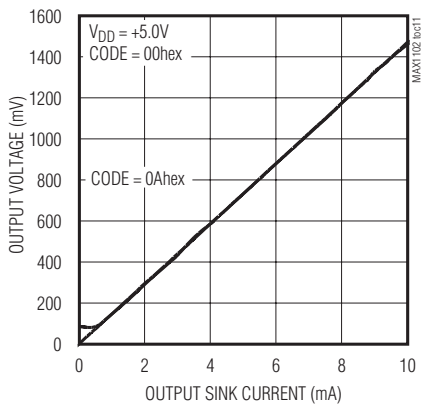
Typical Operating Characteristics (continued)

(V_{DD} = +3.0V (MAX1102), V_{DD} = +5V (MAX1103), f_{SCLK} = 6.0MHz (50% duty cycle), R_{OUT} = 10kΩ, C_{OUT} = 100pF, T_A = +25°C, unless otherwise noted.)

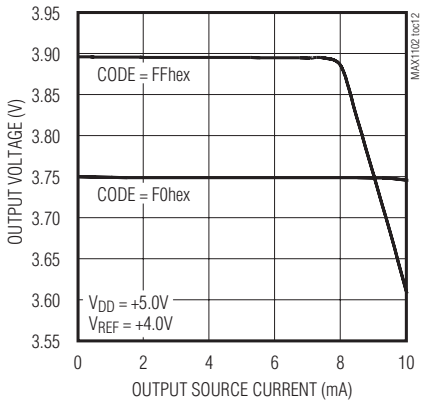
DAC GAIN ERROR vs. TEMPERATURE



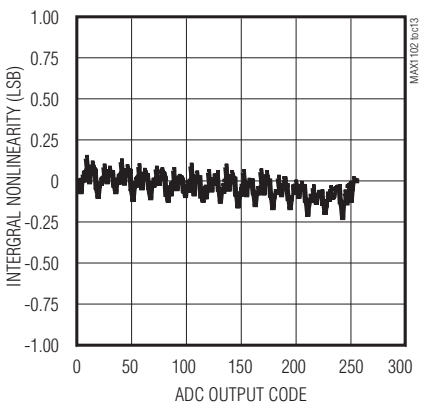
DAC OUTPUT LOW VOLTAGE vs. OUTPUT SINK CURRENT



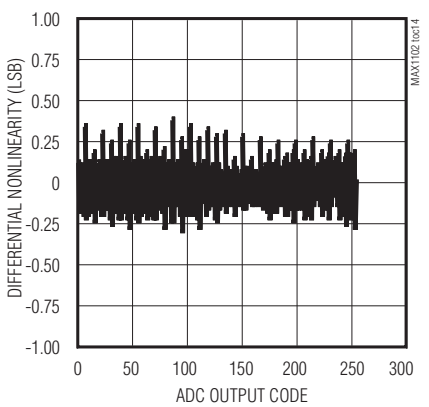
DAC OUTPUT HIGH VOLTAGE vs. OUTPUT SOURCE CURRENT



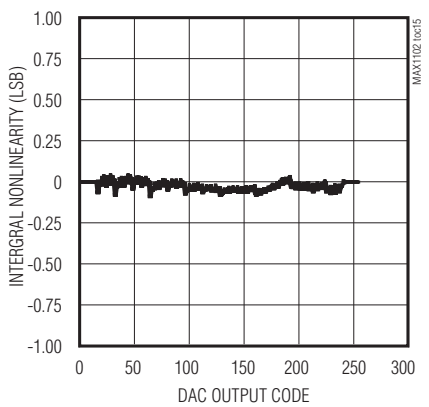
ADC INTEGRAL NONLINEARITY vs. CODE



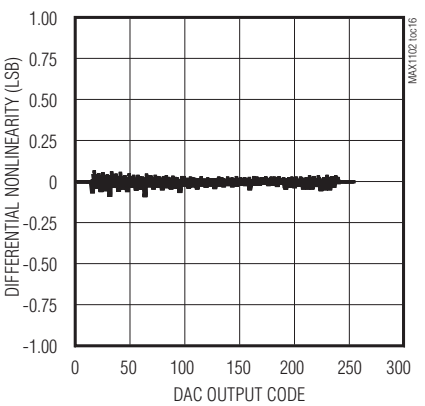
ADC DIFFERENTIAL NONLINEARITY vs. CODE



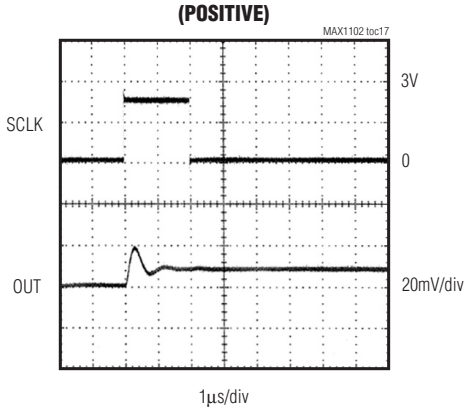
DAC INTEGRAL NONLINEARITY vs. CODE



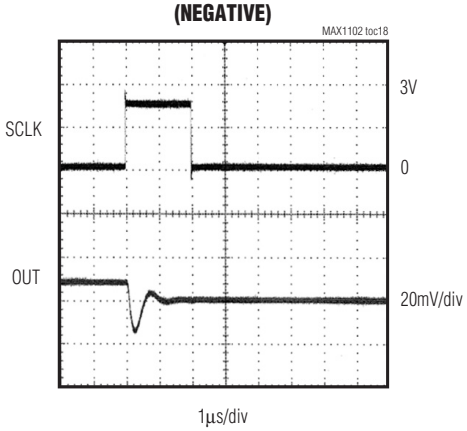
DAC DIFFERENTIAL NONLINEARITY vs. CODE



WORST-CASE 1LSB DIGITAL STEP CHANGE (POSITIVE)



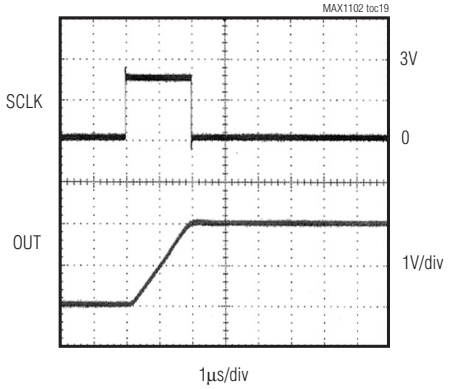
WORST-CASE 1LSB DIGITAL STEP CHANGE (NEGATIVE)



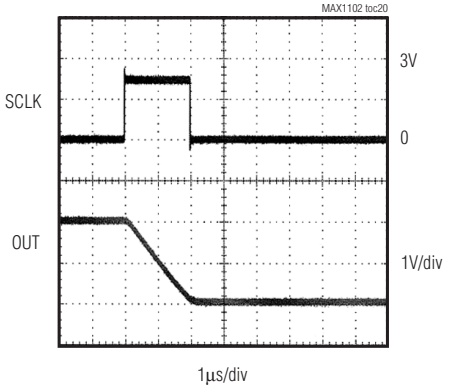
Typical Operating Characteristics (continued)

(V_{DD} = +3.0V (MAX1102), V_{DD} = +5V (MAX1103), f_{SCLK} = 6.0MHz (50% duty cycle), R_{OUT} = 10kΩ, C_{OUT} = 100pF, T_A = +25°C, unless otherwise noted.)

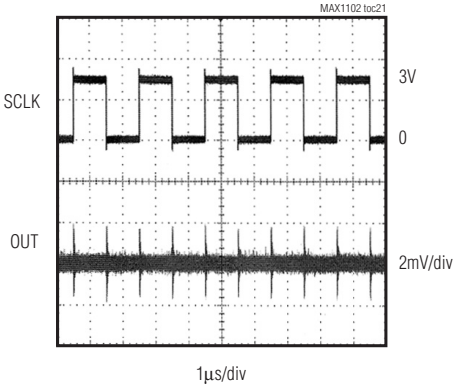
POSITIVE SETTLING TIME



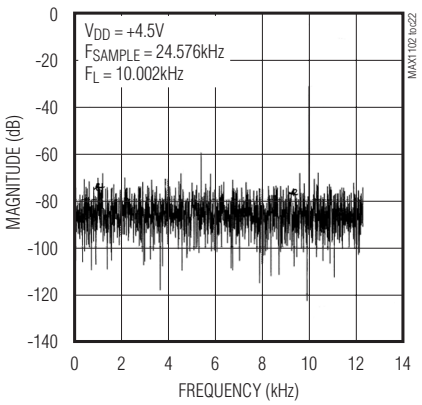
NEGATIVE SETTLING TIME



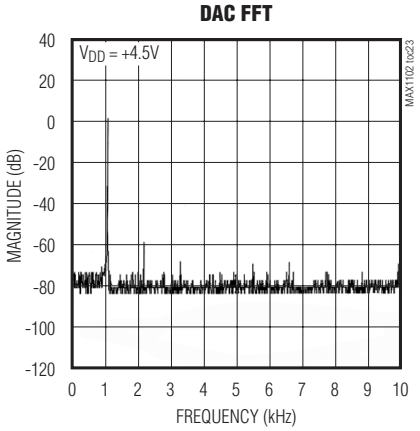
CLOCK FEEDTHROUGH



ADC FFT



DAC FFT



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Voltage Supply
2	GND	Ground
3	AIN	ADC Analog Input
4	OUT	DAC Analog Voltage Output
5	$\overline{CS}$	Chip Select Input. Device ignores all logic signals when $\overline{CS}$ is high.
6	SCLK	Serial Clock Input. Data in is latched on the rising edge, data out transitions on the falling edge.
7	DOUT	ADC Digital Output. Output is high impedance when $\overline{CS}$ is high.
8	DIN	DAC Digital Input. Input ignores all signals when $\overline{CS}$ is high.

Detailed Description

The MAX1102/MAX1103/MAX1104 are 8-bit CODECs in a compact 8-pin package. These devices consist of an 8-bit ADC, an 8-bit DAC, track/hold (T/H), DAC output buffer amplifier, internal voltage reference, input multiplexer (mux) and a 6MHz SPI, QSPI and MICROWIRE compatible 4-wire serial interface. A single 8-bit word configures the MAX1102/MAX1103/MAX1104, providing a simple interface to a microcontroller (µC).

Analog-to-Digital Converter

The MAX1102/MAX1103/MAX1104 ADC section uses a successive-approximation (SAR) conversion technique and input T/H circuitry to convert an analog signal to an 8-bit digital output. No external hold capacitors are required. The MAX1102/MAX1103 have an input multiplexer that directs either AIN or $V_{DD}/2$ to the input of the T/H, allowing these devices to either convert the analog input, or monitor the power supply. Figure 1 shows the detailed functional diagram of the ADC block.

ADC Operation

The input architecture of the ADC is illustrated in Figure 2, the equivalent input circuit, and is composed of the T/H, input mux (MAX1102/MAX1103), input comparator, switched capacitor DAC, and the auto-zero rail. The switched capacitor DAC is independent of the R-2R ladder DAC and does not provide the converted analog output on OUT.

The T/H is in hold mode while a conversion is taking place. Once the conversion is completed, the T/H enters acquisition mode, and tracks the input signal until the start of the next conversion. In single conversion mode, conversion starts at the falling clock edge corresponding to the last bit of the control word. In continuous conversion mode, the first conversion following the control word starts on the falling clock edge of the

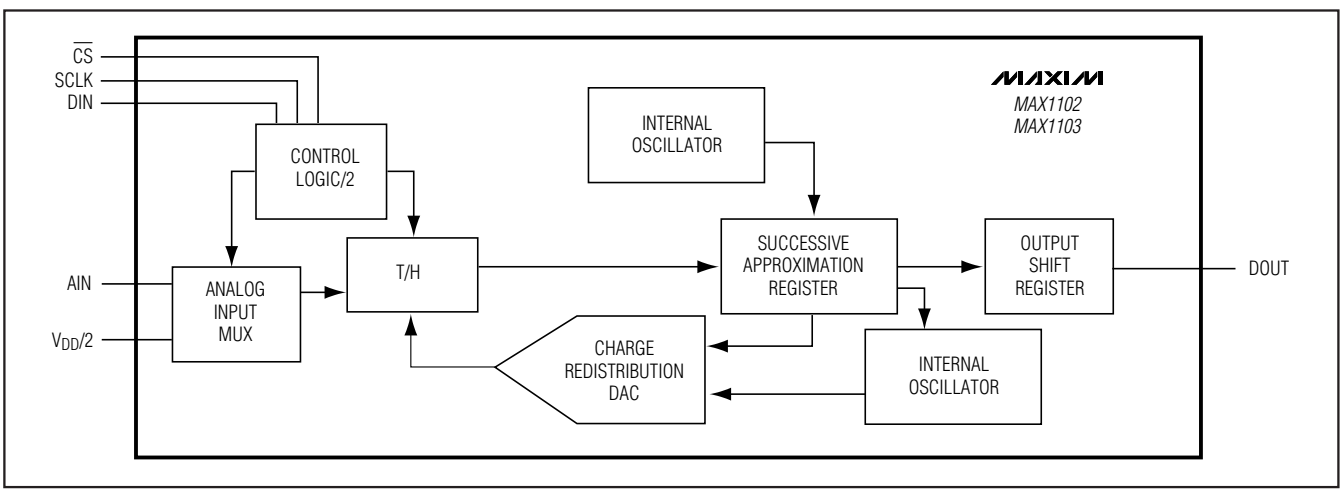


Figure 1. ADC Detailed Functional Diagram

LSB of the control word. Successive conversions are initiated after the last bit of the previous conversion result has been clocked out. Resultant data is only available after conversion is complete.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. This time, t_{ACQ2}, is calculated by the following equation:

$$t_{ACQ2} = (6.2 \times R_S \times 15pF) + t_{ACQ}$$

where R_S = the source impedance of the input signal; t_{ACQ} is the T/H acquisition time from the *Electrical Characteristics* table.

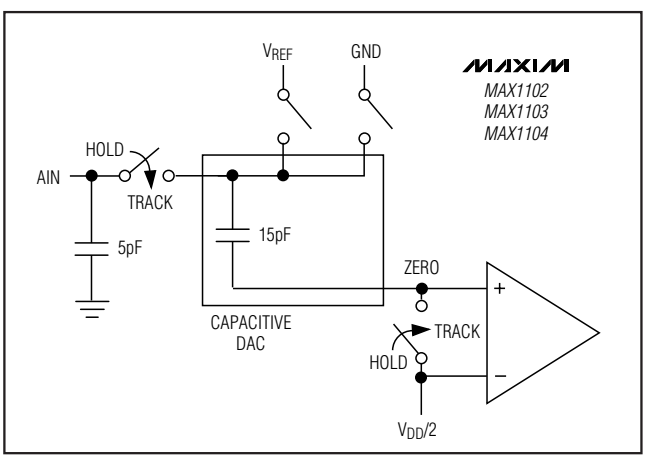


Figure 2. Equivalent Input Circuit

Conversion Progress

The comparator's negative input is connected to the auto-zero rail. Since the device requires only a single supply, the ZERO node at the input of the comparator equals $V_{DD}/2$. The capacitive DAC restores node ZERO to have no voltage difference at the comparator inputs within the limits of an 8-bit resolution.

Input Voltage Range

Internal protection diodes that clamp the analog input to V_{DD} and GND allow AIN to swing from (V_{GND} - 0.3V) to (V_{DD} + 0.3V) without damaging the device. However, for accurate conversions, the input must not exceed (V_{DD} + 0.05V) or be less than (V_{GND} - 0.05V).

The valid input range for the analog input is from GND to V_{REF}. The output code is invalid (code zero) when a negative input voltage is applied, and full scale (FS) when the input voltage exceeds the reference.

Input Bandwidth

The ADC's input tracking circuitry has a 2.5MHz full-power bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, low-pass filters such as the MAX7418–MAX7426 are recommended.

Digital-to-Analog Converter

The MAX1102/MAX1103/MAX1104 DAC section uses an R-2R ladder network that converts the 8-bit digital input into an equivalent analog output voltage proportional to the applied reference voltage (Figure 3). The DAC features a double-buffered input, and a buffered analog output.

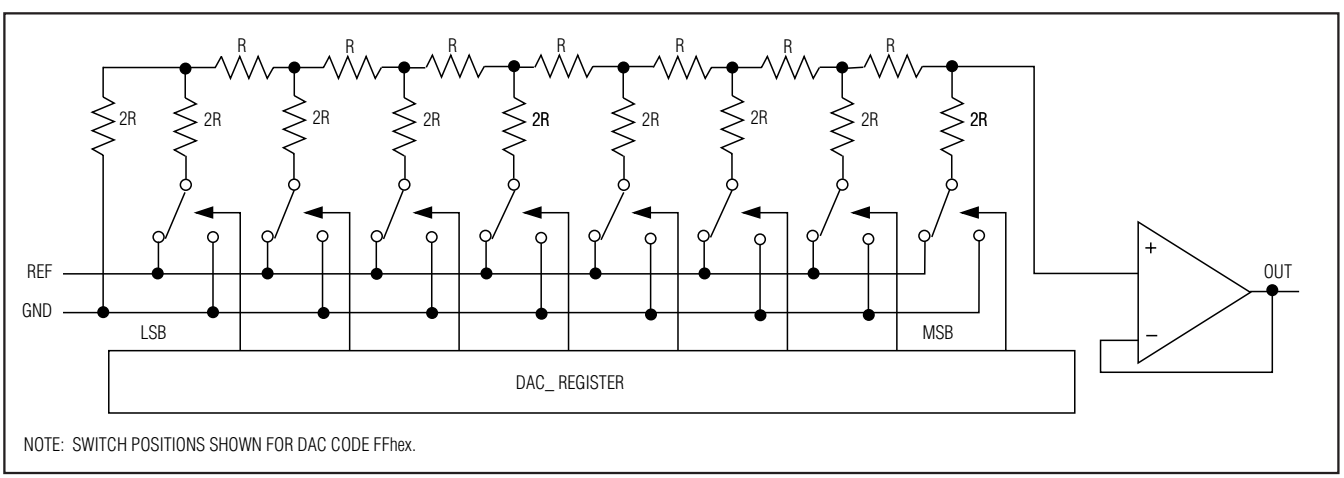


Figure 3. DAC Simplified Circuit Diagram

Output Buffer

The MAX1102/MAX1103/MAX1104 analog output is internally buffered by a precision unity-gain buffer that slews at 1.2V/µs (typ). The output swings from V_{GND} to V_{DD} - 0.1V. With a 0 to V_{DD} - 0.1V (or V_{DD} - 0.1V to 0) output transition, the amplifier output typically settles to 1/2LSB in 11µs when loaded with 10kΩ in parallel with 100pF.

The buffer amplifier is stable with any combination of resistive (≥ 10kΩ) or capacitive (≤ 100pF) loads.

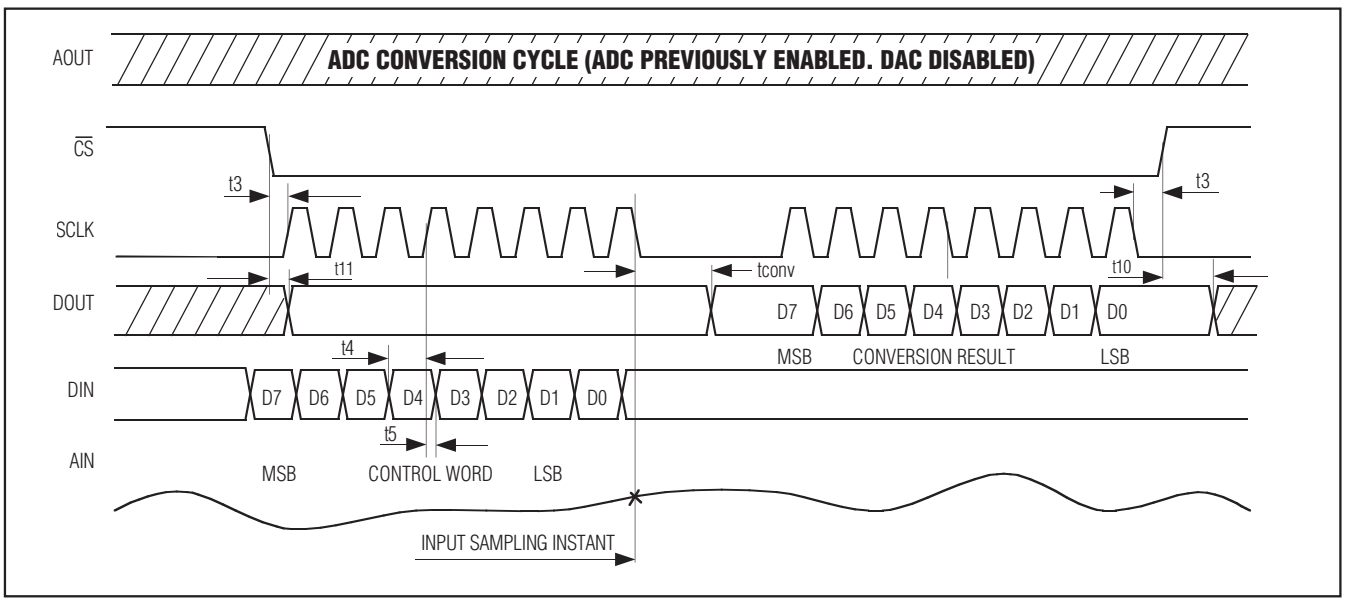


Figure 4a. Serial Interface Timing Diagram. ADC enabled and DAC disabled.

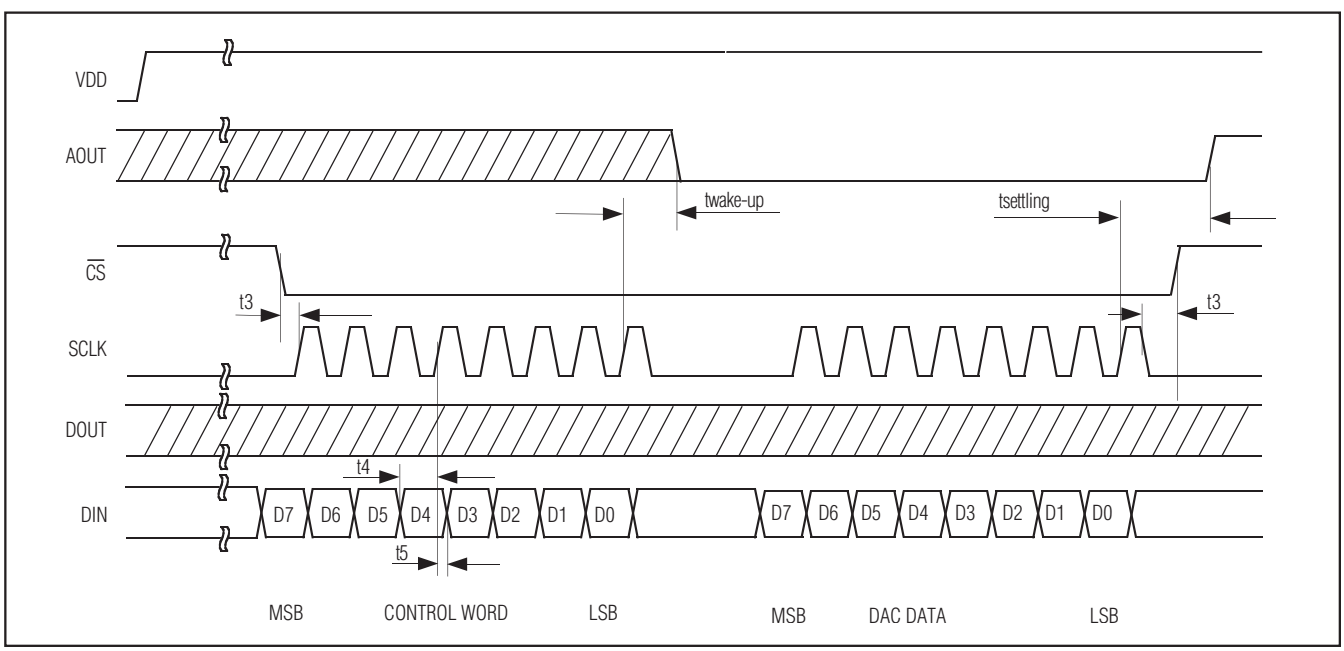


Figure 4b. Serial Interface Timing Diagram. ADC disabled and DAC disabled.

Serial Interface and Control Logic

The MAX1102/MAX1103/MAX1104 have 4-wire serial interfaces (Figure 4). The $\overline{CS}$, SCLK, and DIN inputs are used to control and configure the device, while the three-state DOUT provides access to the ADC conversion result. DIN also serves as the data input to the DAC.

The serial interface provides easy connection to µCs with SPI, QSPI, and MICROWIRE serial interfaces at clock rates up to 6MHz. For SPI and QSPI, set CPOL = CPHA = 0 in the SPI control registers of the µC. Figure 4 gives detailed timing information.

Digital Inputs and Outputs

The logic levels of the MAX1102/MAX1103/MAX1104 digital inputs are set to accept voltage levels from both +3V and +5V systems regardless of the supply voltages.

Performing a Conversion

Configuring the MAX1102/MAX1103/MAX1104

The MAX1102/MAX1103/MAX1104 must be configured before a conversion can occur. Following $\overline{CS}$ falling, on each rising edge of SCLK, a bit from DIN is clocked into the MAX1102/MAX1103/MAX1104's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the MSB of the control byte (START). Until the START bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The control word sets the mode in which the MAX1102/MAX1103/MAX1104 operate. The enable bits, E0 to E2, determine what sections of the device are operating by either enabling or shutting down the two converters and voltage reference (see *Shutdown Modes*). The enable bits are independent of the address bits; for example, the ADC need not be addressed for it to be shutdown or powered up.

C0 and C1 are the control bits. C0 sets the conversion mode, either single or continuous (see *Conversion Modes*). C1 determines whether the ADC monitors $V_{DD}/2$ or AIN (see *Power Sense*). When changing C1, two control words must be written. The first control word changes the state of the mux. Then wait 3.5µs for the T/H to acquire the new input. Finally, the second control word causes the conversion to take place. For MAX1104 set C1 = 0.

A0 is the ADC address bit. A logic "1" on A0 addresses the ADC. The control word configures the ADC. A logic "0" on A0 deselects the ADC. In this state, the ADC is still active, but does not perform any conversions.

A1 is the DAC address bit. A logic "1" on A1 addresses the DAC. The control word configures the DAC, and the eight bits following the control word are read in as DAC data. The converted analog output is available after the eighth data bit is read into the device. A logic "0" deselects the DAC. In this state the DAC is still active, but ignores any digital inputs.

Both the ADC and DAC can be addresses from the same control word, allowing both converters to operate simultaneously.

Table 1. Control-Byte Format

BIT	NAME	DESCRIPTION
7 (MSB)	START	1 = designates a new control word. 0 = control word ignored, unless byte is DAC data.
6	A1	1 = DAC addressed. Current byte configures DAC, the following byte is DAC data. 0 = DAC not addressed.
5	A0	1 = ADC addressed. Current byte configures ADC. After the 36µs conversion time, the next eight clock cycles clock out the conversion result. 0 = ADC not addressed.
4	C1*	1 = ADC input to $V_{DD}/2$. 0 = ADC input to AIN.
3	C0	1 = Continuous conversion. Control word not required unless the device is reconfigured. 0 = Single conversion. New control word required before next conversion.
2	E2	1 = Reference enabled. 0 = Reference disabled. Don't care for MAX1104.
1	E1	1 = ADC enabled. 0 = ADC disabled.
0	E0	1 = DAC enabled. 0 = DAC disabled.

** Leave C1 = 0 for MAX1104.*

Configuring the ADC

When configuring the ADC immediately following power-up, the first control word enables the ADC and sets the T/H to track mode. Then wait 200µs for the internal reference to stablize (3µs typical from standby mode). Finally, the second control word sets the ADC into either single or continuous mode and causes conversion to take place.

Conversion Modes

The MAX1102/MAX1103/MAX1104 have two conversion modes, single and continuous.

In single conversion mode (C0 = 0), a control word must be written before an ADC conversion result can be read, or DAC input data is accepted. Once a conversion has occurred, the device will ignore any input until a new control word is written. Figures 5 and 6 show the DAC and ADC single conversion mode timing diagrams.

In continuous conversion mode (C0 = 1), the device maintains its configuration from a single control word, and continuously updates the ADC conversion result, or accepts new DAC input data.

When operating the ADC and DAC simultaneously, both converters must be in the same conversion mode.

ADC Single Conversion Mode

Set C0 = 0 to select single conversion mode. The falling edge of SCLK after the eighth bit of each control word causes the ADC to switch from track to hold mode and begin conversion. To avoid corruption of the conversion result, SCLK must be disabled for 36µs (Figure 6). After completing the conversion, the ADC automatically returns to track mode, and the next eight clock cycles shift out the result on DOUT.

A minimum of 3.5µs in track mode is required for complete acquisition.

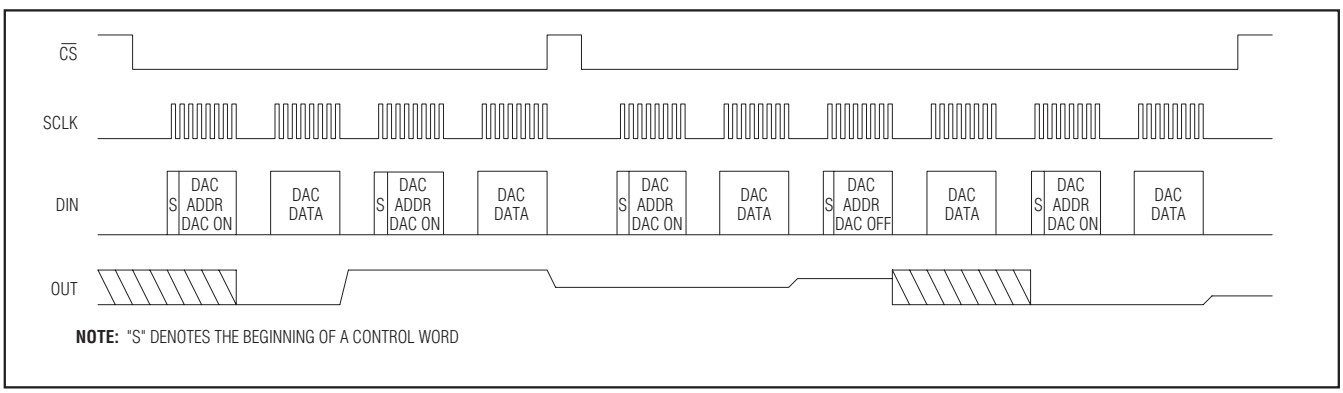


Figure 5. DAC Single Conversion Mode Timing Diagram

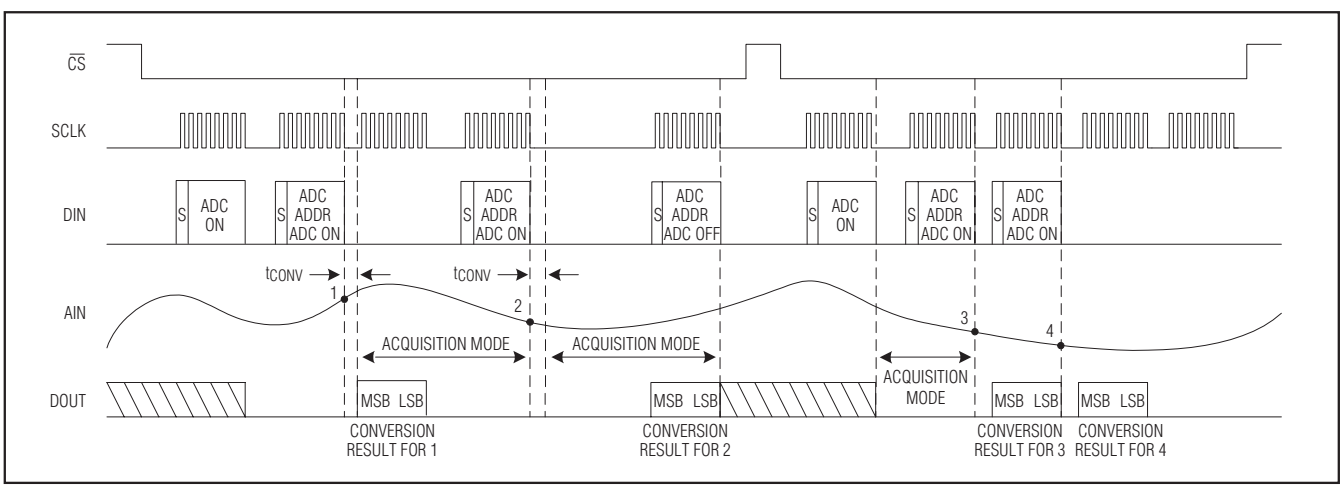


Figure 6. ADC Single Conversion Mode Timing Diagram

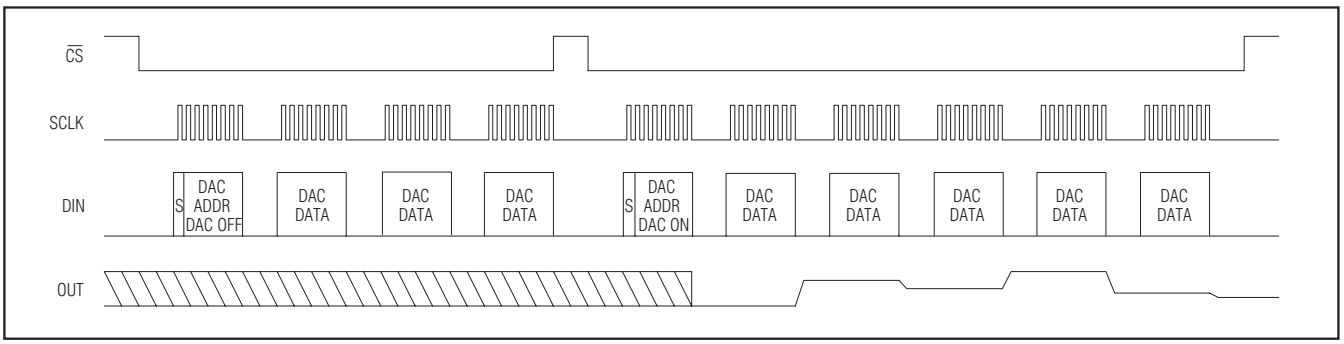


Figure 7. DAC Continuous Conversion Mode Timing Diagram

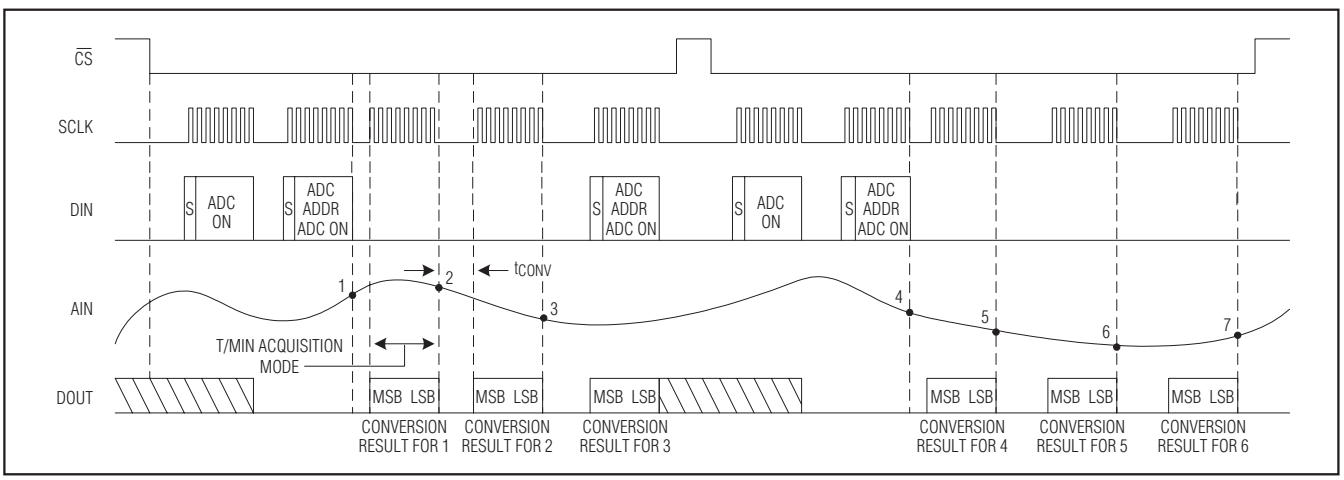


Figure 8. ADC Continuous Conversion Mode Timing Diagram

DAC Continuous Conversion Mode

Once the DAC is configured in continuous conversion mode, the analog output, OUT, is updated at the rising edge of every eighth clock pulse (Figure 7). To exit DAC continuous conversion mode, toggle $\overline{CS}$. The device requires a new control word before any further conversions take place.

ADC Continuous Conversion Mode

Set C0 = 1 to select continuous conversion mode. The falling edge of SCLK after the eighth bit of the control word causes the ADC to switch from track to hold mode and begin conversion. To avoid corruption of the conversion result, SCLK must be disabled for 36µs (Figure 8). After completing the conversion, the ADC automatically returns to track mode, and the next eight clock cycles shift out the result on DOUT. The falling edge of SCLK during the eighth bit of the result will again cause the ADC to switch from track to hold mode and begin the next conversion.

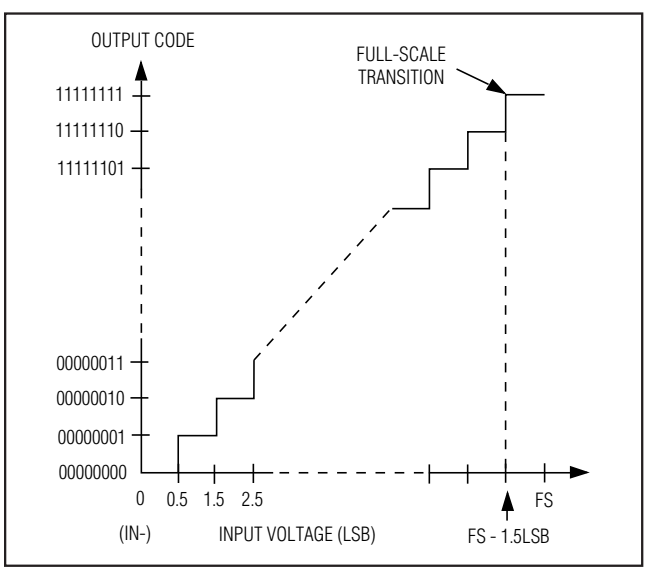


Figure 9. ADC Input/Output Transfer Function

A minimum of 3.5µs in track mode is required for complete acquisition.

In continuous ADC-only conversion mode, a new control word (START = 1) reconfigures the device.

Interrupted Communication Results

If $\overline{CS}$ transitions from low to high during the reception of a control word, the MAX1102/MAX1103/MAX1104 enters its power-on reset state (full shutdown mode). If $\overline{CS}$ is toggled while receiving DAC data, the input is ignored and any received bits are discarded. In both cases, once $\overline{CS}$ returns low, the device requires a new control word before further conversions can occur. If $\overline{CS}$ goes high while data is read from the device, DOUT enters a high-impedance state, and the serial clock is ignored. When $\overline{CS}$ returns low, the remaining bits of the conversion result can be clocked out.

Applications Information

Power-On Reset

When power is first applied, the device enters full shutdown mode and the DAC registers are reset to 0. To wake up the device, the proper control word must be written and 200µs allowed for the internal reference to stablize. DAC data may be written to the device immediately following the control word, but OUT will not finish settling until the wake-up time has passed.

Power Sense

The MAX1102/MAX1103 provide a multiplexer which sets the T/H to either AIN or one-half of V_{DD}. With C1 = 1, the ADC converts the $V_{DD}/2$ voltage, providing power sensing capability to the system. When switching the input multiplexer, two control words must be written before any conversion takes place. The first control word changes the multiplexer state, and the second starts the conversion.

Reference

The full-scale range of both the ADC and DAC is set by the internal voltage reference. The MAX1102 provides a +2.0V reference, the MAX1103 has a +4.0V reference, and the MAX1104 uses V_{DD} as the reference voltage.

ADC Transfer Function

Figure 9 depicts the ADC input/output transfer function. Code transitions occur at the center of every LSB step. Output coding is binary; with a 2.0V reference 1LSB = (V_{REF}/256) = 7.8125mV. Full scale is achieved at V_{AIN} = V_{REF} - 1.5LSB. Negative input voltages are invalid and give a zero output code. Voltages greater than full scale give an all ones output code.

Shutdown Modes

The MAX1102/MAX1103/MAX1104 feature four software-selectable shutdown modes, helping to conserve power by disabling any unused portion of the device. Bits 0 through 2 of the control word select the device shutdown mode (Table 1). Table 2 details the four power modes with the corresponding supply current and operating sections.

The ADC and DAC are individually controlled and can be shutdown independently of each other. Bit 0 (E0) controls the DAC, a logic “1” enables the DAC, a logic “0” disables the DAC. Bit 1 (E1) controls the ADC, a logic “1” enables the ADC, a logic “0” disables the ADC. Either the ADC or DAC or both can be shutdown, conserving power when one or both converters are not in use. A fast wake-up time (3µs ADC, 10µs DAC) allows the converters to be cycled in and out of shutdown even during short duration idle times.

Data can be written to the DAC while it is in shutdown. A control word with A1 = 1 and E0 = 0 disables the DAC while allowing data to be written to the DAC. The eight bits following this control word are shifted into the DAC register. Conversion takes place once the DAC is enabled.

Table 2. Operation Modes

BIT			SUPPLY CURRENT	OPERATING SECTIONS		
E2	E1	E0		REF	ADC	DAC
0	0	0	1µA	Off	Off	Off
1	0	0	18µA	On	Off	Off
1	1	0	250µA	On	On	Off
1	0	1	400µA	On	Off	On
1	1	1	520µA	On	On	On

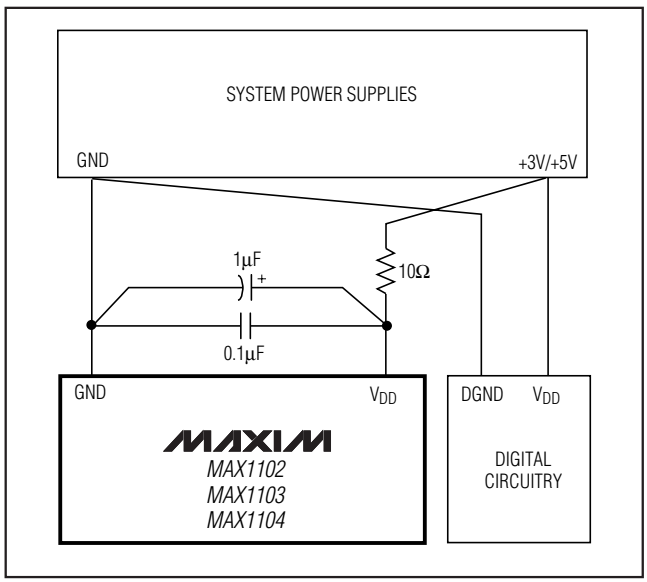


Figure 10. Power-Supply Connections

Two control words are necessary to enable the ADC. The first control word brings the ADC out of shutdown, and sets the T/H in acquisition mode. The second control word initiates the conversion.

Bit 2 (E2) controls the reference. A logic "1" enables the reference, a logic "0" disables the reference, further reducing power consumption.

Power Supply Bypassing and Layout

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another or run digital lines underneath the device.

Figure 10 shows the recommended system-ground connections. A single-point analog ground (star-ground point) should be established at the device ground. Connect all analog grounds to the star ground. No digital-system ground should be connected to this point. The ground return to the power supply for the star ground should be connected to this point. The ground return to the power supply for the star ground should be low impedance and as short as possible for noise-free operation. High-frequency noise in the VDD power supply may affect device performance. Bypass the supply to the star ground with 0.1µF and 1µF capacitors close to the device. Minimize capacitor lead lengths for best supply-noise rejection. If the power supply is very noisy, connect a 10Ω resistor in series with VDD to form a lowpass filter.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 µMAX	U8+1	21-0036	90-0092

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/00	Initial release	—
1	1/11	Changed spec in *Timing Characteristics* section	4