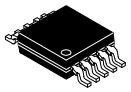
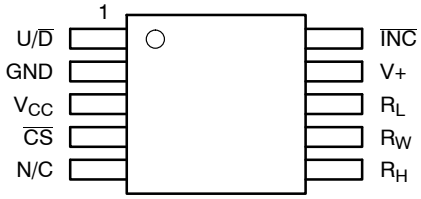
# 16 Volt Digital Potentiometer (POT) with 128 Taps and an Increment Decrement Interface

# CAT5133



**MSOP10**
**Z SUFFIX**
**CASE 846AG**

## PIN CONNECTIONS




(Top View)

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| CAT5133ZI−10−GT3 | MSOP10 (Pb−Free) | 3,000/ Tape & Reel |
| CAT5133ZI−50−GT3 (Note 4) | MSOP10 (Pb−Free) | 3,000/ Tape & Reel |
| CAT5133ZI−00−GT3 (Note 4) | MSOP10 (Pb−Free) | 3,000/ Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com.
2. All packages are RoHS-compliant (Lead-Free, Halogen-Free).
3. The standard lead finish is NiPdAu.
4. For additional package and temperature options, please contact your nearest **onsemi** Sales office.

## Description

The CAT5133 is a high voltage digital POT integrated with EEPROM memory and control logic to operate in a similar manner to a mechanical potentiometer. The digital ponentiometer consists of a series of resistive elements connected between two externally accessible end points. The tap points between each resistive element are connected to the wiper outputs with CMOS switches. A 7-bit wiper control register (WCR) independently controls the wiper tap switches for the digital potentiometer. Associated with the control register is a 7-bit nonvolatile memory data register (DR) used for storing the wiper settings. Changing the value of the wiper control register or storing that value into the nonvolatile memory is performed via a 3-input Increment-Decrement interface.

The CAT5133 comes with 2 voltage supply inputs: $V_{CC}$ (digital supply voltage) input and V+ (analog bias supply) input. Providing separate Digital and Analog inputs allow the potentiometer terminals to be as much as 10 volts above $V_{CC}$ and 16 volts above ground.

The CAT5133 can be used as a potentiometer or as a two terminal, variable resistor. It is designed for circuit level or system level adjustments in a wide variety of applications.

On power-up, the contents of the nonvolatile data register (DR) are transferred to the wiper control register (WCR) and the wiper is positioned to that location. The CAT5133 is shipped with the DR programmed to position 64.

## Features

- Single Linear Digital Potentiometer with 128 Taps
- End-to-End Resistance of 10 kΩ, 50 kΩ or 100 kΩ
- 2-wire Interface
- Fast Up/Down Wiper Control Mode
- Non-volatile Wiper Setting Storage
- Automatic Wiper Setting Recall at Power−up
- Digital Supply Range ($V_{CC}$): 2.7 V to 5.5 V
- Analog Supply Range (V+): +8 V to +16 V
- Low Standby Current: 15 μA
- 100 Year Wiper Setting Memory
- Industrial Temperature Range: −40°C to +85°C
- 10-pin MSOP Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

## Applications

- LCD Screen Adjustment
- Volume Control
- Mechanical Potentiometer Replacement
- Gain Adjustment
- Line Impedance Matching
- VCOM Settings Adjustment

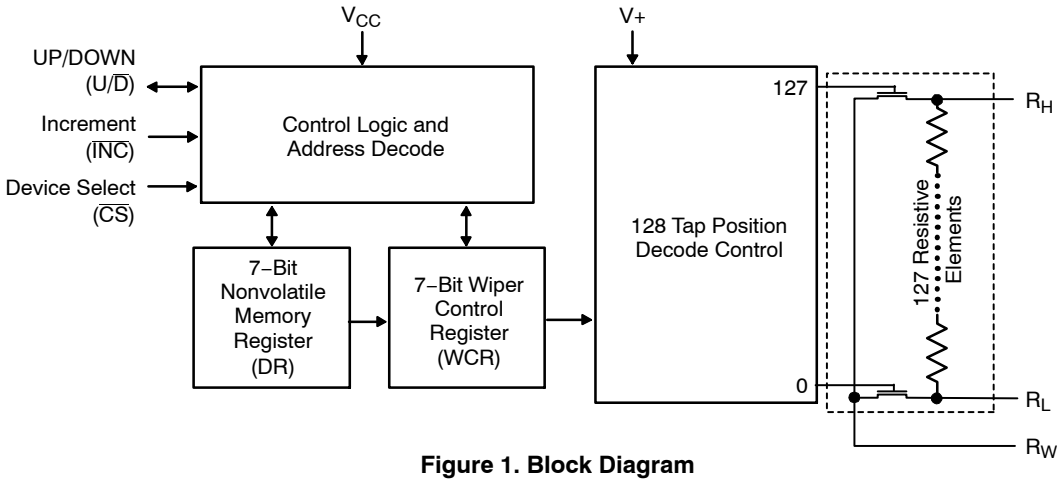



**Figure 1. Block Diagram**

**Table 1. PIN DESCRIPTIONS**

| Pin | Name | Function |
|---|---|---|
| 1 | U/$\overline{D}$ | Up/Down Data Input – Determines the direction of movement of the wiper |
| 2 | GND | Ground |
| 3 | $V_{CC}$ | Logic Supply Voltage (2.7 V to 5.5 V) |
| 4 | $\overline{CS}$ | Chip Select – The chip is selected when the input is low. |
| 5 | N/C | No Connect |
| 6 | $R_H$ | High Reference Terminal for the Potentiometer |
| 7 | $R_W$ | Wiper Terminal for the Potentiometer |
| 8 | $R_L$ | Low Reference Terminal for the Potentiometer |
| 9 | $V_+$ | Analog Bias Voltage Input (+8.0 V to +16.0 V) |
| 10 | $\overline{INC}$ | Increment Input – Moves the wiper in the direction determined by the Up/Down input on each negative edge |

## DEVICE OPERATION

The CAT5133 operates like a digitally controlled potentiometer with $R_H$ and $R_L$ equivalent to the high and low terminals and $R_W$ equivalent to the mechanical potentiometer's wiper. There are 128 available tap positions including the resistor end points, $R_H$ and $R_L$. There are 127 resistor elements connected in series between the $R_H$ and $R_L$ terminals. The wiper terminal is connected to one of the 128 taps and controlled by three inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$. These inputs control a 7-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the $\overline{INC}$ and $\overline{CS}$ inputs.

With $\overline{CS}$ set LOW the CAT5133 is selected and will respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement the wiper (depending on the state of the U/$\overline{D}$ input and 7-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH. When the CAT5133 is powered-down; the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With $\overline{INC}$ set low, the CAT5133 may be de-selected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

**Table 2. OPERATION MODES**

| $\overline{INC}$ | $\overline{CS}$ | U/$\overline{D}$ | Operation |
|---|---|---|---|
| High to Low | Low | High | Wiper toward H |
| High to Low | Low | Low | Wiper toward L |
| High | Low to High | X | Store Wiper Position |
| Low | Low to High | X | No Store, Return to Standby |
| X | High | X | Standby |

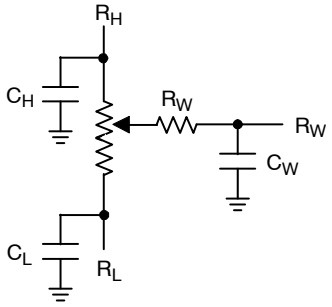



**Figure 2. Potentiometer Equivalent Circuit**

### Power-On and Potentiometer Characteristics

The CAT5133 is a 128-position, digital controlled potentiometer. When applying power to the CAT5133, $V_{CC}$ must be supplied prior to or simultaneously with V+. At the same time, the signals on $R_H$, $R_W$ and $R_L$ terminals should not exceed V+. If V+ is applied before $V_{CC}$, the electronic switches of the digital potentiometer are powered in the absence of the switch control signals, that could result in multiple switches being turned on. This causes unexpected wiper settings and possible current overload of the potentiometer.

When $V_{CC}$ is applied, the device turns on at the mid-point wiper location (64) until the wiper register can be loaded with the nonvolatile memory location previously stored in the device. After the nonvolatile memory data is loaded into the wiper register the wiper location will change to the previously stored wiper position.

At power-down, it is recommended to turn-off first the signals on $R_H$, $R_W$ and $R_L$, followed by V+ and, after that, $V_{CC}$, in order to avoid unexpected transitions of the wiper and uncontrolled current overload of the potentiometer.

The end-to-end nominal resistance of the potentiometer has 128 contact points linearly distributed across the total resistor. Each of these contact points is addressed by the 7 bit wiper register which is decoded to select one of these 128 contact points.

Each contact point generates a linear resistive value between the 0 position and the 127 position. These values can be determined by dividing the end-to-end value of the potentiometer by 127. The 10 kΩ potentiometer has a resistance of ~79 Ω between each wiper position. However in addition to the ~79 Ω for each resistive segment of the potentiometer, a wiper resistance offset must be considered. Table 3 shows the effect of this value and how it would appear on the wiper terminal.

This offset will appear in each of the CAT5133 end-to-end resistance values in the same way as the 10 kΩ example. However resistance between each wiper position for the 50 kΩ version will be ~395 Ω and for the 100 kΩ version will be ~790 Ω.

**Table 3. POTENTIOMETER RESISTANCE AND WIPER RESISTANCE OFFSET EFFECTS**

| Position | Typical $R_W$ to $R_L$ Resistance for 10 kΩ Digital Potentiometer | | Position | Typical $R_W$ to $R_H$ Resistance for 10 kΩ Digital Potentiometer | |
|---|---|---|---|---|---|
| 0 | 70 Ω or | 0 Ω + 70 Ω | 00 | 10,070 Ω or | 10,000 Ω + 70 Ω |
| 01 | 149 Ω or | 79 Ω + 70 Ω | 64 | 5,047 Ω or | 4,977 Ω + 70 Ω |
| 63 | 5,047 Ω or | 4,977 Ω + 70 Ω | 126 | 149 Ω or | 79 Ω + 70 Ω |
| 127 | 10,070 Ω or | 10,000 Ω + 70 Ω | 127 | 70 Ω or | 0 Ω + 70 Ω |

**Table 4. ABSOLUTE MAXIMUM RATINGS**

| Parameters | Ratings | Units |
|---|---|---|
| Temperature Under Bias | −55 to +125 | °C |
| Storage Temperature | −65 to +150 | °C |
| Voltage on any U/$\overline{D}$, $\overline{INC}$, & $\overline{CS}$ Pins with Respect to $V_{CC}$ (Note 5) | −0.3 to +$V_{CC}$ + 0.3 | V |
| Voltage on $R_H$, $R_L$, & $R_W$ Pins with Respect to $V_{CC}$ | V+ | V |
| $V_{CC}$ with Respect to Ground | −0.3 to +6.0 | V |
| V+ with respect to Ground | −0.3 to +16.5 | V |
| Wiper Current | ±6 | mA |
| Lead Soldering temperature (10 seconds) | +300 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

5. Latch-up protection is provided for stresses up to 100 mA on the digital from −0.3 V to $V_{CC}$ + 0.3 V.

## RECOMMENDED OPERATING CONDITIONS

$V_{CC}$ = +2.7 V to +5.5 V
V+ = +8.0 V to +16.0 V
Operating Temperature Range: −40°C to +85°C

**Table 5. POTENTIOMETER CHARACTERISTICS** (Over recommended operating conditions unless otherwise stated.)

| Symbol | Parameter | Test Conditions | Limits | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $R_{POT}$ | Potentiometer Resistance (10 kΩ) | | | 10 | | kΩ |
| $R_{POT}$ | Potentiometer Resistance (50 kΩ) (Note 12) | | | 50 | | kΩ |
| $R_{POT}$ | Potentiometer Resistance (100 kΩ) (Note 12) | | | 100 | | kΩ |
| $R_{TOL}$ | Potentiometer Resistance Tolerance | | | | ±20 | % |
| | Power Rating | 25°C | | | 50 | mW |
| $I_W$ | Wiper Current | | | | ±3 | mA |
| $R_W$ | Wiper Resistance | $I_W$ = +1 mA @ V+ = 12 V | | 70 | 150 | Ω |
| | | $I_W$ = +1 mA @ V+ = 8 V | | 110 | 200 | |
| $V_{TERM}$ | Voltage on $R_W$, $R_H$ or $R_L$ | GND = 0 V; V+ = 8 V to 16 V | GND | | V+ | V |
| RES | Resolution | | | 0.78 | | % |
| $A_{LIN}$ | Absolute Linearity (Note 7) | $V_{W(n)(actual)} - V_{W(n)(expected)}$ (Notes 10, 11) | | | ±1 | LSB (Note 9) |
| $R_{LIN}$ | Relative Linearity (Note 8) | $V_{W(n+1)} - [V_{W(n)} + LSB]$ (Notes 10, 11) | | | ±0.5 | LSB (Note 9) |
| $TC_{RPOT}$ | Temperature Coefficient of $R_{POT}$ | (Note 6) | | ±300 | | ppm/°C |
| $TC_{Ratio}$ | Ratiometric Temperature Coefficient | (Note 6) | | | 30 | ppm/°C |
| $C_H/C_L/C_W$ | Potentiometer Capacitances | (Note 6) | | 10/10/25 | | pF |
| fc | Frequency Response | $R_{POT}$ = 50 kΩ | | 0.4 | | MHz |

6. This parameter is tested initially and after a design or process change that affects the parameter.
7. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
8. Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer.
9. LSB = $(R_{HM} - R_{LM})/127$; where $R_{HM}$ and $R_{LM}$ are the highest and lowest measured values on the wiper terminal.
10. n = 1, 2, ..., 127.
11. $V^+$ @ $R_H$; 0 V @ $R_L$; $V_W$ measured @ $R_W$, with no load.
12. Contact factory for availability on this version of the CAT5133.

**Table 6. DC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +2.7 V to +6.0 V, unless otherwise specified.)

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{CC1}$ | Power Supply Current | $V_{CC}$ = 5.5 V, $f_{INC}$ = 1 MHz, Input = GND | | 1 | mA |
| $I_{CC2}$ | Power supply Current Nonvolatile WRITE | $V_{CC}$ = 5.5 V, $f_{INC}$ = 1 MHz, Input = GND | | 3.0 | mA |
| $I_{SB(VCC)}$ | Standby Current ($V_{CC}$ = 5 V) | $V_{IN}$ = GND or $V_{CC}$, INC = VCC | | 5 | μA |
| $I_{SB(V+)}$ | V+ Standby Current | $V_{CC}$ = 5 V, V+ = 16 V | | 10 | μA |
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = GND to $V_{CC}$ | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = GND to $V_{CC}$ | | 10 | μA |
| $V_{IL}$ | Input Low Voltage | | –1 | $V_{CC}$ x 0.3 | V |
| $V_{IH}$ | Input High Voltage | | $V_{CC}$ x 0.7 | $V_{CC}$ + 1.0 | V |
| $V_{OL1}$ | Output Low Voltage ($V_{CC}$ = 3.0 V) | $I_{OL}$ = 3 mA | | 0.4 | V |

**Table 7. CAPACITANCE** ($T_A$ = 25°C, f = 1.0 MHz, $V_{CC}$ = 5.0 V)

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $C_{I/O}$ | Input/Output Capacitance (SDA) | $V_{I/O}$ = 0 V (Note 13) | | 8 | pF |
| $C_{IN}$ | Input Capacitance (A0, A1, SCL) | $V_{IN}$ = 0 V (Note 13) | | 6 | pF |

**Table 8. POWER UP TIMING** (Notes 13, 14)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{PUR}$ | Power-up to Read Operation | | 1 | ms |
| $t_{PUW}$ | Power-up to Write Operation | | 1 | ms |

**Table 9. WIPER TIMING**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{WRPO}$ | Wiper Response Time After Power Supply Stable | 5 | 10 | μs |
| $t_{WRL}$ | Wiper Response Time After Instruction Issued | 5 | 10 | μs |

**Table 10. WRITE CYCLE LIMITS**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{WR}$ | Write Cycle Time | | 5 | ms |

**Table 11. RELIABILITY CHARACTERISTICS** (Over recommended operating conditions unless otherwise stated.)

| Symbol | Parameter | Reference Test Method | Min | Max | Units |
|---|---|---|---|---|---|
| $N_{END}$ (Note 13) | Endurance | MIL–STD–883, Test Method 1033 | 100,000 | | Cycles/Byte |
| $T_{DR}$ (Note 13) | Data Retention | MIL–STD–883, Test Method 1008 | 100 | | Years |

13. This parameter is tested initially and after a design or process change that affects the parameter.
14. $t_{PUR}$ and $t_{PUW}$ are the delays required from the time $V_{CC}$ is stable until the time the specified operation can be initiated.

**Table 12. A.C. OPERATING CHARACTERISTICS** ($V_{CC}$ = +2.5 V to +6.0 V, $V_H$ = $V_{CC}$, $V_L$ = 0 V, unless otherwise specified.)

| Symbol | Parameter | Min | Typ (Note 15) | Max | Units |
|---|---|---|---|---|---|
| $t_{CI}$ | $\overline{CS}$ to $\overline{INC}$ Setup | 100 | | | ns |
| $t_{DI}$ | U/$\overline{D}$ to $\overline{INC}$ Setup | 50 | | | ns |
| $t_{ID}$ | U/$\overline{D}$ to $\overline{INC}$ Hold | 100 | | | ns |
| $t_{IL}$ | $\overline{INC}$ LOW Period | 250 | | | ns |
| $t_{IH}$ | $\overline{INC}$ HIGH Period | 250 | | | ns |
| $t_{IC}$ | $\overline{INC}$ Inactive to $\overline{CS}$ Inactive | 1 | | | µs |
| $t_{CPH}$ | $\overline{CS}$ Deselect Time (NO STORE) | 100 | | | ns |
| $t_{CPH}$ | $\overline{CS}$ Deselect Time (STORE) | 10 | | | ms |
| $t_{IW}$ | $\overline{INC}$ to VOUT Change | | 1 | 5 | µs |
| $t_{CYC}$ | $\overline{INC}$ Cycle Time | 1 | | | µs |
| $t_R$, $t_F$ (Note 16) | $\overline{INC}$ Input Rise and Fall Time | | | 500 | µs |
| $t_{PU}$ (Note 16) | Power-up to Wiper Stable | | | 1 | ms |
| $t_{WR}$ | Store Cycle | | 5 | 10 | ms |

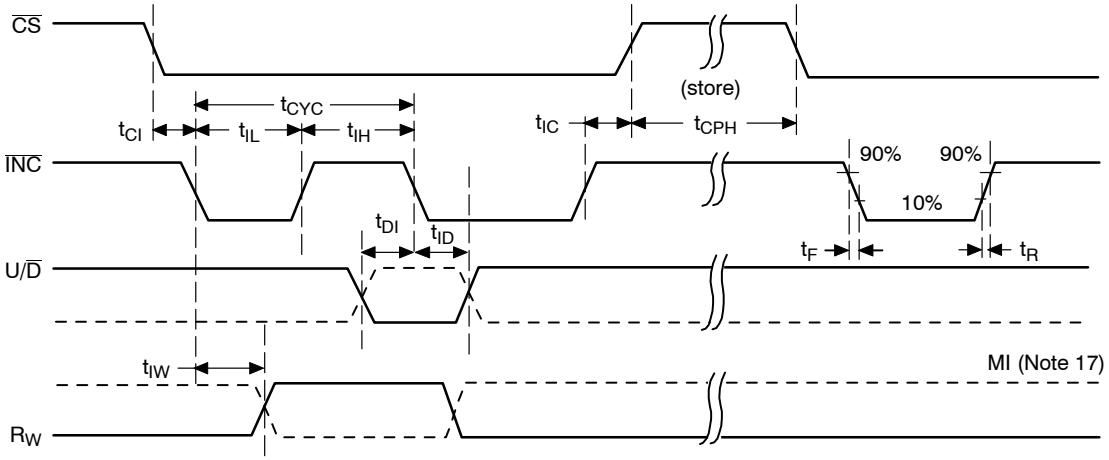



**Figure 3. A.C. Timing**

15. Typical values are for $T_A$ = 25°C and nominal supply voltage.
16. This parameter is periodically sampled and not 100% tested.
17. MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

## TYPICAL PERFORMANCE CHARACTERISTICS

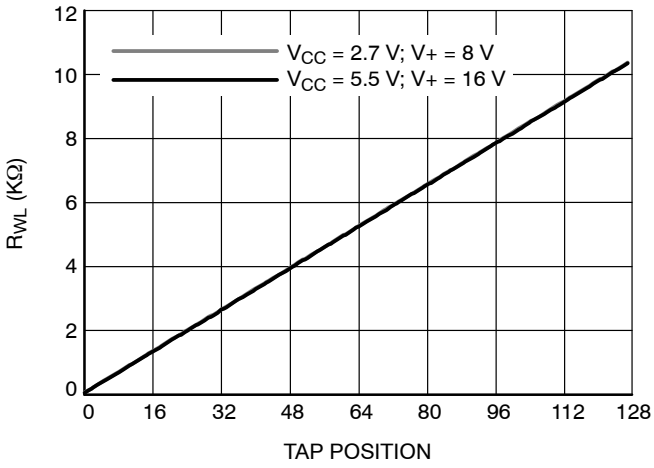



**Figure 4. Resistance between $R_W$ and $R_L$**

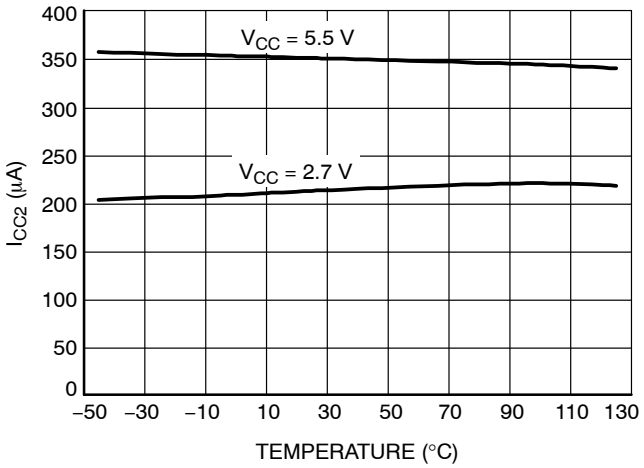



**Figure 5. $I_{CC2}$ (NV Write) vs. Temperature**

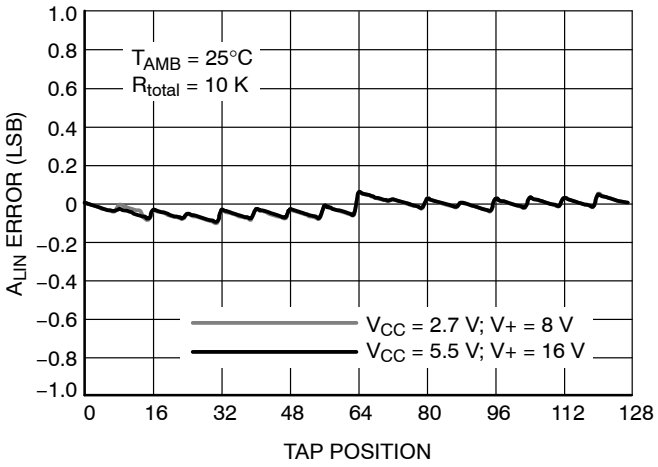



**Figure 6. Absolute Linearity Error per Tap Position**

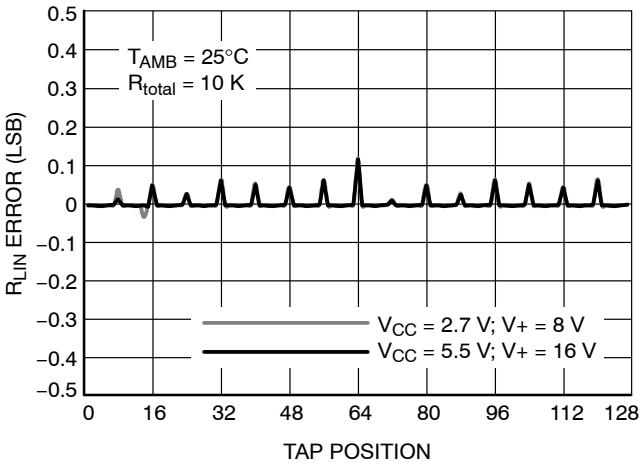



**Figure 7. Relative Linearity Error**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

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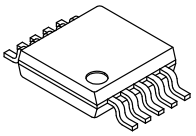

**Micro10 / MSOP10 (150 mil)**
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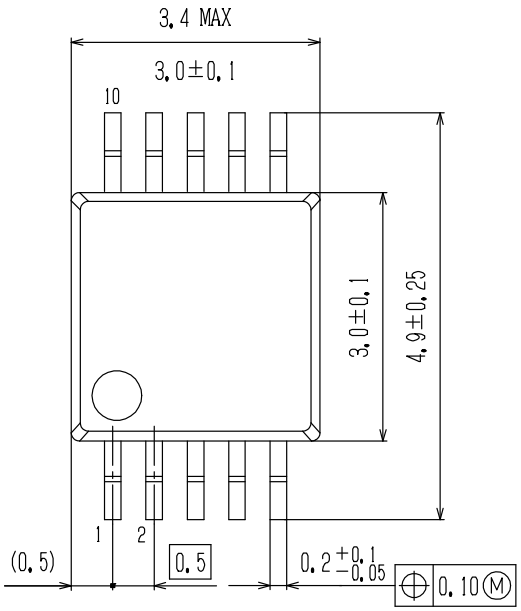
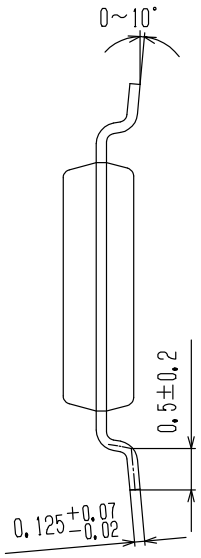
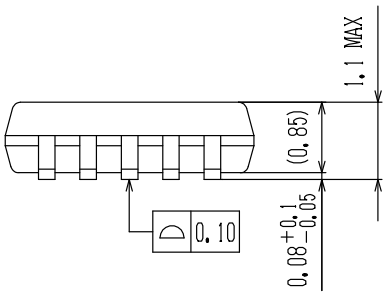
ISSUE A

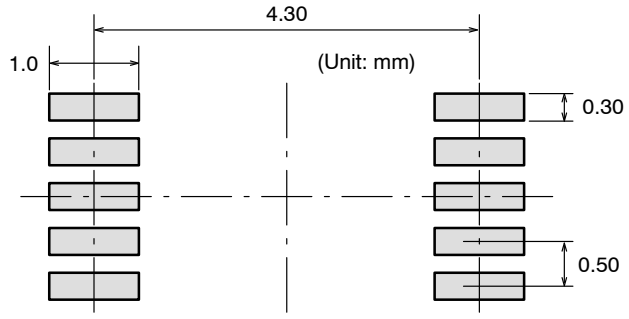
DATE 23 OCT 2013



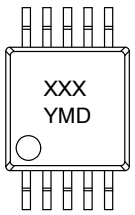

**SOLDERING FOOTPRINT***




NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




XXX = Specific Device Code
Y = Year
M = Month
D = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

| | | |
|---|---|---|
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