1.5°C ACCURATE DIGITAL TEMPERATURE SENSOR WITH SPI™ INTERFACE

FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of -40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Digital Output: SPI-Compatible Interface**
- **Resolution: 12-Bit + Sign, 0.0625°C**
- **Accuracy: ±1.5°C from –25°C to 85°C (max)**
- **Low Quiescent Current: 50 μA (max)**
- **Wide Supply Range: 2.7 V to 5.5 V**
- **Tiny SOT23-6 Package**
- **Operation to 150°C**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

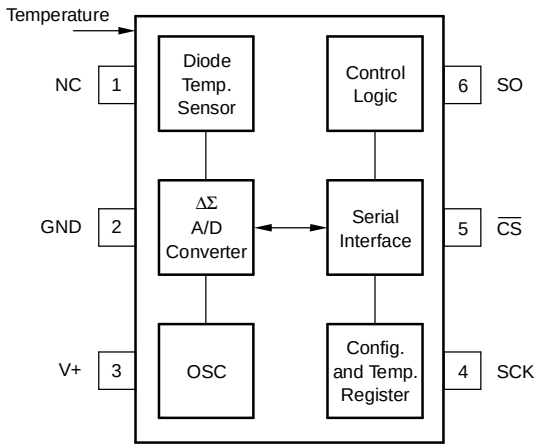
APPLICATIONS

- **Power-Supply Temperature Monitoring**
- **Computer Peripheral Thermal Protection**
- **Notebook Computers**
- **Battery Management**
- **Environmental Monitoring**

DESCRIPTION

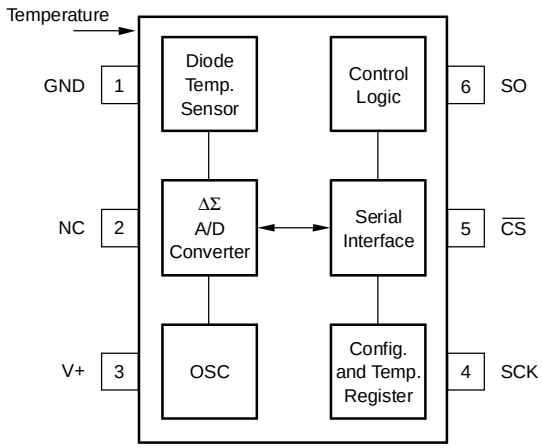
The TMP121 and TMP123 are SPI-compatible temperature sensors available in the tiny SOT23-6 package. Requiring no external components, the TMP121 and TMP123 are capable of measuring temperatures within 2°C of accuracy over a temperature range of –40°C to 125°C. Low supply current and a supply range from 2.7 V to 5.5 V make the TMP121 and TMP123 excellent candidates for low-power applications.

The TMP121 and TMP123 are ideal for extended thermal measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.



TMP121

NC = No Connection(1)



TMP123

NC = No Connection(1)

(1) Pins Labeled NC should be left floating or connected to GND.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_A	PACKAGE-LEAD	ORDERABLE PART NUMBER	PACKAGE MARKING
–40°C to 125°C	SOT23-6 (DBV) Reel of 3000	TMP121AQDBVREP	121E
		TMP123AQDBVREP(1)	123E

(1) Product Preview

ABSOLUTE MAXIMUM RATINGS(1)

		UNIT
V+	Power supply	7 V
	Input voltage(2)	–0.3 V to 7 V
	Input current	10 mA
	Operating temperature range	–55°C to 150°C
	Storage temperature range	–60°C to 150°C
T_J max	Junction temperature	150°C
	Lead temperature (soldering)	300°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input voltage rating applies to all TMP121 and TMP123 input voltages.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to 125°C and V+ = 2.7 V to 5.5 V, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT						
	Range		–40		125	°C
	Accuracy (temperature error)	–25°C to 85°C		±0.5	±1.5	°C
		–40°C to 125°C		±1	±2	
		–40°C to 150°C		±1.5		
	Accuracy vs Supply			0.1		°C/V
	Resolution			±0.0625		°C
DIGITAL INPUT/OUTPUT						
V_{IH}	Input logic levels		0.7(V+)			V
V_{IL}					0.3(V+)	
I_{IN}	Input current, SO, SCK, $\overline{CS}$	0 V ≤ V_{IN}≤ V+			±1	µA
V_{OL} SO	Output logic levels	I_{SINK} = 3 mA			0.4	V
V_{OH} SO		I_{SOURCE} = 2 mA	(V+)–0.4			
	Resolution			12		Bits
	Input capacitance, SO, SCK, $\overline{CS}$			2.5		pF
	Conversion time	12-Bit		240	320	ms
	Conversion period(1)	12-BIt		480	640	ms
POWER SUPPLY						
	Operating range		2.7		5.5	V
I_Q	Quiescent current	Serial bus inactive		35	50	µA
I_{SD}	Shutdown current (TPM121)	Serial bus inactive		0.1	1	µA
I_{SD}	Shutdown current (TMP123)	Serial bus inactive		0.1	3	µA
TEMPERATURE RANGE						
	Specified range		–40		125	°C
	Operating range		–55		150	°C
	Storage range		–60		150	°C
θ_{JA}	Thermal resistance	SOT23-6 surface-mount		200		°C/W

(1) Period indicates time between conversion starts.

PIN CONFIGURATIONS

Top View **SOT23-6**

Pin 1 orientation is determined by package marking.

(1) Pin 1 of the SOT23-6 package is determined by orienting the package marking as shown.

(2) Pins labeled NC should be left floating or connected to GND.

TYPICAL CHARACTERISTICS

At T_A = 25°C and V+ = 5 V, unless otherwise noted.

QUIESCENT CURRENT vs TEMPERATURE

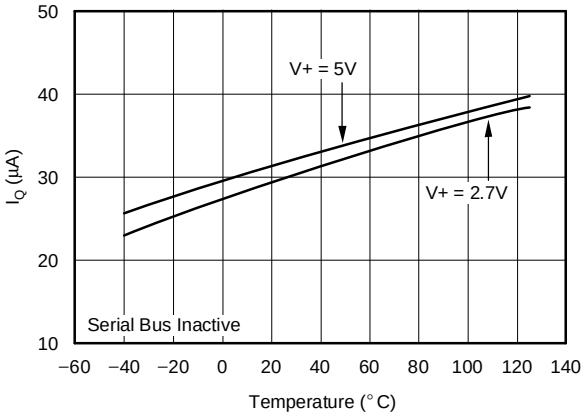


Figure 1.

SHUTDOWN CURRENT vs TEMPERATURE

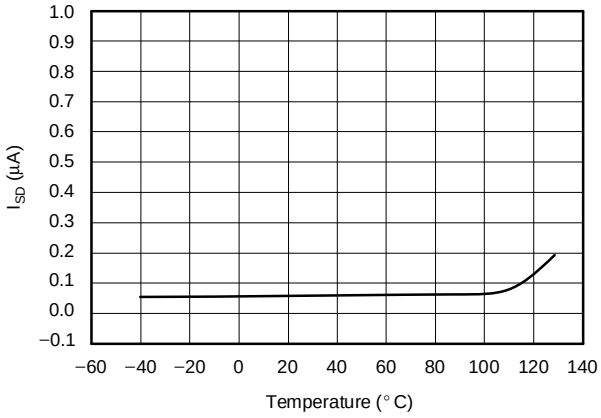


Figure 2.

CONVERSION TIME vs TEMPERATURE

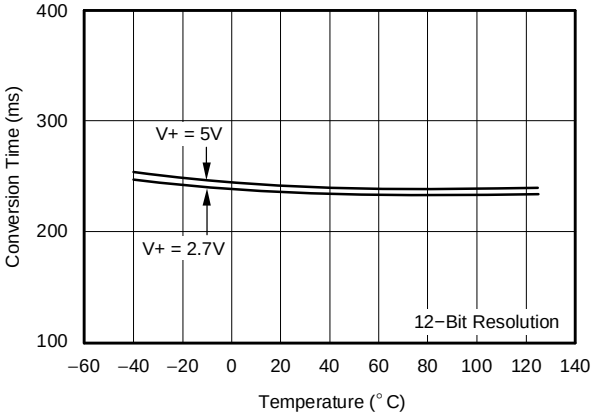


Figure 3.

TEMPERATURE ACCURACY vs TEMPERATURE

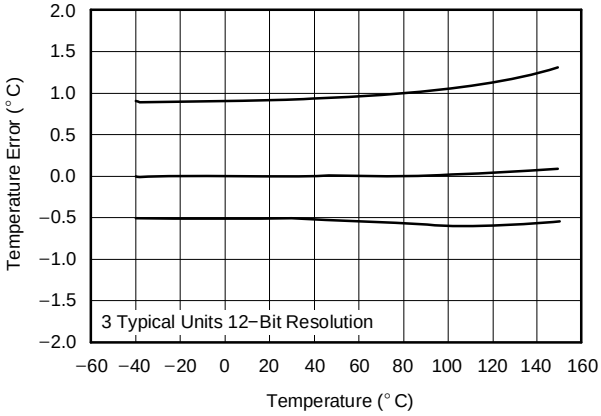


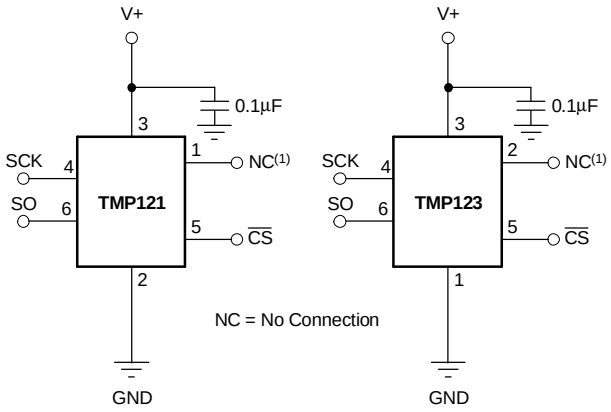
Figure 4.

APPLICATION INFORMATION

The TMP121 and TMP123 are 12-bit plus sign read-only digital temperature sensors optimal for thermal management and thermal protection applications. The TMP121 and the TMP123 communicate through a serial interface that is SPI-compatible. Temperature is converted to a 12-bit plus sign data word with 0.0625°C resolution. The TMP121 and TMP123 are specified for a temperature range of –40°C to 125°C, with operation extending from –55°C to 150°C.

The TMP121 and TMP123 are optimal for low power applications, with a 0.5 s conversion period for reduced power consumption. The TMP121 and TMP123 are specified for a supply voltage range of 2.7 V to 5.5 V, and also feature a hardware shutdown to provide additional power savings.

The TMP121 and TMP123 require no external components for operation, though a 0.1-µF supply bypass capacitor is recommended. Figure 5 shows typical connections for the TMP121 and TMP123.



NOTE: Pins labeled NC should be left floating or connected to GND.

Figure 5. Typical Connections of the TMP121 and TMP123

The sensing device of both the TMP121 and TMP123 is the chip itself; the die flag of the lead frame is thermally connected to pin 2 of the TMP121 and of the TMP123. Thermal paths run through the package leads as well as the plastic package, and the lower thermal resistance of metal causes the leads to provide the primary thermal path. The GND pin (pin 2) of the TMP121 and the NC pin (pin 2) of the TMP123 are thermally connected to the metal lead frame and are the best choice for thermal input.

To maintain accuracy in applications requiring air or surface temperature measurement, care should be taken to isolate the package and leads from ambient air temperature.

APPLICATION INFORMATION (continued)

TEMPERATURE REGISTER

The temperature register of the TMP121 and TMP123 is a 16 bit, signed read-only register that stores the output of the most recent conversion. Up to 16 bits can be read to obtain data and are described in Table 1. The first 13 bits are used to indicate temperature with bits D2 = 0 and D1, D0 in a high impedance state. Data format for temperature is summarized in Table 2. Following power-up or reset, the temperature register reads 0°C until the first conversion is complete.

Table 1. Temperature Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	0	Z	Z

Table 2. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT(1) (BINARY)	HEX
150	0100 1011 0000 0000	4B00
125	0011 1110 1000 0000	3E80
25	0000 1100 1000 0000	0C80
0.0625	0000 0000 0000 1000	0008
0	0000 0000 0000 0000	0000
–0.0625	1111 1111 1111 1000	FFF8
–25	1111 0011 1000 0000	F380
–55	1110 0100 1000 0000	E480

(1) The last two bits are high impedance and are shown as 00 in the table.

COMMUNICATING WITH THE TMP121

The TMP121 and TMP123 continuously convert temperatures to digital data while $\overline{CS}$ is high. $\overline{CS}$ must be high for a minimum of one conversion time (320 ms max) to update the temperature data. Reading temperature data from the TMP121 and TMP123 is initiated by pulling $\overline{CS}$ low, which causes any conversion in progress to terminate, and places the device into analog shutdown. Quiescent current is reduced to 1 µA during analog shutdown. Once $\overline{CS}$ is pulled low, temperature data from the last completed conversion prior to dropping $\overline{CS}$ is latched into the shift register and clocked out at SO on the falling SCK edge. The 16-bit data word is clocked out sign bit first, followed by the MSB. Any portion of the 16-bit word can be read before raising $\overline{CS}$. The TMP121 and TMP123 typically require 0.25 s to complete a conversion and consume 50 µA of current during this period. If $\overline{CS}$ is held high for longer than one conversion time period the TMP121 and TMP123 goes into idle mode for 0.25 s, requiring only 20 µA of current. A new conversion begins every 0.5 s. Figure 6 describes the conversion timing for the TMP121 and TMP123.

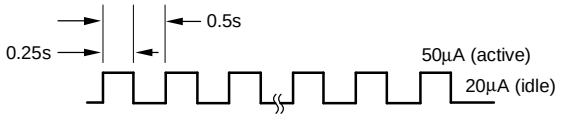


Figure 6. Conversion Time and Period

The serial data of the TMP121 and TMP123 consists of 12-bit plus sign temperature data followed by a confirmation bit and two high impedance bits. Data is transmitted in binary two's complement format. Figure 7 describes the output data of the TMP121 and TMP123.

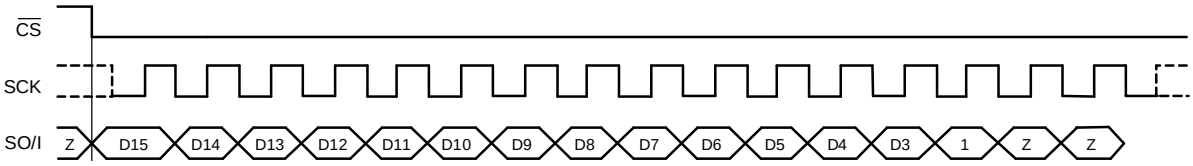


Figure 7. Data READ

Timing Diagrams

The TMP121 and TMP123 are SPI-compatible. Figure 8 and Figure 9 describe the various timing requirements, with parameters defined in Table 3.

Table 3. Timing Description

		MIN	MAX	UNIT
t_1	SCK period	100		ns
t_2	SCK falling edge to output data delay		30	ns
t_3	$\overline{CS}$ to rising edge SCK set-up time	40		ns
t_4	$\overline{CS}$ to output data delay		30	ns
t_5	$\overline{CS}$ rising edge to output high impedance		30	ns

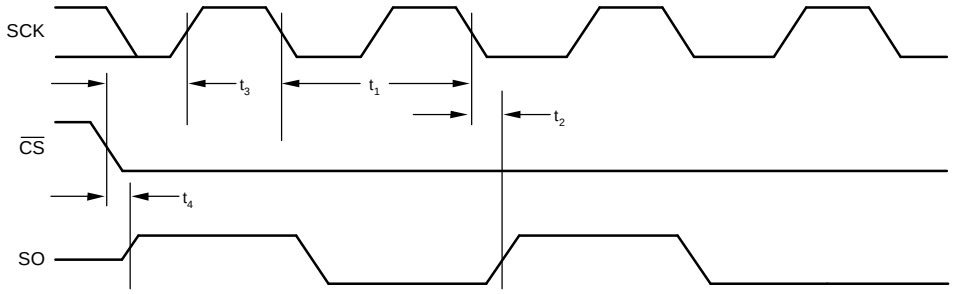


Figure 8. Output Data Timing Diagram

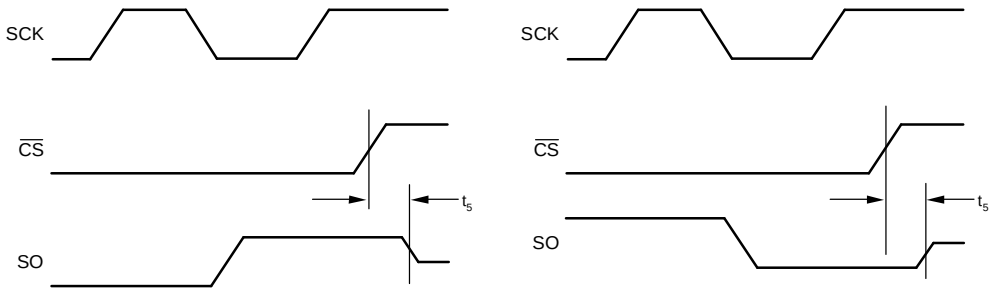


Figure 9. High Impedance Output Timing Diagram

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP121AQDBVREP	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	121E	Samples
V62/06608-01XE	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	121E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TMP121-EP :

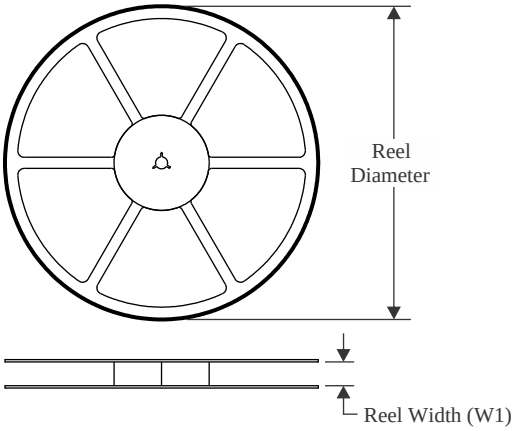
- Catalog: TMP121

NOTE: Qualified Version Definitions:

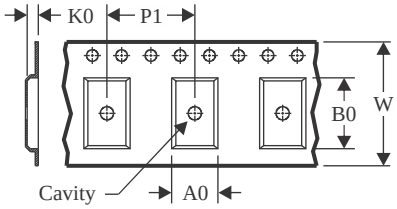
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

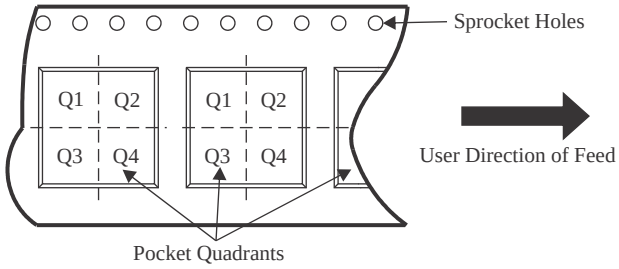


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

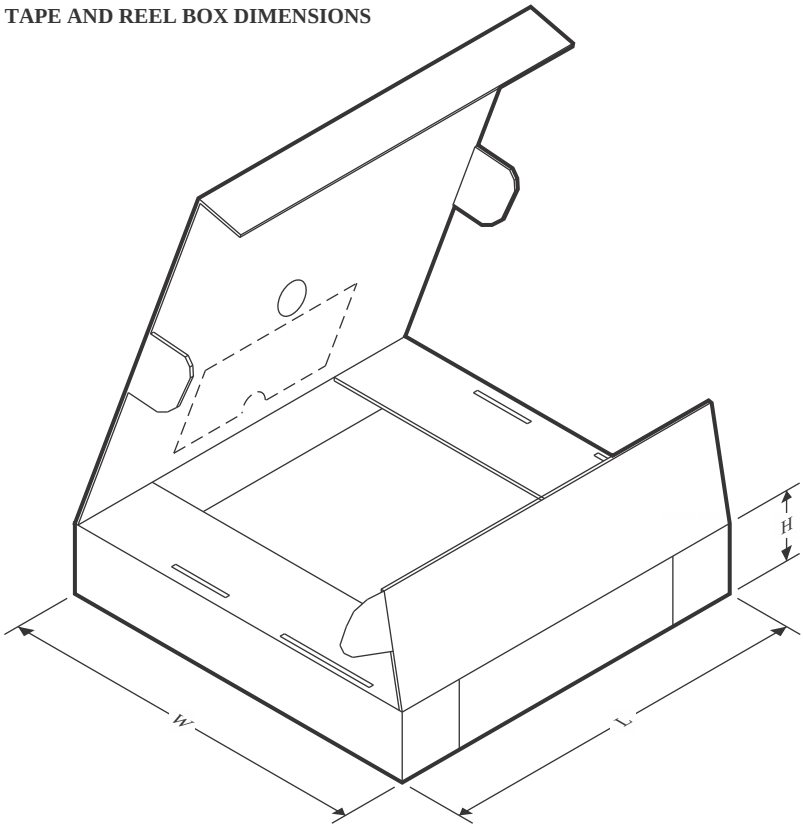
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP121AQDBVREP	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

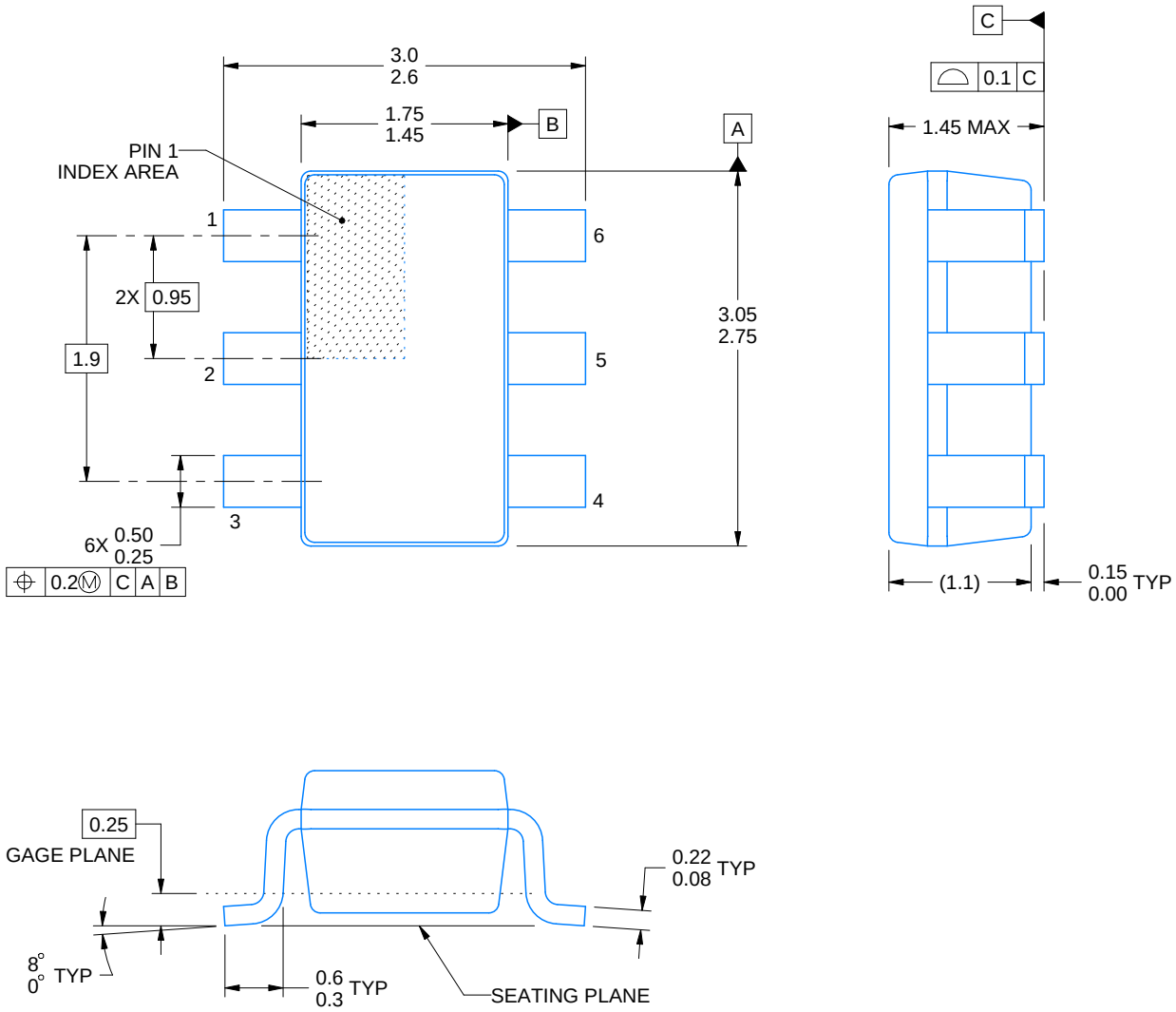
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP121AQDBVREP	SOT-23	DBV	6	3000	213.0	191.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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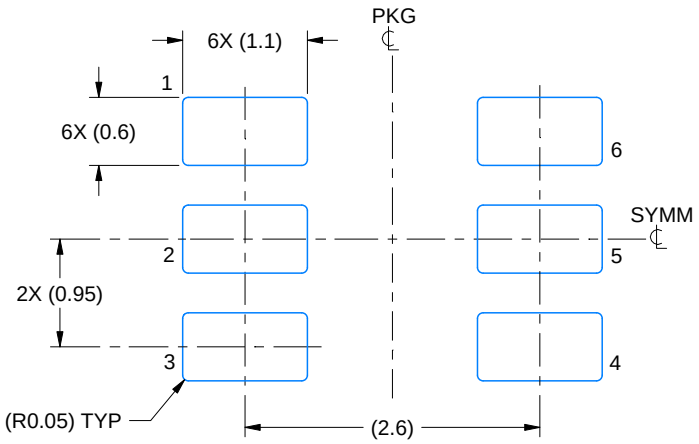
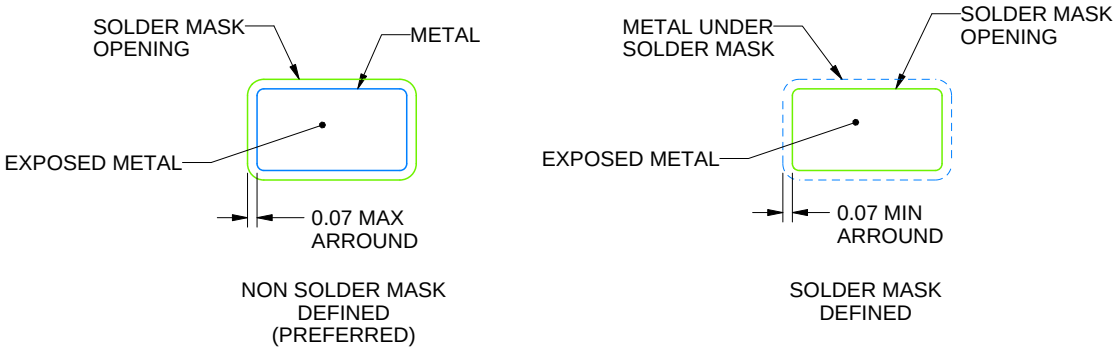
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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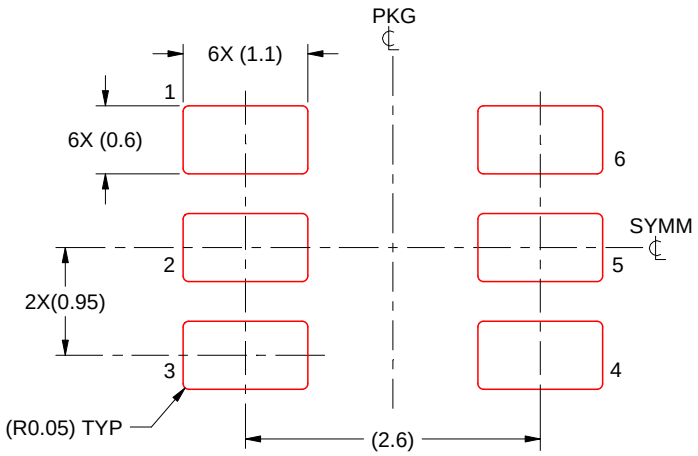
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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