PRODUCT INFORMATION LETTER

PIL IPG-DIS/14/8617
Dated 29 Jul 2014

Assembly and Testing transfer from the ST plant of

Longgang to ST Shenzhen

and introduction of the leads electroplating finishing

Sales Type/product family label	STTH60P03SW
Type of change	Package assembly location change
Reason for change	To provide a better service and standardize the manufacturing process
Description	Continuing in the already announced plan of consolidating the assembly and testing activities for the products housed in TO-247 and DO247 packages, ST is glad to announce the transfer of the production lines from the ST plant of Longgang to the ST plant of Shenzhen.
Forecasted date of implementation	11-Aug-2014
Forecasted date of samples for customer	18-Aug-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	22-Jul-2014
Involved ST facilities	ST assembly plant in China

DOCUMENT APPROVAL

Name	Function
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STMicroelectronics
IPG - ASD & IPAD™ Division[1]
BU Thyristors and Triacs

(1) IPG: Industrial & Power Group - ASD: Application Specific Device – IPAD™: Integrated Passive and Active Devices

PIL
Product/Process Information Letter

Assembly and Testing transfer from the ST plant of Longgang to ST Shenzhen and introduction of the leads electroplating finishing

Notification number:	IPG-DIS/14/8617	**Issue Date**	21/07/2014
Issued by	Aline AUGIS		
Product series affected by the change		STTH60P03SW	

Reason for change

To provide a better service to our customers and standardize manufacturing processes for the power packages typology.

Effects of change

Continuing in the already announced plan of consolidating the assembly and testing activities for the products housed in TO-247 and DO247 packages, ST is glad to announce the transfer of the production lines from the ST plant of Longgang to the ST plant of Shenzhen.

The change will also benefit of the standardization for those packages of the electroplating process.

The changed here reported will not affect the electrical, dimensional and thermal parameters, keeping unchanged all information reported on the relevant product's datasheets.
There are as well neither modification in the packing modes nor in the standard delivery quantities.

Product identification and traceability

Unless otherwise stated by customer specific requirement, the traceability of the parts produced in ST Shenzhen will be ensured by the **Q.A. number** and **plant code identification** "GK" marked on the package, as illustrated in the below picture:

Package marking example

Qualification complete date	Week 28 2014

Forecasted sample availability

Samples of the test vehicles products manufactured in the ST plant of Shenzhen are available right now upon request for immediate customer qualification. Concerning STTH60P03SW, samples will be available in **week 34**.

Change implementation schedule

Estimated production start	Estimated first shipments
W33	**W36**

Qualification:	The qualification program consists in a full set of comparative electrical characterization and reliability tests. Please refer to Appendix 1 for all the details.
Comments:	

Reliability Report

Qualification of assembly and testing transfer from Longgang ST plant to Shenzhen ST plant for rectifier products in TO247&DO247 package.

General Information	
Product Description	*Rectifier*
Product Group	*IPG*
Product division	*ASD&IPAD*
Package	*TO-247* *DO-247*
Maturity level step	*Qualified*

Locations	
Wafer fab	*ST TOURS (FRANCE)* *ST AMK (SINGAPORE)*
Assembly plant	*ST SHENZHEN (CHINA)*
Reliability Lab	*ST Tours*
Reliability assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	28/04/2014	8	Aude DROMEL	Jean-Paul REBRASSE	
2.0	22/05/2014	8	Aude DROMEL	Jean-Paul REBRASSE	Automotive grade qualification

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101 rev C	Stress test qualification for automotive grade discrete semiconductors
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices

2 GLOSSARY

DUT	Device Under Test
PTV	Product Test Vehicle
PCB	Printed Circuit Board
SS	Sample Size
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
THB	Temperature Humidity Bias
IOLT	Intermittent Operating Life Test
PCT/AC	Pressure Cooker Test (Autoclave)
RSH	Resistance to Solder Heat
SD	Solderability
DPA	Destructive Physical Analysis

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify the assembly and testing transfer from the ST plant of Longgang to ST plant of Shenzhen for the rectifiers products in TO-247 and DO-247 packages.

The reliability test methodology used follows the JESD47-H: « Stress Test Driven Qualification Methodology ». Rectifier diodes perimeter is covered through 5 different test vehicles including turbo/bipolar diodes and Schottky barrier diodes. These test vehicles have been chosen to include the most critical parameters for reliability (die size, highest voltage, etc.)
The following reliability tests are:

- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- TC and IOLT to ensure the mechanical robustness of the products.
- THB/AC to check the robustness to corrosion and the good package hermeticity.
- RSH and Solderability

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

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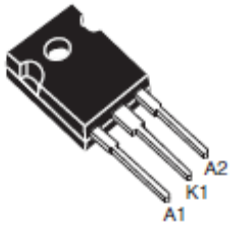
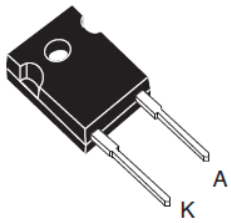
4 DEVICES CHARACTERISTICS

4.1 Devices descriptions

All rectifiers (bipolar, turboswitch, power shottky in silicon and silicon carbide) assembled in TO-247 and DO-247 packages.



TO-247



DO-247

4.2 Construction Note

	STTHxxxxW & STTHxxxxWY
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS FRANCE
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST TOURS FRANCE
Assembly information	
Assembly site	ST SHENZHEN -CHINA
Package description	TO-247 & DO-247
Molding compound	ECOPACK®2 (“Halogen-free”)
Lead finishing material	Tin 100%
Final testing information	
Testing location	ST SHENZHEN CHINA

	STPSxxxxW & STPSxxxxWY
Wafer/Die fab. information	
Wafer fab manufacturing location	ST AMK SINGAPORE or ST TOURS FRANCE
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST AMK SINGAPORE or ST TOURS FRANCE
Assembly information	
Assembly site	ST SHENZHEN -CHINA
Package description	TO-247
Molding compound	ECOPACK®2 (“Halogen-free”)
Lead finishing material	Tin 100%
Final testing information	
Testing location	ST SHENZHEN -CHINA

	STPSCxxxW
Wafer/Die fab. information	
Wafer fab manufacturing location	ST CATANIA ITALY
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST CATANIA ITALY
Assembly information	
Assembly site	ST SHENZHEN -CHINA
Package description	TO-247
Molding compound	ECOPACK®2 ("Halogen-free")
Lead finishing material	Tin 100%
Final testing information	
Testing location	ST SHENZHEN -CHINA

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Part Number	Package	Technology family	Comments
1	STTH100W06CW	TO-247	Rectifier Turboswitch	-Big die -Ribbon bonding
2	STPSC2006CW	TO-247	Power Shottky SiC	-Big die SiC -Dual configuration
3	STTH3012W	DO-247	Rectifier Turboswitch	-Highest voltage -2-leads package
4	STPS80170CW	TO-247	Power Schottky	-Highest voltage Schottky -Big die -Multi-wires bonding
5	STPS4045CWY	TO-247	Power Schottky	-Low voltage Schottky -Standard Al 20mils bonding

Detailed results in below chapter will refer to these references.

5.2 Test plan and results summary

Test	Std ref.	Conditions	SS	Steps / duration	Failure/SS				
					L1	L2	L3	L4	L5
HTRB	JESD22 A-108	VR = 0.8xVRRM = 960V Tj = 175°C for GD1 150°C for other lots	231	1000h		0/77	0/77	0/77	
THB	JESD22 A-101	85% RH, 85°C VR=100V	231	1000h	0/77	0/77			0/77
DPA after TC (AEC-Q101)			2	N/A	Accep table				
TC	JESD22 A-104	-65 / +150°C 2 cycles/hour	231	1000cy	0/77	0/77		0/77	
DPA after TC (AEC-Q101)			2	N/A	Accep table				
AC	JESD22 A-102	121°C 2bar 100% RH	231	96h	0/77	0/77		0/77	
IOLT	Mil Std 750 method 1037	ΔTc = 85°C $t_{on} = t_{off} = 300s$	231	6kcy	0/77	0/77			0/77
RSH	JESD22 B-106	Oil bath* 245°C 10sec/dip 2 dips	10	N/A	0/10				
SD	ST internal 0018688	Wet ageing + Sn/Pb bath Wet ageing + Sn/Ag/Cu bath	30		0/15 0/15				

*oil bath dipping with all the package dipped is assumed to be more stressing than lead dipping in solder bath in terms if die temperature profile.

6 ANNEXES

6.1 Tests description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
PCT Pressure Cooker Test (Autoclave)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
IOLT Intermittent Operating Life Test	All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly, not gradually, to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors) +15°C, -5°C, followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature. Auxiliary (forced) cooling is permitted during the off period only. Heat sinks are not intended to be used in this test, however, small heat sinks may be used when it is otherwise difficult to control case temperature of test samples, such as with small package types (e.g., TO39).	The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.
RSH Resistance to Solder Heat	Package is dipped by the leads 2 times in a solder bath.	To simulate wave soldering process and verify that package will not be thermally damaged during this step.
SD Solderability	Wet ageing + dipping in a solder bath. Assessment by visual inspection of the leads.	To check package ability to be soldered with no difficulty. To simulate

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