# SN74LVC07A Hex Buffer and Driver With Open-Drain Outputs

## 1 Features

- Operates From 1.65 V to 5 V
- Inputs and Open-Drain Outputs Accept Voltages Up to 5.5 V
- Max $t_{pd}$ of 2.6 ns at 5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- $I_{off}$ Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection

## 2 Applications

- AV Receiver
- Audio Dock: Portable
- Blu-ray Player and Home Theater
- MP3 Player or Recorder
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD, Digital, and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

## 3 Description

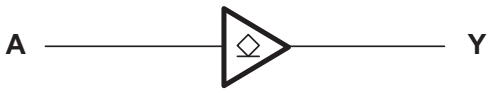
The SN74LVC07A device is a hex buffer and driver that is designed for 1.65-V to 5.5-V $V_{CC}$ operation.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LVC07AD | SOIC (14) | 8.65 mm × 3.91 mm |
| SN74LVC07ADB | SSOP (14) | 6.20 mm × 5.30 mm |
| SN74LVC07ADGV | TVSOP (14) | 3.60 mm × 4.40 mm |
| SN74LVC07APW | TSSOP (14) | 5.00 mm × 4.40 mm |
| SN74LVC07ANS | SO (14) | 10.30 mm × 5.30 mm |
| SN74LVC07ARGY | VQFN (14) | 3.50 mm × 3.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision V (May 2015) to Revision W** — **Page**

- Changed *Pin Functions* table ... 4
- Added Junction temperature to the *Absolute Maximum Ratings* table ... 5
- Reformatted the *Electrical Characteristics* and the *Switching Characteristics* tables ... 6
- Changed *Typical Application Diagram* ... 13
- Added *Receiving Notification of Documentation Updates* section ... 16

**Changes from Revision U (June 2014) to Revision V** — **Page**

- Changed *Handling Ratings* table to *ESD Ratings* table ... 5
- Added industry standard terms to package designators in the *Thermal Information* table ... 6
- Changed from "High" to "High-Z" in the *Function Table* ... 12

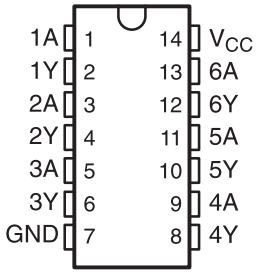
**Changes from Revision T (February 2011) to Revision U** — **Page**

- Updated document to new TI data sheet format ... 1
- Removed *Ordering Information* table ... 1
- Added *Applications* ... 1
- Added $I_{off}$ *Features* bullet ... 1
- Added *Device Information* table ... 1
- Added *Handling Ratings* table. ... 5
- Changed MAX operating free-air temperature from 85°C to 125°C. ... 5
- Updated *Thermal Information* table. ... 6
- Added –40°C TO +125°C temperature range to *Electrical Characteristics* table ... 6
- Added *Switching Characteristics* table for –40°C TO 125°C temperature range ... 6

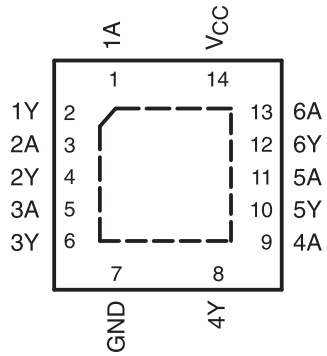
- Added *Typical Characteristics* ..... 7

# 5 Pin Configuration and Functions

**D, DB, DGV, NS, PW Package**
**14-Pin SOIC, SSOP, TVSOP, SO, TSSOP**
**Top View**




**RGY Package**
**14-Pin VQFN**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | 1A | I | Input 1 |
| 2 | 1Y | O | Output 1 |
| 3 | 2A | I | Input 2 |
| 4 | 2Y | O | Output 2 |
| 5 | 3A | I | Input 3 |
| 6 | 3Y | O | Output 3 |
| 7 | GND | — | Ground pin |
| 8 | 4Y | O | Output 4 |
| 9 | 4A | I | Input 4 |
| 10 | 5Y | O | Output 5 |
| 11 | 5A | I | Input 5 |
| 12 | 6Y | O | Output 6 |
| 13 | 6A | I | Input 6 |
| 14 | $V_{CC}$ | — | Power pin |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage(2) | | –0.5 | 6.5 | V |
| $V_O$ | Output voltage | | –0.5 | 6.5 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_j$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±4000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.65 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0.7 × $V_{CC}$ | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 0.3 × $V_{CC}$ | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | 5.5 | V |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 12 | |
| | | $V_{CC}$ = 2.7 V | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | |
| | | $V_{CC}$ = 4.5 V | | 24 | |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

## 6.4 Thermal Information

| THERMAL METRIC[1] | | SN74LVC07A | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | D (SOIC) | DB (SSOP) | DGV (TVSOP) | NS (SO) | PW (TSSOP) | RGY (VQFN) | |
| | | 14 PINS | | | | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 177.4 | 135.1 | 157.7 | 120.3 | 160.3 | 80.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 75.4 | 86.7 | 78.3 | 76.3 | 84.4 | 97.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 70.6 | 82.4 | 90.8 | 79.0 | 102.1 | 56.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 34.7 | 43.7 | 21.0 | 36.2 | 24.3 | 16.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 70.4 | 81.9 | 90.1 | 78.7 | 101.4 | 56.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | n/a | n/a | n/a | 35.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics—DC Limit Changes

$T_A$ = –40°C to +125°C, unless otherwise noted

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OL}$ | $I_{OL}$ = 100 µA | 1.65 V to 5.5 V | | | 0.2 | V |
| | $I_{OL}$ = 4 mA | 1.65 V | | | 0.45 | |
| | $I_{OL}$ = 12 mA | 2.3 V | | | 0.7 | |
| | | 2.7 V | | | 0.4 | |
| | $I_{OL}$ = 24 mA | 3 V | | | 0.55 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 3.6 V | | | ±5 | µA |
| $I_{off}$ | $V_I$ or $V_O$ = 5.5 V | 0 V | | | ±10 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 3.6 V | | | 10 | µA |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | 2.7 V to 3.6 V | | | 500 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 5.0 | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3 through Figure 6)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pd}$ | A | Y | –40°C to 85°C | $V_{CC}$ = 1.8 V ± 0.15 V | 1 | 5.6 | ns |
| | | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1 | 3.4 | |
| | | | | $V_{CC}$ = 2.7 V | 1 | 3.3 | |
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 3.6 | |
| | | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 2.6 | |
| | | | –40°C to 125°C | $V_{CC}$ = 1.8 V ± 0.15 V | 1 | 6.1 | |
| | | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1 | 3.9 | |
| | | | | $V_{CC}$ = 2.7 V | 1 | 3.8 | |
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 4.1 | |
| | | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 3.1 | |

## 6.7 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | $V_{CC}$ = 5 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance per buffer and driver | f = 10 MHz | 1.8 | 2 | 2.5 | 3.78 | pF |

## 6.8 Typical Characteristics

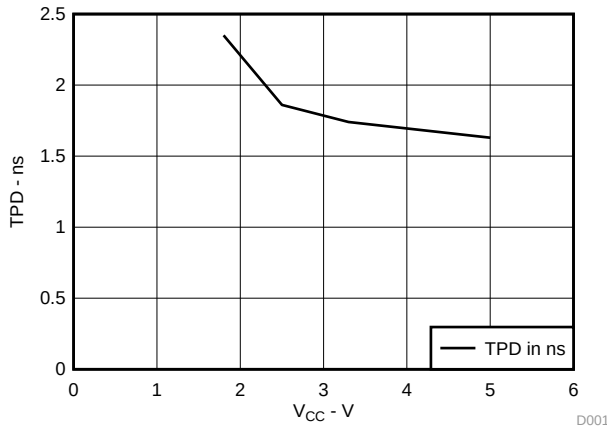



**Figure 1. TPD vs $V_{CC}$**

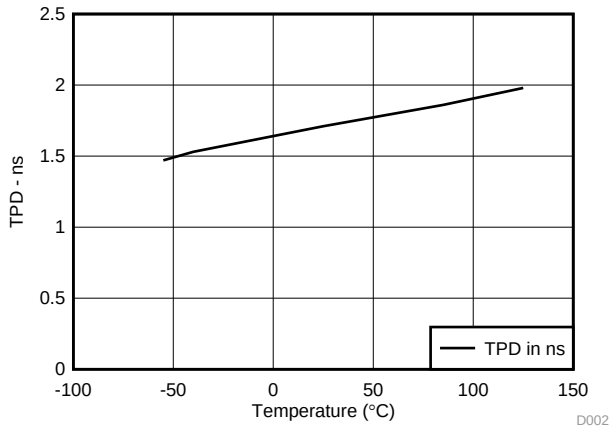
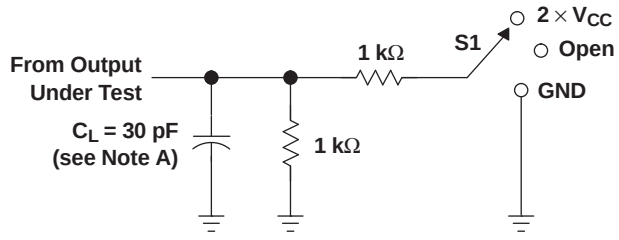



**Figure 2. TPD vs Temperature**

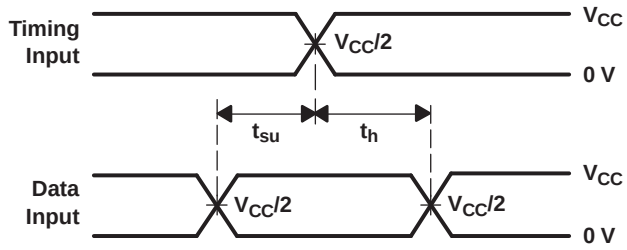
# 7 Parameter Measurement Information

## 7.1 $V_{CC}$ = 1.8 V ± 0.15 V

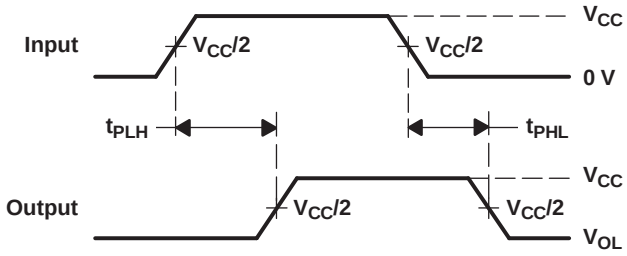



LOAD CIRCUIT

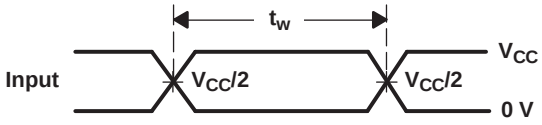
| TEST | S1 |
|---|---|
| $t_{PZL}$ (see Note F) | 2 × $V_{CC}$ |
| $t_{PLZ}$ (see Note G) | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | 2 × $V_{CC}$ |



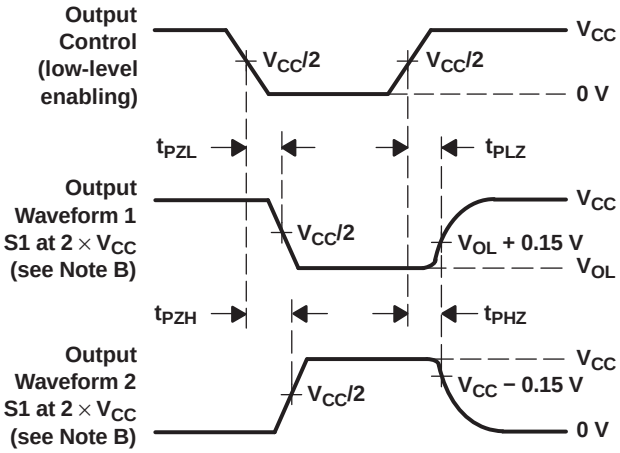

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

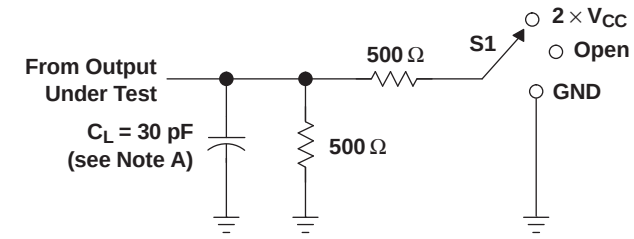



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. Since this device has open-drain outputs, $t_{PLZ}$ and $t_{PZL}$ are the same as $t_{pd}$.
F. $t_{PZL}$ is measured at $V_{CC}/2$.
G. $t_{PLZ}$ is measured at $V_{OL}$ + 0.15 V.
H. All parameters and waveforms are not applicable to all devices.

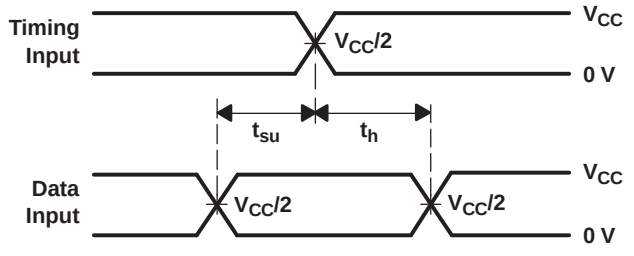
**Figure 3. Load Circuit and Voltage Waveforms**

## 7.2 $V_{CC}$ = 2.5 V ± 0.2 V

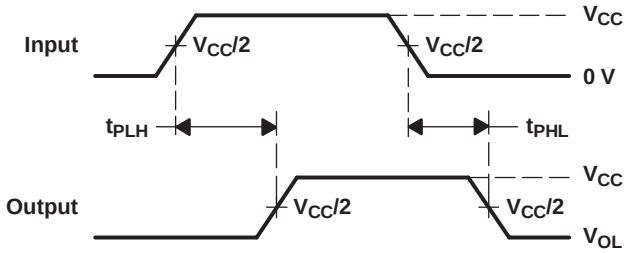



LOAD CIRCUIT

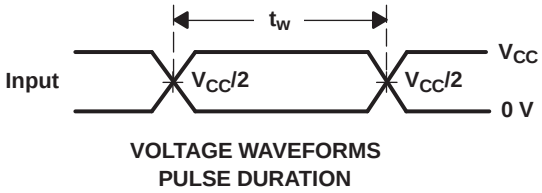
| TEST | S1 |
|---|---|
| $t_{PZL}$ (see Note F) | 2 × $V_{CC}$ |
| $t_{PLZ}$ (see Note G) | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | 2 × $V_{CC}$ |



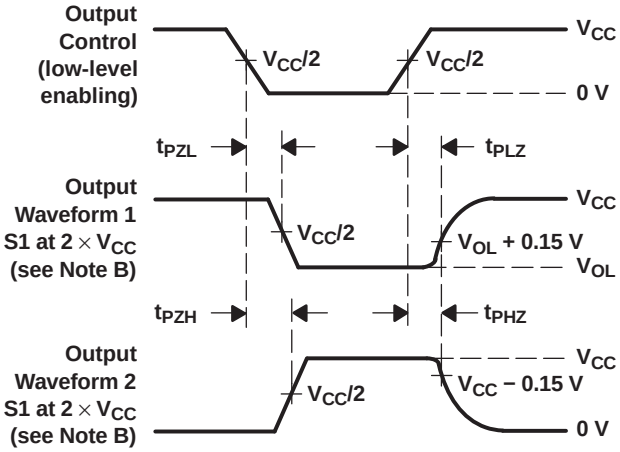

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

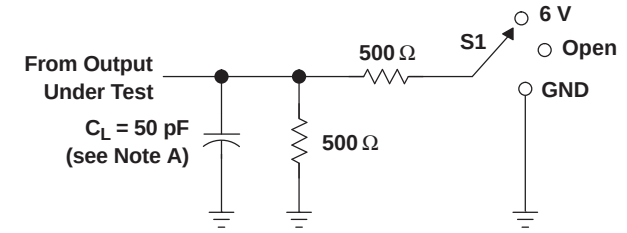



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. Since this device has open-drain outputs, $t_{PLZ}$ and $t_{PZL}$ are the same as $t_{pd}$.
F. $t_{PZL}$ is measured at $V_{CC}/2$.
G. $t_{PLZ}$ is measured at $V_{OL}$ + 0.15 V.
H. All parameters and waveforms are not applicable to all devices.

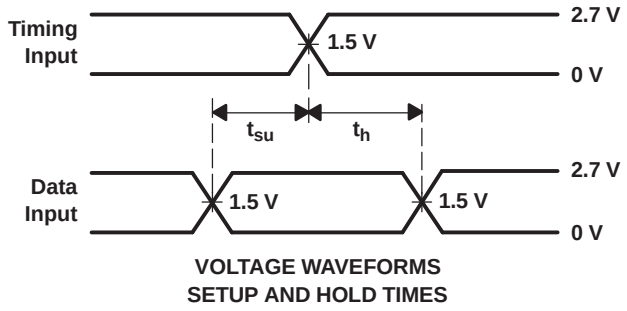
**Figure 4. Load Circuit and Voltage Waveforms**

## 7.3 $V_{CC}$ = 2.7 and 3.3 V ± 0.3 V

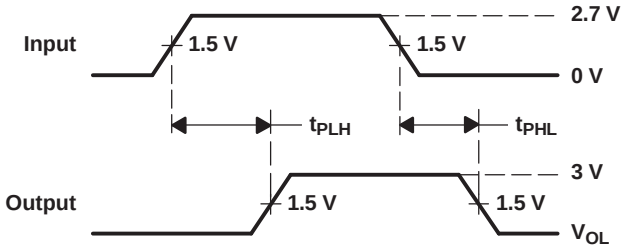



LOAD CIRCUIT

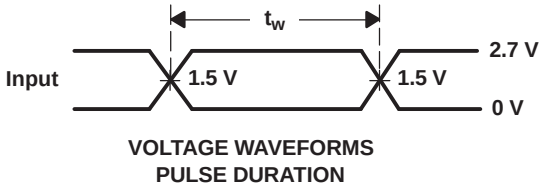
| TEST | S1 |
|---|---|
| $t_{PZL}$ (see Note F) | 6 V |
| $t_{PLZ}$ (see Note G) | 6 V |
| $t_{PHZ}/t_{PZH}$ | 6 V |



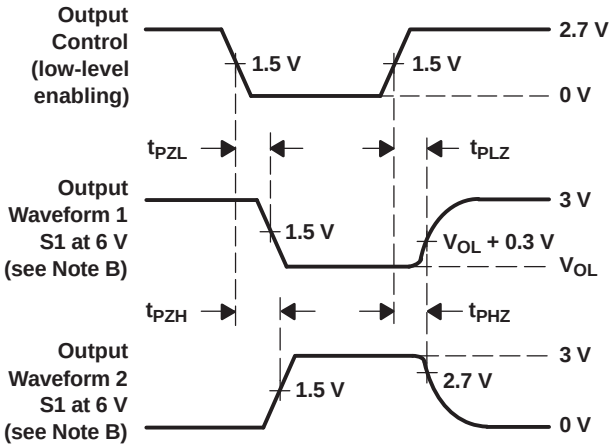

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

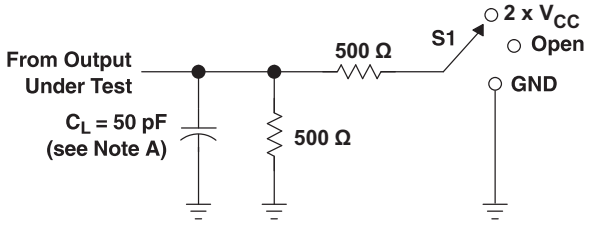



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. Since this device has open-drain outputs, $t_{PLZ}$ and $t_{PZL}$ are the same as $t_{pd}$.
F. $t_{PZL}$ is measured at 1.5 V.
G. $t_{PLZ}$ is measured at $V_{OL}$ + 0.3 V.
H. All parameters and waveforms are not applicable to all devices.

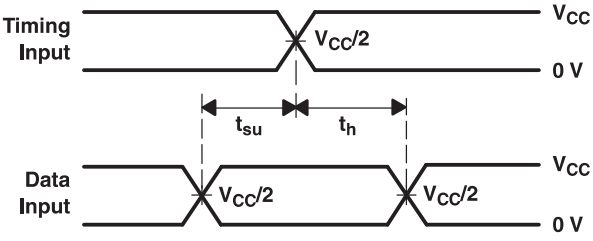
**Figure 5. Load Circuit and Voltage Waveforms**

## 7.4 $V_{CC}$ = 5 V ± 0.5 V

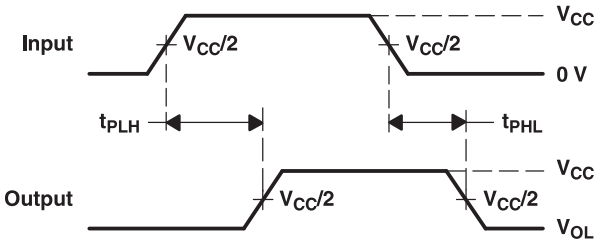



| TEST | S1 |
|---|---|
| $t_{PZL}$ (see Note F) | 2 x $V_{CC}$ |
| $t_{PLZ}$ (see Note G) | 2 x $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | 2 x $V_{CC}$ |

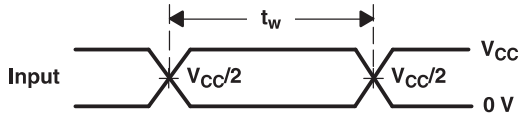
LOAD CIRCUIT



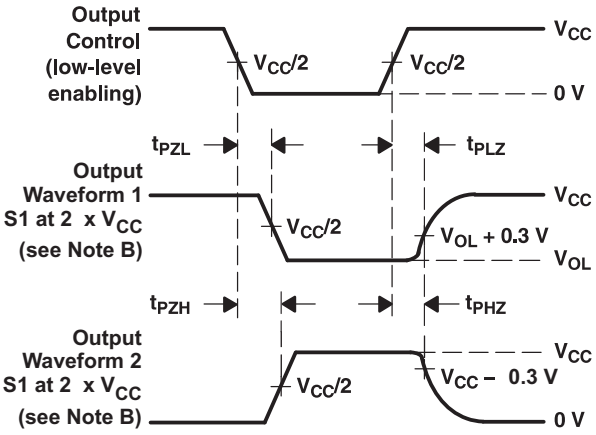

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal connections such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal connections such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. Since this device has open-drain outputs, $t_{PLZ}$ and $t_{PZL}$ are the same as $t_{pd}$.
F. $t_{PZL}$ is measured at $V_{CC}/2$.
G. $t_{PLZ}$ is measured at $V_{OL}$ + 0.3 V.
H. All parameters and waveforms are not applicable to all devices.

**Figure 6. Load Circuit and Voltage Waveforms**

# 8 Detailed Description

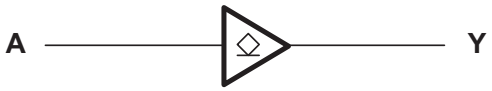
## 8.1 Overview

The outputs of the SN74LVC07A device are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

Inputs can be driven from 1.8-V, 2.5-V, 3.3-V (LVTTL), or 5-V (CMOS) devices. This feature allows the use of this device as translators in a mixed-system environment.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## 8.2 Functional Block Diagram






## 8.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65 V to 5.5 V
- Allows up or down voltage translation
  - Inputs and outputs accept voltages to 5.5 V
- $I_{off}$ feature
  - Allows voltages on the inputs and outputs when $V_{CC}$ is 0 V

## 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC07A.

**Table 1. Function Table**

| INPUT A | OUTPUT Y |
|---|---|
| H | Hi-Z |
| L | L |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LVC07A device is a high-drive, open-drain CMOS device that can be used for a multitude of buffer-type functions. It can produce 24 mA of drive current at 3.3 V. Therefore, this device is ideal for driving multiple inputs and for high-speed applications up to 100 MHz. The inputs and outputs are 5.5-V tolerant allowing the device to translate up to 5.5 V or down to $V_{CC}$.

## 9.2 Typical Application

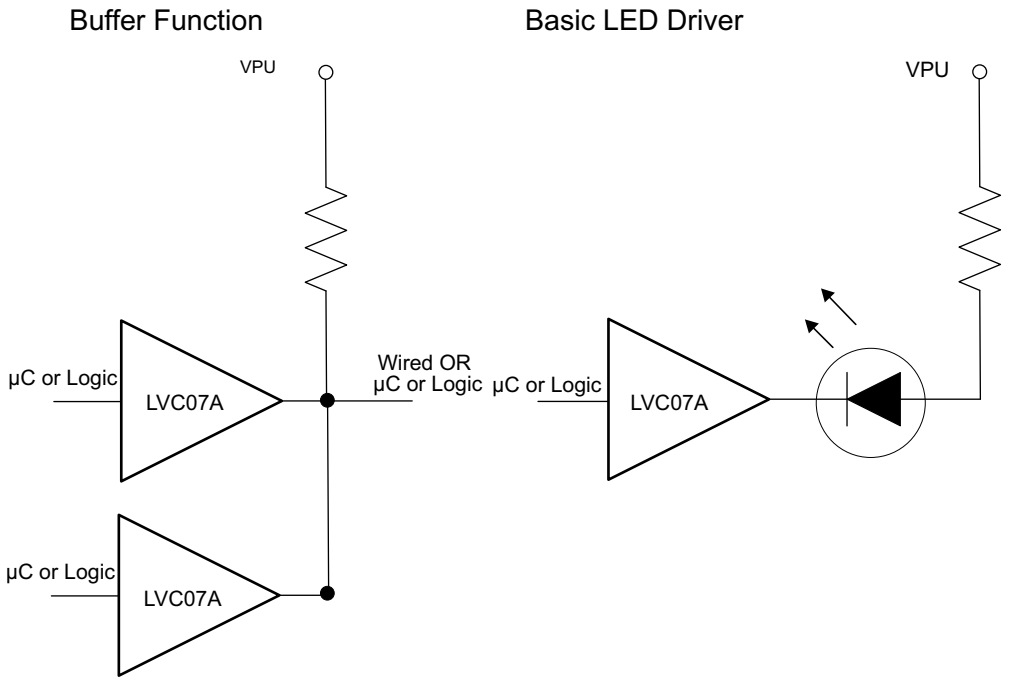



**Figure 7. Typical Application Diagram**

### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions must be considered to prevent ringing.

### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs: See ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
   - Specified high and low levels: See ($V_{IH}$ and $V_{IL}$) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$.
2. Recommended Output Conditions

## Typical Application (continued)

- Load currents must not exceed 25 mA per output and 50 mA total for the part.
- Outputs must not be pulled above 5.5 V.

### 9.2.3 Application Curve

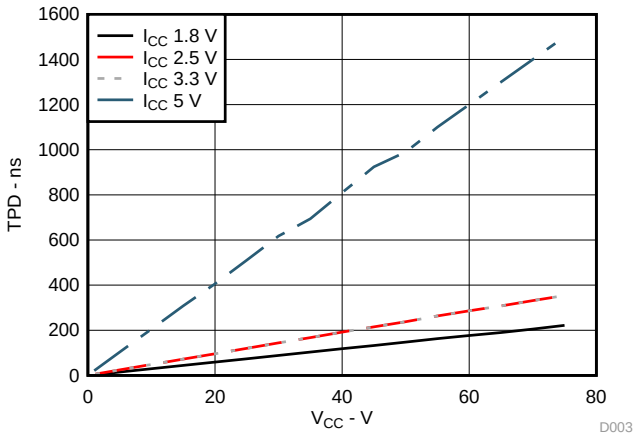



**Figure 8. $I_{CC}$ vs Frequency**

## 10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each $V_{CC}$ pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µf is recommended; if there are multiple $V_{CC}$ pins, then 0.01 µf or 0.022 µf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µf and a 1 µf are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 9 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

## 11.2 Layout Example

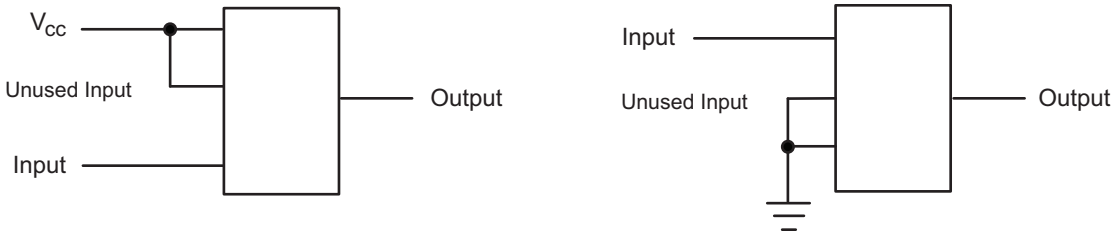



**Figure 9. Layout Diagram**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs*, SCBA004.
- *Semiconductor and IC Package Thermal Metrics*, SPRA953.

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC07AD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC07A | Samples |
| SN74LVC07ADBR | ACTIVE | SSOP | DB | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC07A | Samples |
| SN74LVC07ADBRG4 | ACTIVE | SSOP | DB | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC07A | Samples |
| SN74LVC07ADE4 | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC07A | Samples |
| SN74LVC07ADGVR | ACTIVE | TVSOP | DGV | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC07A | Samples |
| SN74LVC07ADR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LVC07A | Samples |
| SN74LVC07ADRG3 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LVC07A | Samples |
| SN74LVC07ADRG4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC07A | Samples |
| SN74LVC07ADT | ACTIVE | SOIC | D | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC07A | Samples |
| SN74LVC07ANSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC07A | Samples |
| SN74LVC07APW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC07A | Samples |
| SN74LVC07APWE4 | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC07A | Samples |
| SN74LVC07APWG4 | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC07A | Samples |
| SN74LVC07APWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LC07A | Samples |
| SN74LVC07APWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC07A | Samples |
| SN74LVC07APWRG3 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LC07A | Samples |
| SN74LVC07APWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC07A | Samples |
| SN74LVC07APWT | ACTIVE | TSSOP | PW | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC07A | Samples |
| SN74LVC07APWTG4 | ACTIVE | TSSOP | PW | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC07A | Samples |
| SN74LVC07ARGYR | ACTIVE | VQFN | RGY | 14 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC07A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC07ARGYRG4 | ACTIVE | VQFN | RGY | 14 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC07A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN74LVC07A :**

- Automotive: SN74LVC07A-Q1

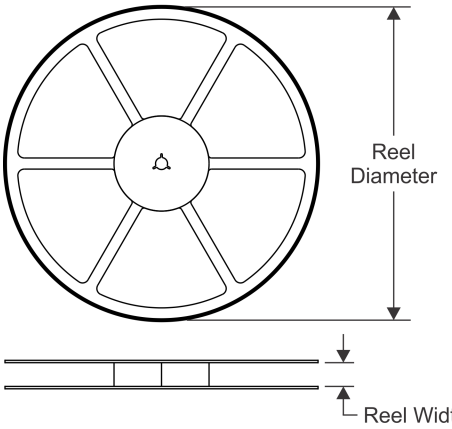
- Enhanced Product: SN74LVC07A-EP

NOTE: Qualified Version Definitions:

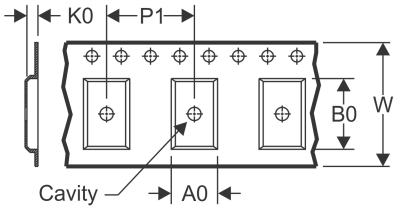
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

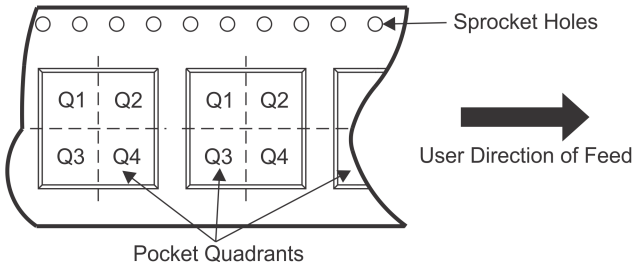



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

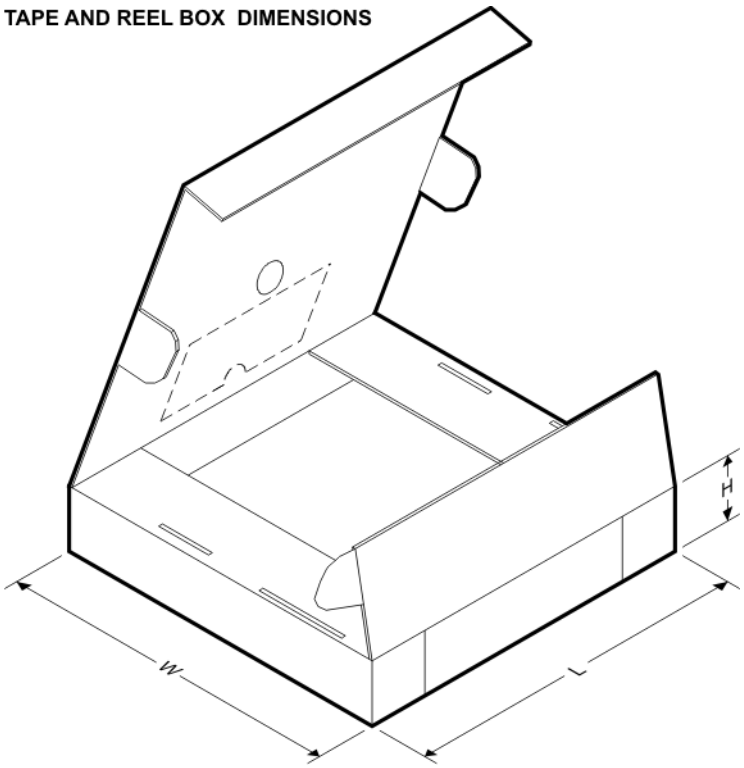
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC07ADBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LVC07ADGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC07ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC07ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC07ADR | SOIC | D | 14 | 2500 | 330.0 | 16.8 | 6.5 | 9.5 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC07ADRG3 | SOIC | D | 14 | 2500 | 330.0 | 16.8 | 6.5 | 9.5 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC07ADRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC07ADRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC07ADT | SOIC | D | 14 | 250 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC07ANSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC07APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC07APWRG3 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC07APWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC07APWT | TSSOP | PW | 14 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC07ARGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

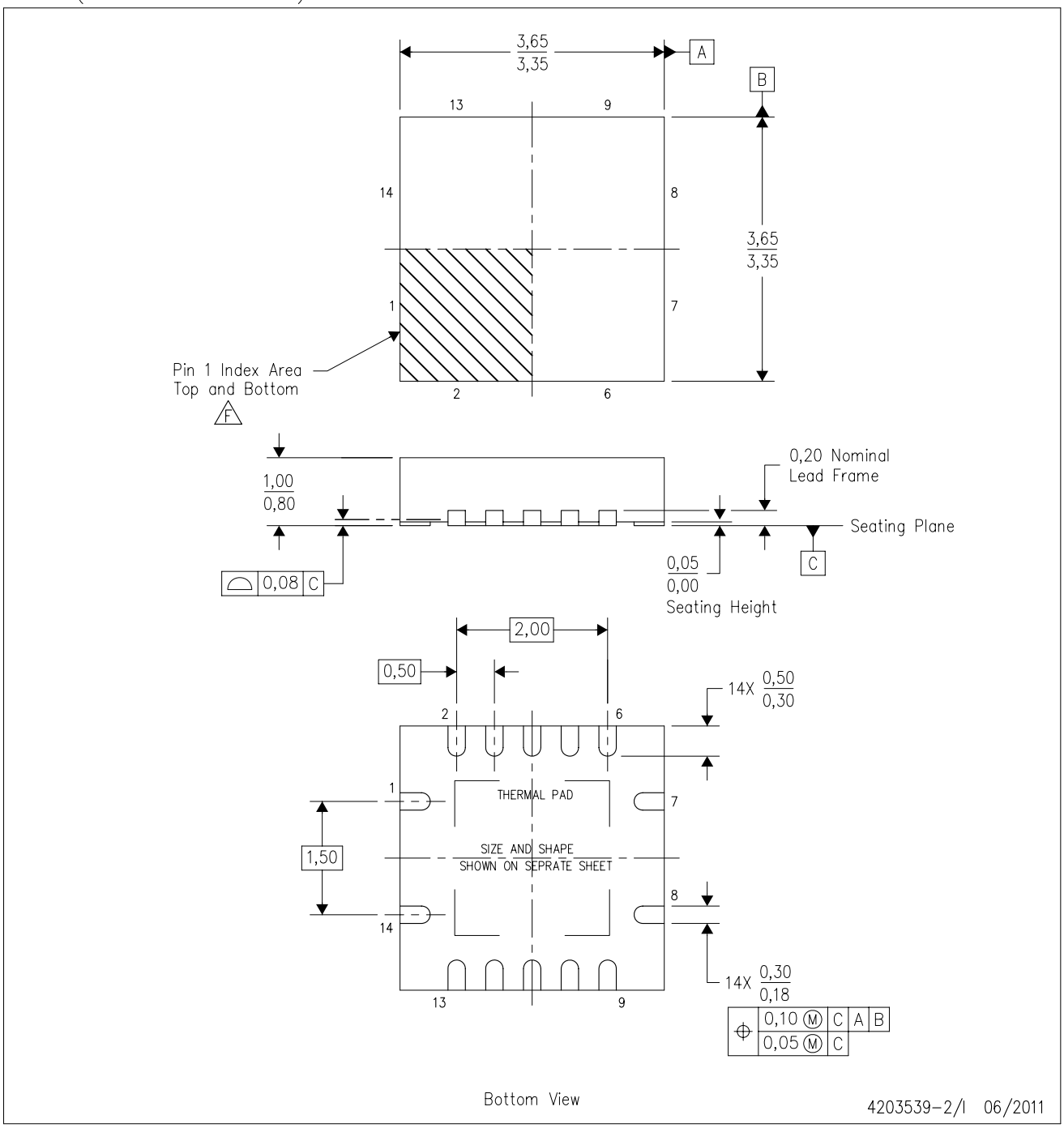
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC07ADBR | SSOP | DB | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LVC07ADGVR | TVSOP | DGV | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LVC07ADR | SOIC | D | 14 | 2500 | 853.0 | 449.0 | 35.0 |
| SN74LVC07ADR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LVC07ADR | SOIC | D | 14 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74LVC07ADRG3 | SOIC | D | 14 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74LVC07ADRG4 | SOIC | D | 14 | 2500 | 853.0 | 449.0 | 35.0 |
| SN74LVC07ADRG4 | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LVC07ADT | SOIC | D | 14 | 250 | 210.0 | 185.0 | 35.0 |
| SN74LVC07ANSR | SO | NS | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LVC07APWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LVC07APWRG3 | TSSOP | PW | 14 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LVC07APWRG4 | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LVC07APWT | TSSOP | PW | 14 | 250 | 853.0 | 449.0 | 35.0 |
| SN74LVC07ARGYR | VQFN | RGY | 14 | 3000 | 853.0 | 449.0 | 35.0 |

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

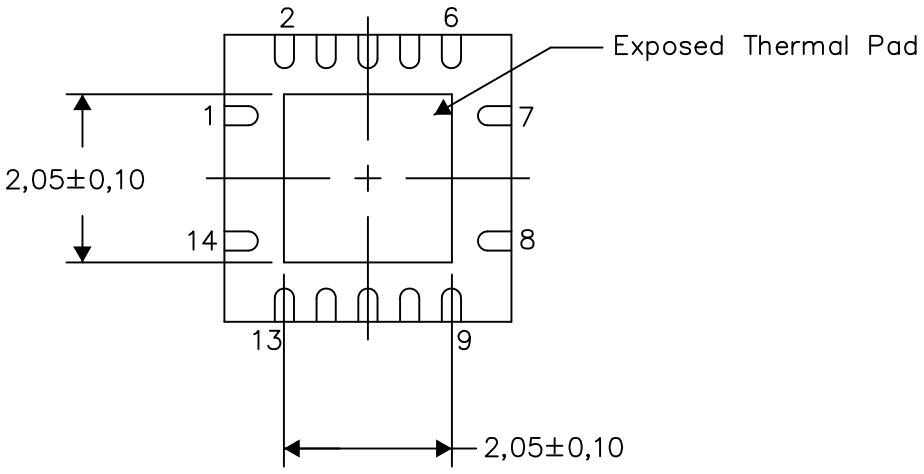
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



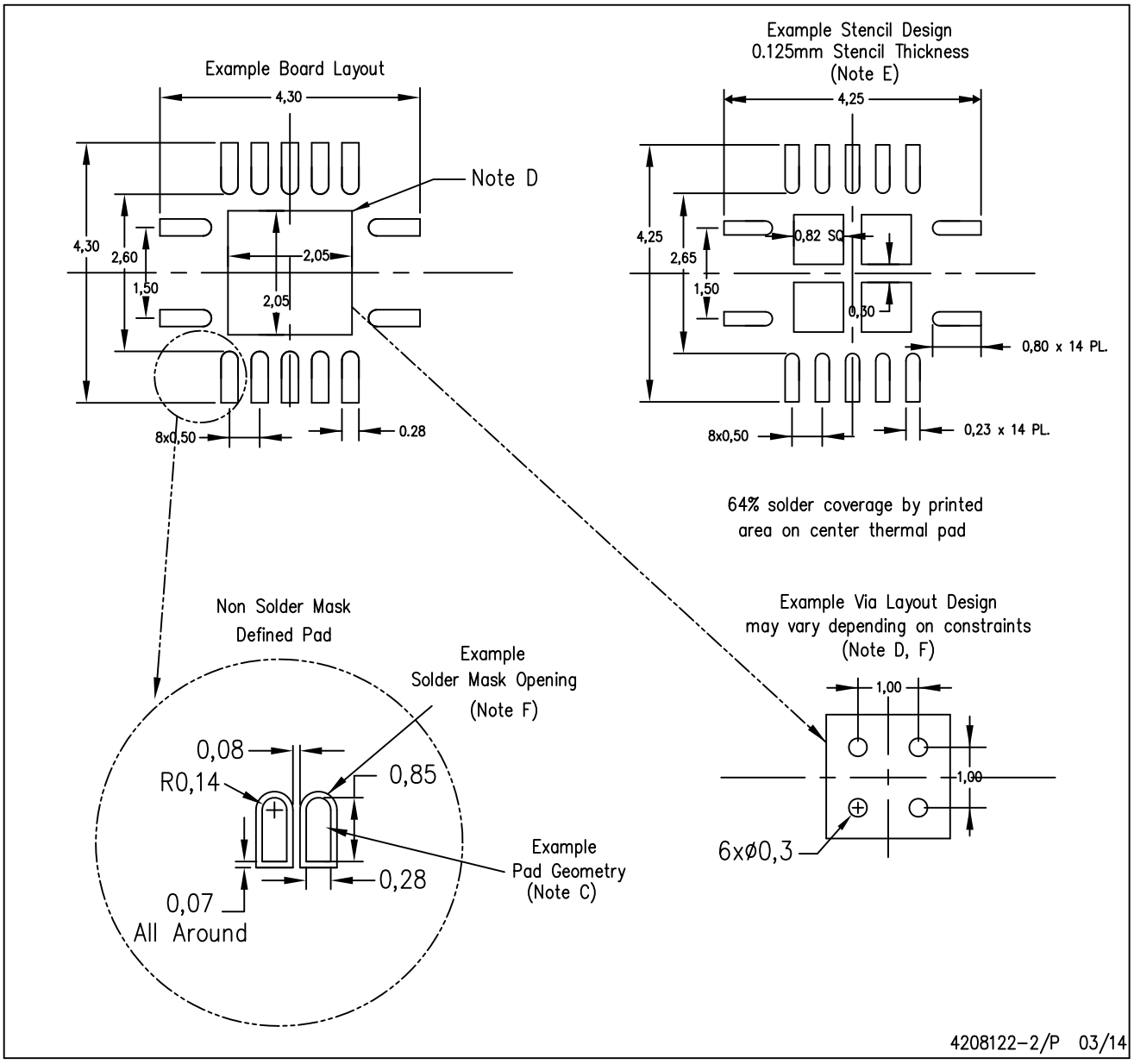

Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

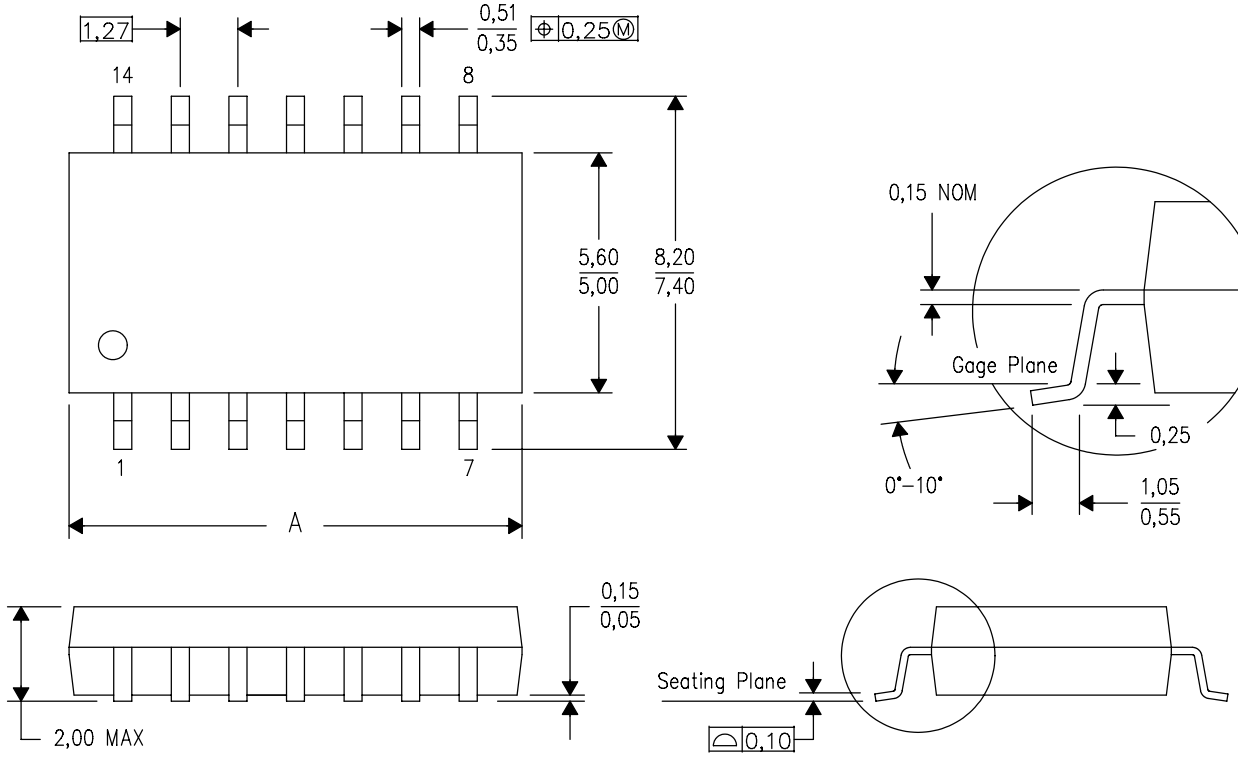



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



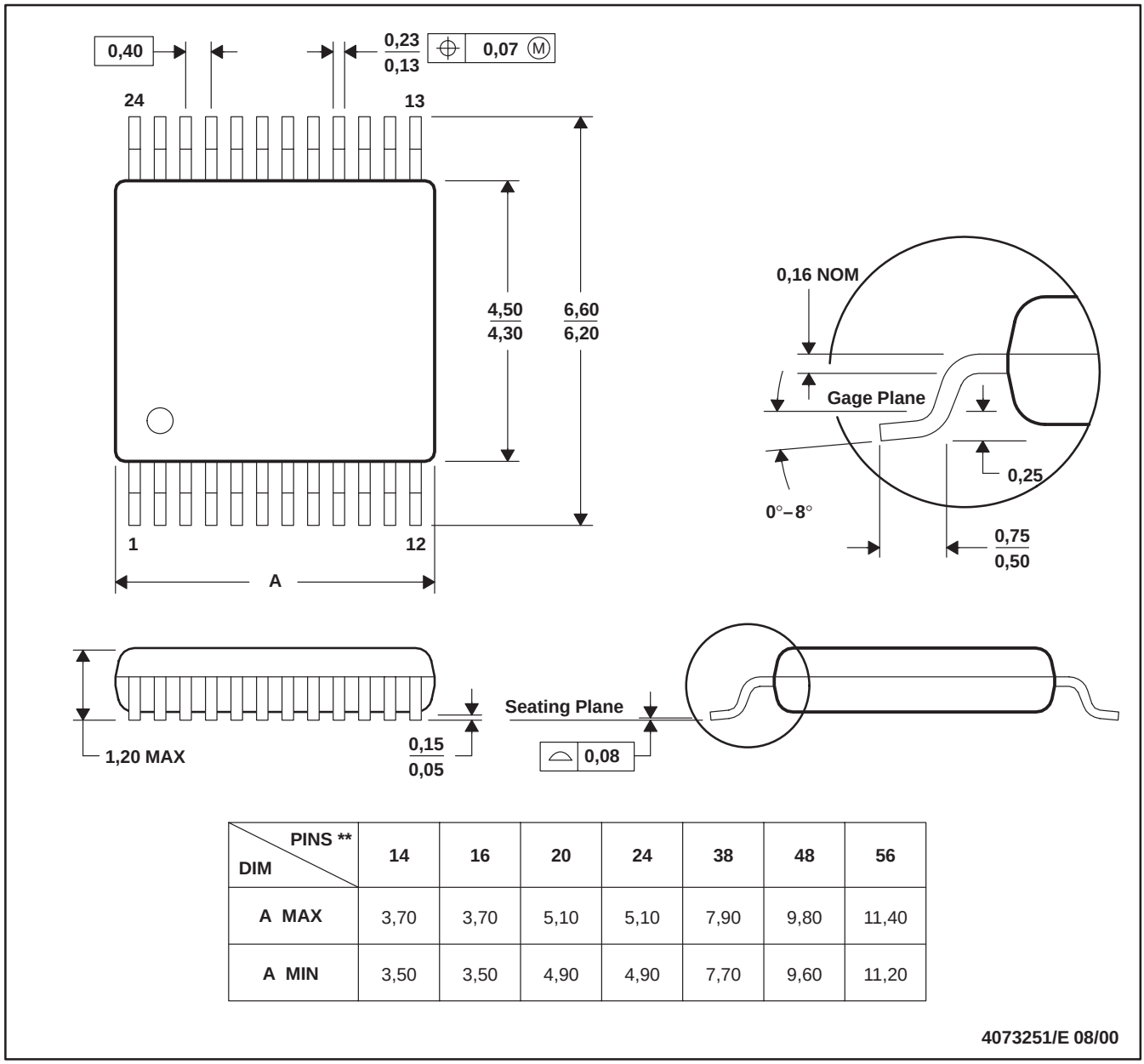

| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

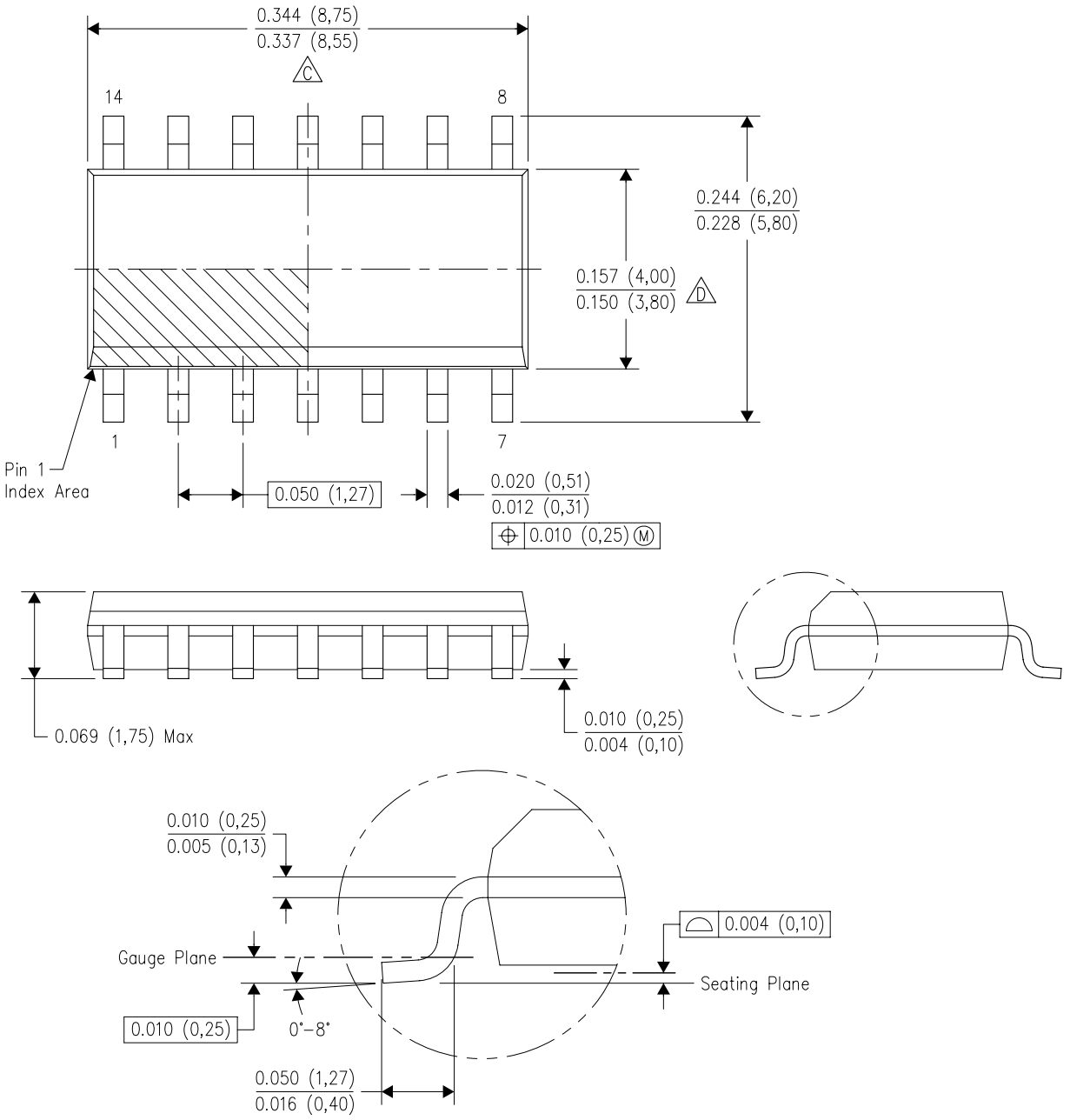



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

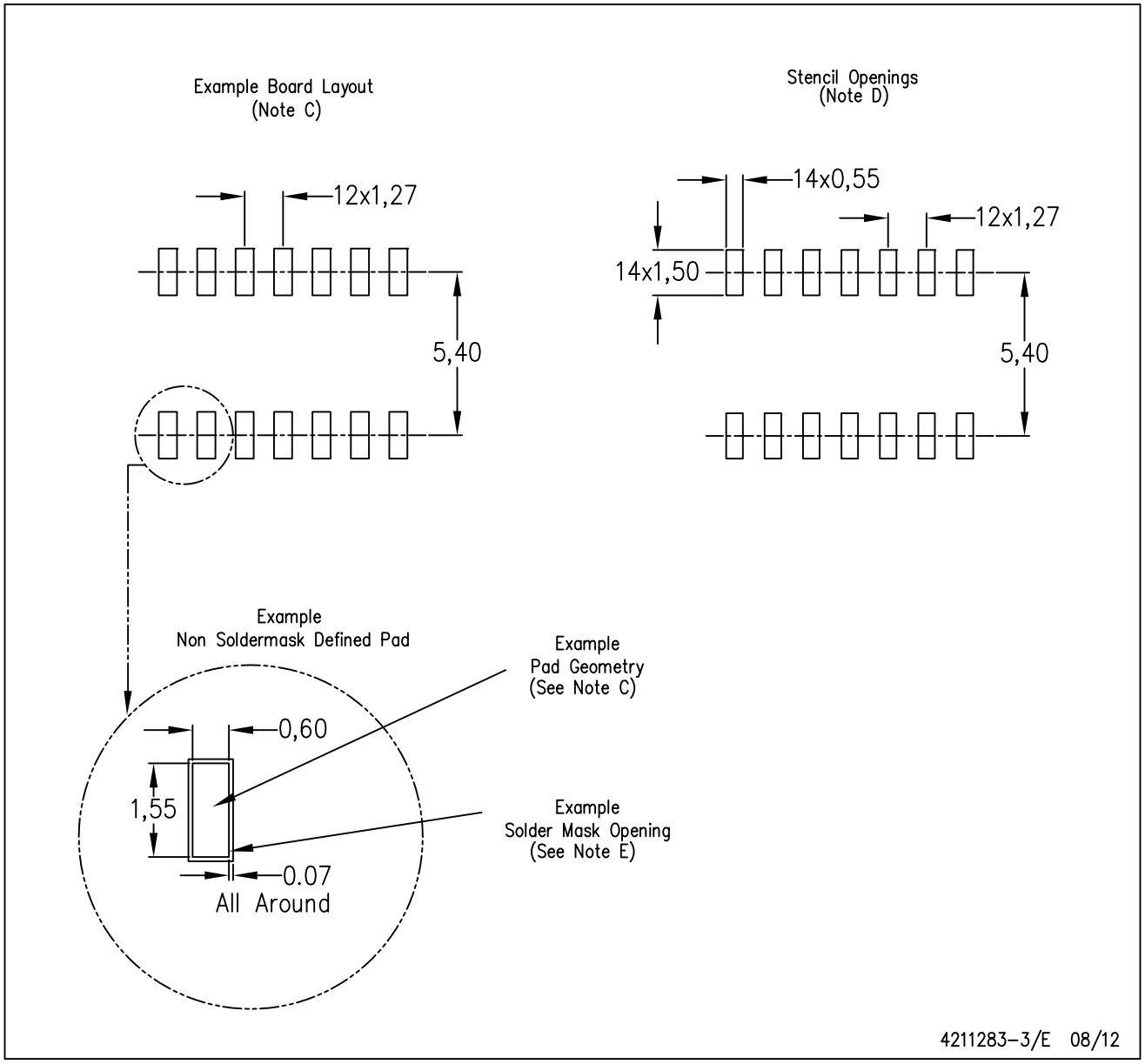
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

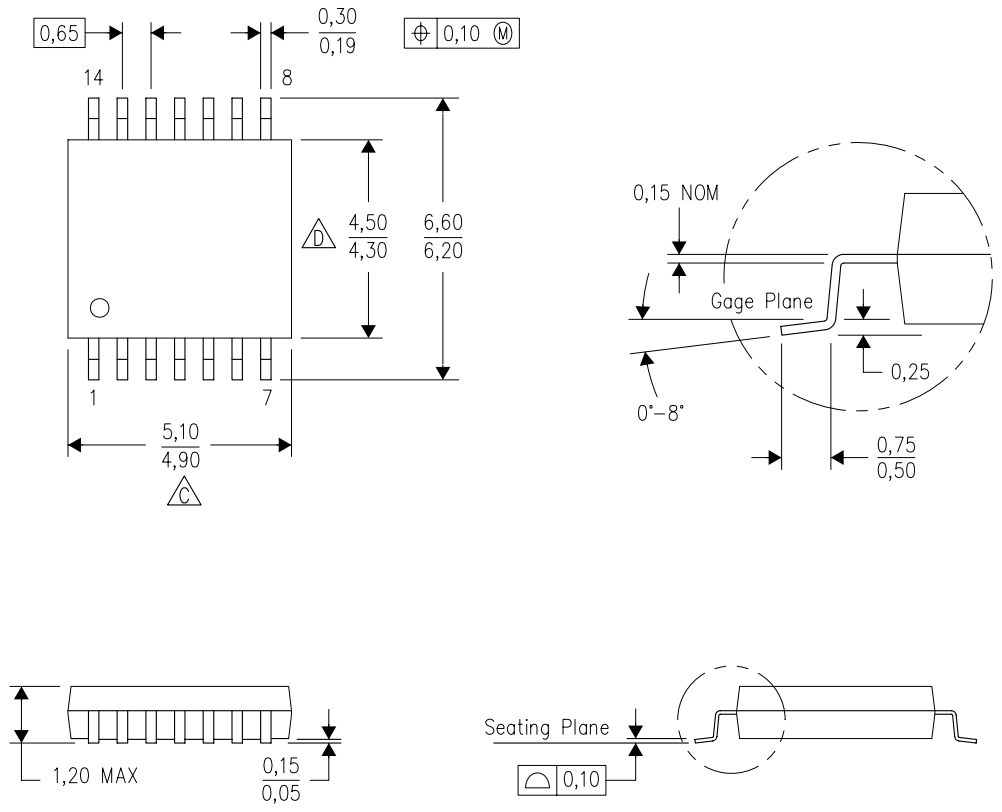
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

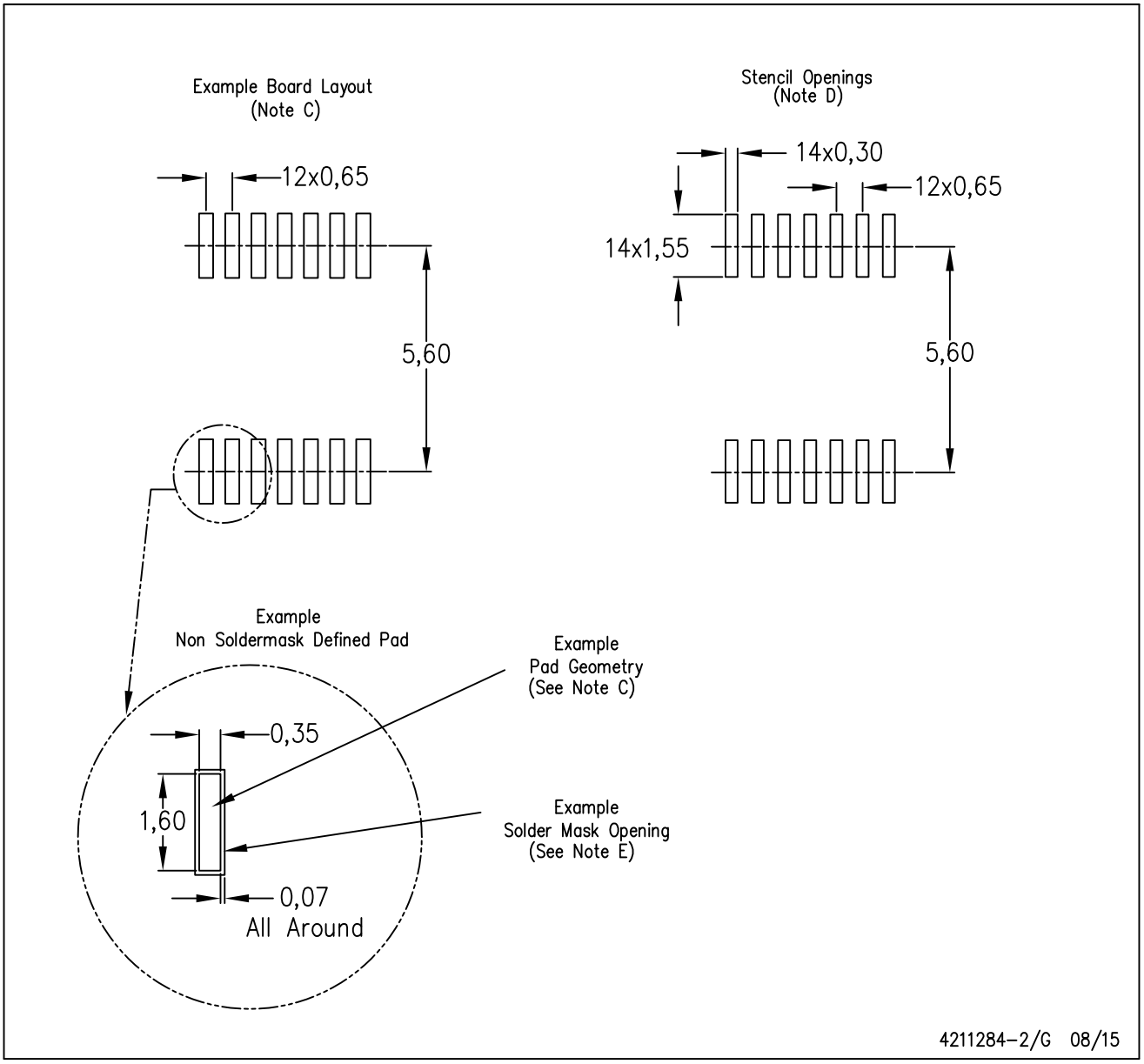
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

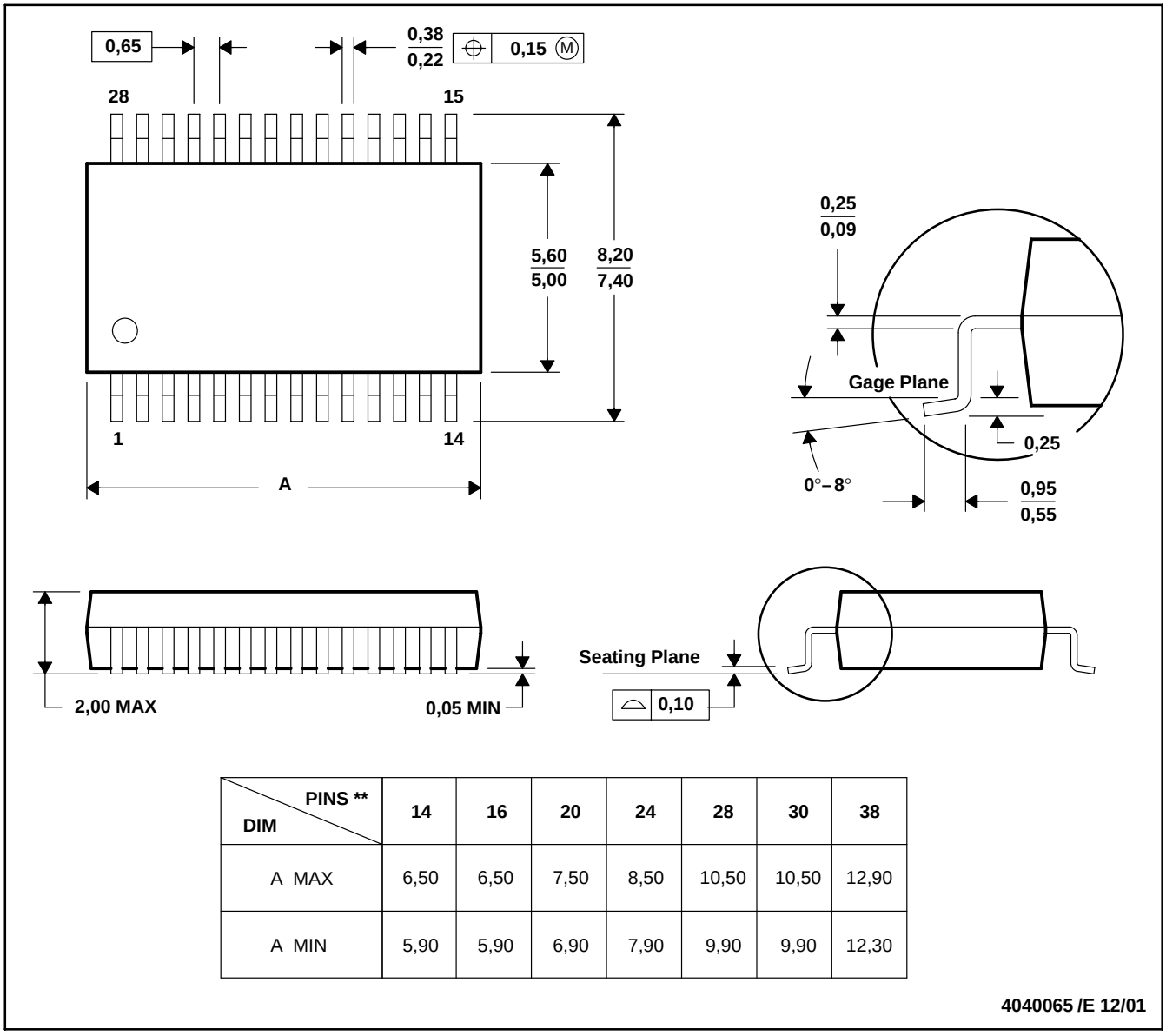



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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