DRV8426E/P Dual H-Bridge Motor Drivers With Integrated Current Sense and Smart Tune Technology

1 Features

- Dual H-bridge motor driver
  - One bipolar stepper motor
  - Dual bidirectional brushed-DC motors
  - Four unidirectional brushed-DC motors
- Integrated current sense functionality
  - No sense resistors required
  - ±5% Full-scale current accuracy
- 4.5-V to 33-V Operating supply voltage range
- Multiple control interface options
  - PHASE/ENABLE (PH/EN)
  - PWM (IN/IN)
- Smart tune, fast and mixed decay options
- Low $R_{DS(ON)}$: 900 mΩ HS + LS at 24 V, 25°C
- High Current Capacity Per Bridge
  - 2.5-A peak (brushed), 1.5-A Full-Scale (stepper)

  Pin to pin compatible with -

  - DRV8424E/P: 33-V, 330 mΩ HS + LS
  - DRV8436E/P: 48-V, 900 mΩ HS + LS
  - DRV8434E/P: 48-V, 330 mΩ HS + LS
- Configurable Off-Time PWM Chopping
  - 7, 16, 24 or 32 µs
- Supports 1.8-V, 3.3-V, 5.0-V logic inputs
- Low-current sleep mode (2 µA)
- Spread spectrum clocking for low EMI
- Inrush current limiting in brushed-DC applications
- Small package and footprint
- Protection features
  - VM undervoltage lockout (UVLO)
  - Charge pump undervoltage (CPUV)
  - Overcurrent protection (OCP)
  - Thermal shutdown (OTSD)
  - Fault condition output (nFAULT)

2 Applications

- Printers and scanners
- ATMs, currency counters, and EPOS
- Office and home automation
- Factory automation and robotics
- Major and small home appliances
- Vacuum, humanoid, and toy robotics

3 Description

The DRV8426E/P devices are dual H-bridge motor drivers for a wide variety of industrial applications. The devices can be used for driving two DC motors, or a bipolar stepper motor.

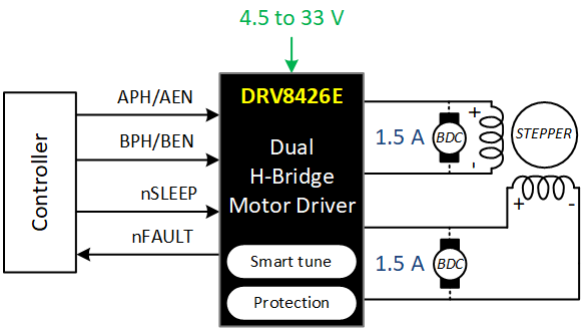
The output stage of the driver consists of N-channel power MOSFETs configured as two full H-bridges, charge pump regulator, current sensing and regulation, and protection circuitry. The integrated current sensing uses an internal current mirror architecture, removing the need for a large power shunt resistor, saving board area and reducing system cost. A low-power sleep mode is provided to achieve ultra- low quiescent current draw by shutting down most of the internal circuitry. Internal protection features are provided for supply undervoltage lockout (UVLO), charge pump undervoltage (CPUV), output overcurrent (OCP), and device overtemperature (OTSD).

The DRV8426E/P is capable of driving a stepper motor with up to 1.5-A full scale or brushed motors with up to 2.5-A peak (dependent on PCB design).

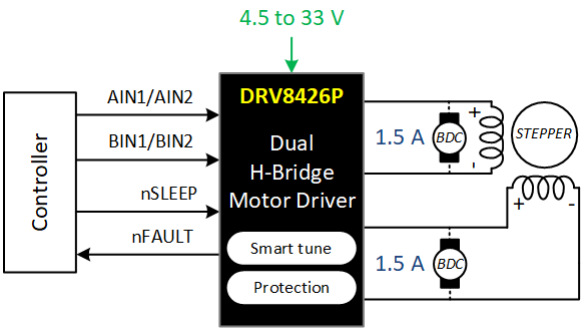
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8426EPWPR	HTSSOP (28)	9.7mm x 4.4mm
DRV8426ERGER	VQFN (24)	4.0mm x 4.0mm
DRV8426PPWPR	HTSSOP (28)	9.7mm x 4.4mm
DRV8426PRGER	VQFN (24)	4.0mm x 4.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



DRV8426E Simplified Schematic



DRV8426P Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2020) to Revision B (May 2022)	Page
• Added Typical Characteristics section	10
• Updated HTSSOP and QFN layout examples.	38

Changes from Revision * (May 2020) to Revision A (November 2020)	Page
• Changed Device Status to "Production Data"	1

5 Pin Configuration and Functions

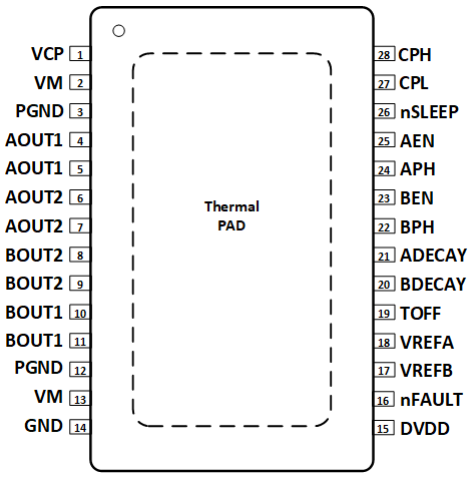


Figure 5-1. PWP PowerPAD™ Package 28-Pin HTSSOP Top View DRV8426E

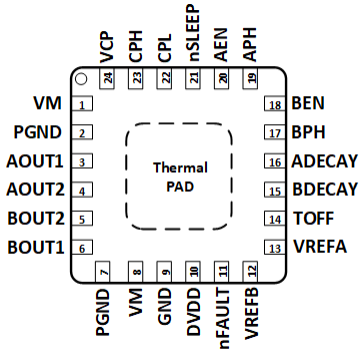


Figure 5-2. RGE Package 24-Pin VQFN with Exposed Thermal PAD Top View DRV8426E

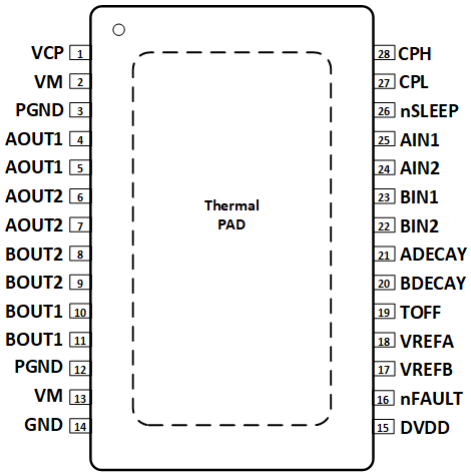


Figure 5-3. PWP PowerPAD™ Package 28-Pin HTSSOP Top View DRV8426P

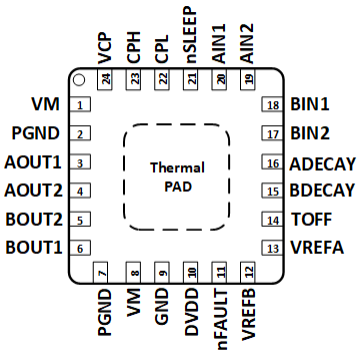


Figure 5-4. RGE Package 24-Pin VQFN with Exposed Thermal PAD Top View DRV8426P

Pin Functions

PIN					TYPE	DESCRIPTION
NAME	PWP		RGE			
	DRV8426E	DRV8426P	DRV8426E	DRV8426P		
ADECAY	21	21	16	16	I	Decay mode setting pin. Set the decay mode for bridge A; quad-level pin.
AEN	25	—	20	—	I	Bridge A enable input. Logic high enables bridge A; logic low disables the bridge Hi-Z.
AIN1	—	25	—	20	I	Bridge A PWM input. Logic controls the state of H-bridge A; internal pulldown.
AIN2	—	24	—	19	I	Bridge B PWM input. Logic controls the state of H-bridge B; internal pulldown.
AOUT1	4, 5	4, 5	3	3	O	Winding A output. Connect to motor winding.
AOUT2	6, 7	6, 7	4	4	O	Winding A output. Connect to motor winding.
APH	24	—	19	—	I	Bridge A phase input. Logic high drives current from AOUT1 to AOUT2.
VREFA	18	18	13	13	I	Reference voltage input. Voltage on this pin sets the full scale chopping current in H-bridge A.
BDECAY	20	20	15	15	I	Decay mode setting pin. Set the decay mode for bridge B; quad-level pin.
BEN	23	—	18	—	I	Bridge B enable input. Logic high enables bridge B; logic low disables the bridge Hi-Z.
BIN1	—	23	—	18	I	Bridge B PWM input. Logic controls the state of H-bridge B; internal pulldown.
BIN2	—	22	—	17	I	Bridge B PWM input. Logic controls the state of H-bridge B; internal pulldown.
BOUT1	10, 11	10, 11	6	6	O	Winding B output. Connect to motor winding.
BOUT2	8, 9	8, 9	5	5	O	Winding B output. Connect to motor winding.
BPH	22	—	17	—	I	Bridge B phase input. Logic high drives current from BOUT1 to BOUT2.
VREFB	17	17	12	12	I	Reference voltage input. Voltage on this pin sets the full scale chopping current in H-bridge B.

PIN					TYPE	DESCRIPTION
NAME	PWP		RGE			
	DRV8426E	DRV8426P	DRV8426E	DRV8426P		
CPH	28	28	23	23	PWR	Charge pump switching node. Connect a X7R, 0.022-µF, VM-rated ceramic capacitor from CPH to CPL.
CPL	27	27	22	22		
GND	14	14	9	9	PWR	Device ground. Connect to system ground.
TOFF	19	19	14	14	I	Sets the decay mode off-time during current chopping; quad-level pin. Also sets the ripple current in smart tune ripple control mode.
DVDD	15	15	10	10	PWR	Logic supply voltage. Connect a X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
VCP	1	1	24	24	O	Charge pump output. Connect a X7R, 0.22-µF, 16-V ceramic capacitor to VM.
VM	2, 13	2, 13	1, 8	1, 8	PWR	Power supply. Connect to motor supply voltage and bypass to PGND with two 0.01-µF ceramic capacitors (one for each pin) plus a bulk capacitor rated for VM.
PGND	3, 12	3, 12	2, 7	2, 7	PWR	Power ground. Connect to system ground.
nFAULT	16	16	11	11	O	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.
nSLEEP	26	26	21	21	I	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor. An nSLEEP low pulse clears faults.
PAD	-	-	-	-	-	Thermal pad. Connect to system ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	35	V
Charge pump voltage (VCP, CPH)	–0.3	V_{VM} + 7	V
Charge pump negative switching pin (CPL)	–0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
Control pin voltage (APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2, nFAULT, ADECAY, BDECAY, TOFF)	–0.3	5.75	V
Open drain output current (nFAULT)	0	10	mA
Reference input pin voltage (VREFA, VREFB)	–0.3	5.75	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–1	V_{VM} + 1	V
Transient 100 ns phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–3	V_{VM} + 3	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	Corner pins	±750	
			Other pins	±500	

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	33	V
V_I	Logic level input voltage	0	5.5	V
V_{REF}	Reference rms voltage range (VREFA, VREFB)	0.05	3.3	V
f_{PWM}	Applied PWM signal (APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2)	0	100	kHz
I_{FS}	Motor full-scale current (xOUTx)	0	1.5	A
I_{rms}	Motor RMS current (xOUTx)	0	1.1	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC		PWP (HTSSOP)	RGE (VQFN)	UNIT
		28 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.0	43.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.0	35.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.9	19.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.8	19.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.9	6.7	°C/W

6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	nSLEEP = 1, No motor load		5	6.5	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		2	4	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.8	1.2	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.8	1.2	ms
V_{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 33 V	4.75	5	5.25	V
		No external load, V_{VM} = 4.5 V	4.2	4.35		V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	6 V < V_{VM} < 33 V		V_{VM} + 5		V
$f_{(VCP)}$	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		360		kHz
LOGIC-LEVEL INPUTS (APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic-high current	V_{IN} = 5 V			100	µA
t_{PD}	Propagation delay	xPH, xEN, xINx input to current change		800		ns
QUAD-LEVEL INPUTS (ADECAY, BDECAY, TOFF)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}		330kΩ ± 5% to GND	1	1.25	1.4	V
V_{I3}	Input Hi-Z voltage	Hi-Z (>500kΩ to GND)	1.8	2	2.2	V
V_{I4}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10		µA
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic-high leakage		–1		1	µA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ONH)}$	High-side FET on resistance	T_J = 25 °C, I_O = -1 A		450	550	mΩ
		T_J = 125 °C, I_O = -1 A		700	850	mΩ
		T_J = 150 °C, I_O = -1 A		780	950	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance	T_J = 25 °C, I_O = 1 A		450	550	mΩ
		T_J = 125 °C, I_O = 1 A		700	850	mΩ
		T_J = 150 °C, I_O = 1 A		780	950	mΩ
t_{SR}	Output slew rate	VM = 24V, I_O = 1 A, Between 10% and 90%		240		V/µs
PWM CURRENT CONTROL (VREFA, VREFB)						
K_V	Transimpedance gain	VREF = 3.3 V	2.09	2.2	2.31	V/A
I_{VREF}	VREF Leakage Current	VREF = 3.3 V			8.25	µA

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OFF}	PWM off-time	TOFF = 0		7		µs
		TOFF = 1		16		
		TOFF = Hi-Z		24		
		TOFF = 330 kΩ to GND		32		
ΔI_{TRIP}	Current trip accuracy	I_O = 1.5 A, 10% to 20% current setting	–15		15	%
		I_O = 1.5 A, 20% to 67% current setting	–10		10	
		I_O = 1.5 A, 68% to 100% current setting	-5		5	
$I_{O,CH}$	AOUT and BOUT current matching	I_O = 1.5 A	–2.5		2.5	%
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling, UVLO falling	4.1	4.25	4.35	V
		VM rising, UVLO rising	4.2	4.35	4.45	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{CPUV}	Charge pump undervoltage	VCP falling		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET	2.5			A
t_{OCP}	Overcurrent deglitch time			1.8		µs
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

6.6 Typical Characteristics

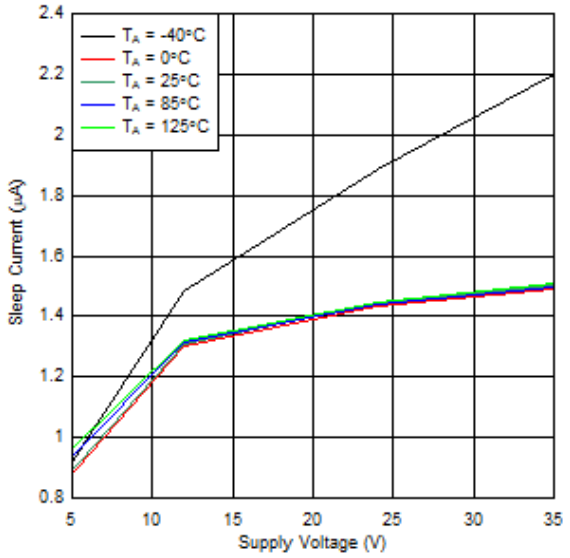


Figure 6-1. Sleep Current over Supply Voltage

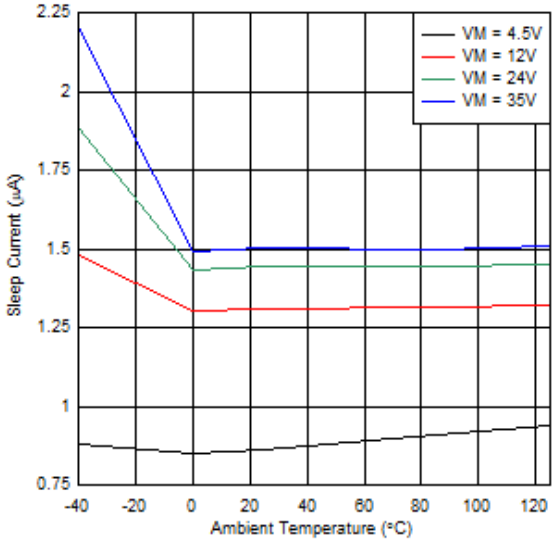


Figure 6-2. Sleep Current over Temperature

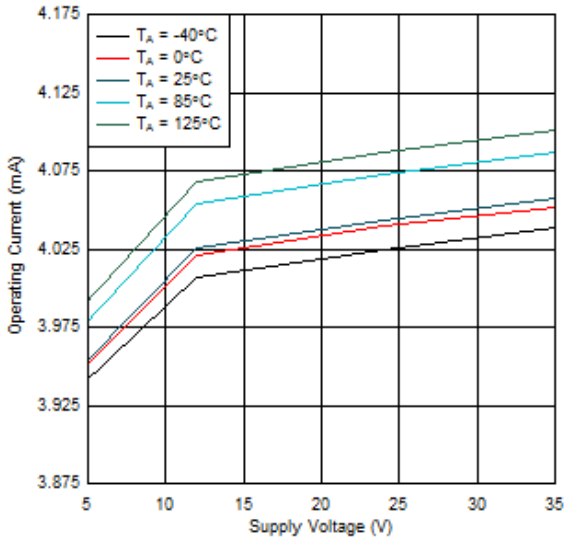


Figure 6-3. Operating Current over Supply Voltage

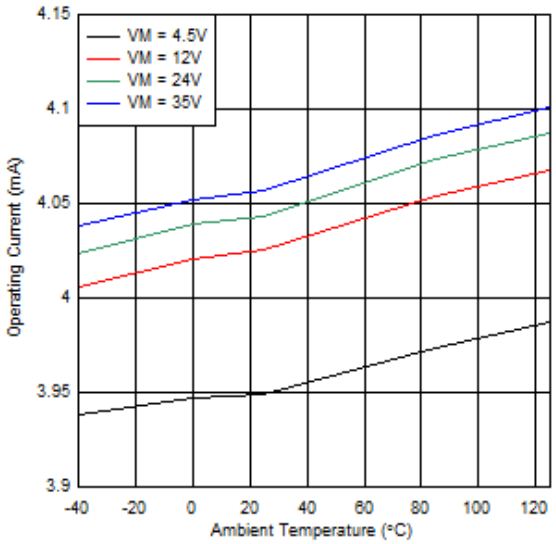


Figure 6-4. Operating Current over Temperature

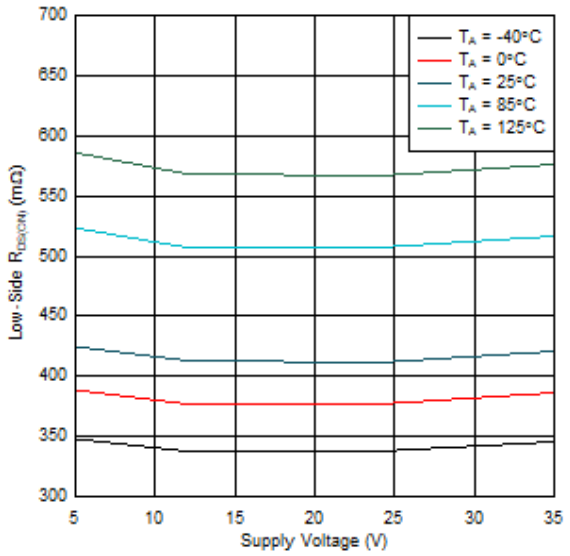


Figure 6-5. Low-Side $R_{DS(ON)}$ over Supply Voltage

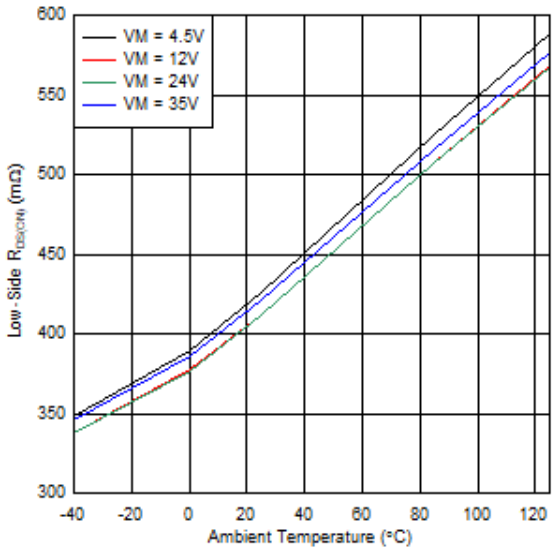


Figure 6-6. Low-Side $R_{DS(ON)}$ over Temperature

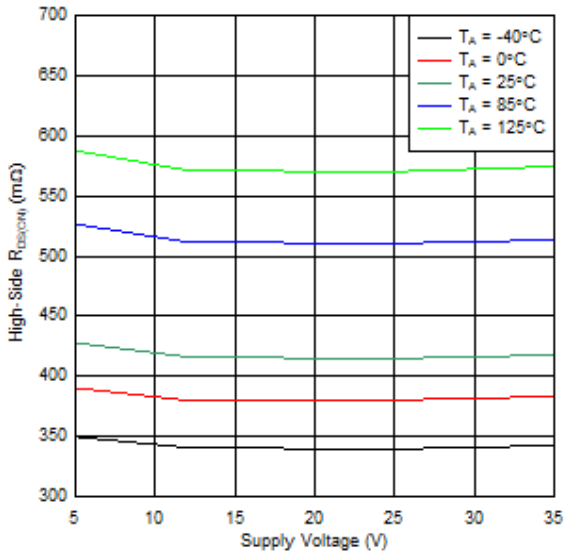


Figure 6-7. High-Side $R_{DS(ON)}$ over Supply Voltage

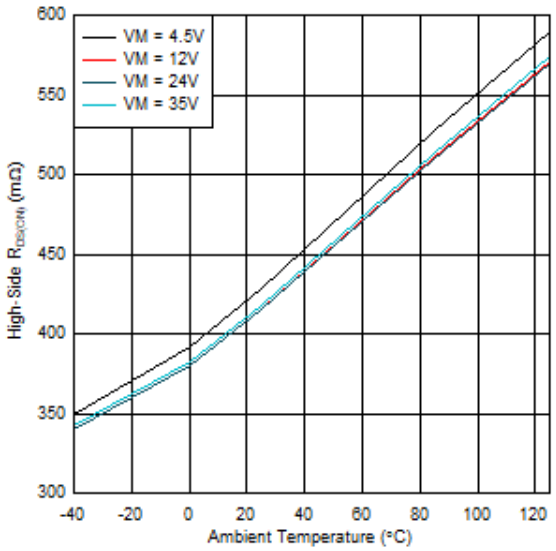


Figure 6-8. High-Side $R_{DS(ON)}$ over Temperature

7 Detailed Description

7.1 Overview

The DRV8426E/P are integrated motor driver solutions for bipolar stepper motors or dual brushed-DC motors. The devices integrate two N-channel power MOSFET H-bridges, integrated current sense and regulation circuitry. The DRV8426E/P are pin-to-pin compatible with the DRV8424E/P, DRV8436E/P, and the DRV8434E/P. The DRV8426E/P can be powered with a supply voltage between 4.5 and 33 V. The DRV8426E/P are capable of providing an output current up to 2.5-A peak or 1.5-A full-scale. The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability.

The DRV8426E/P devices use an integrated current-sense architecture which eliminates the need for two external power sense resistors, hence saving significant board space, BOM cost, design efforts and reduces significant power consumption. This architecture removes the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. The current regulation set point is adjusted by the voltage at the VREFA and VREFB pins.

A simple PH/**E**N (DRV8426**E**) or **P**WM (DRV8426**P**) interface allows easy interfacing to the controller circuit.

The current regulation is highly configurable, with several decay modes of operation. The decay mode can be selected as a smart tune Dynamic Decay, smart tune Ripple Control, mixed, or fast decay. The PWM off-time, t_{OFF}, can be adjusted to 7, 16, 24, or 32 µs.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

7.2 Functional Block Diagrams

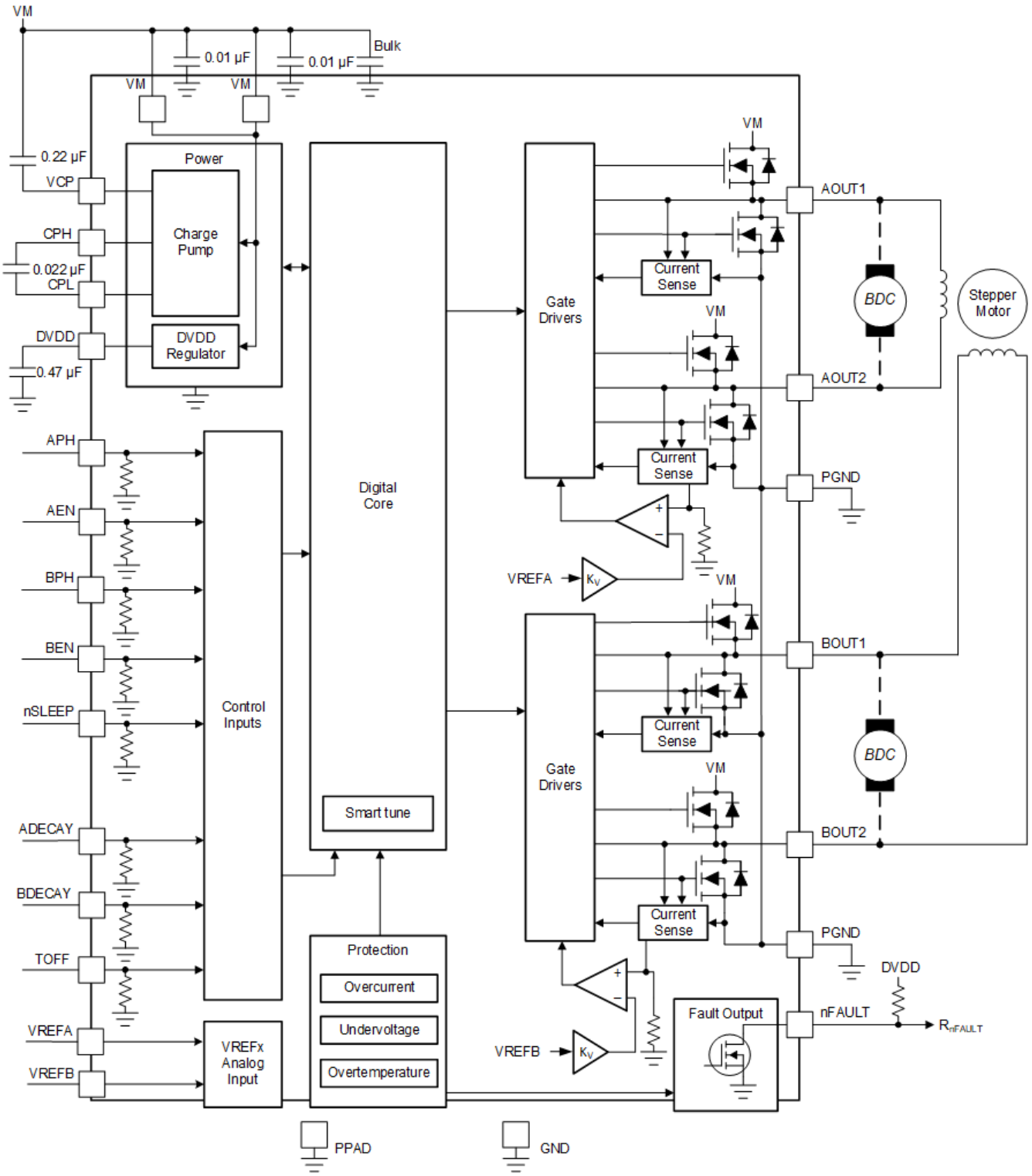


Figure 7-1. DRV8426E Block Diagram

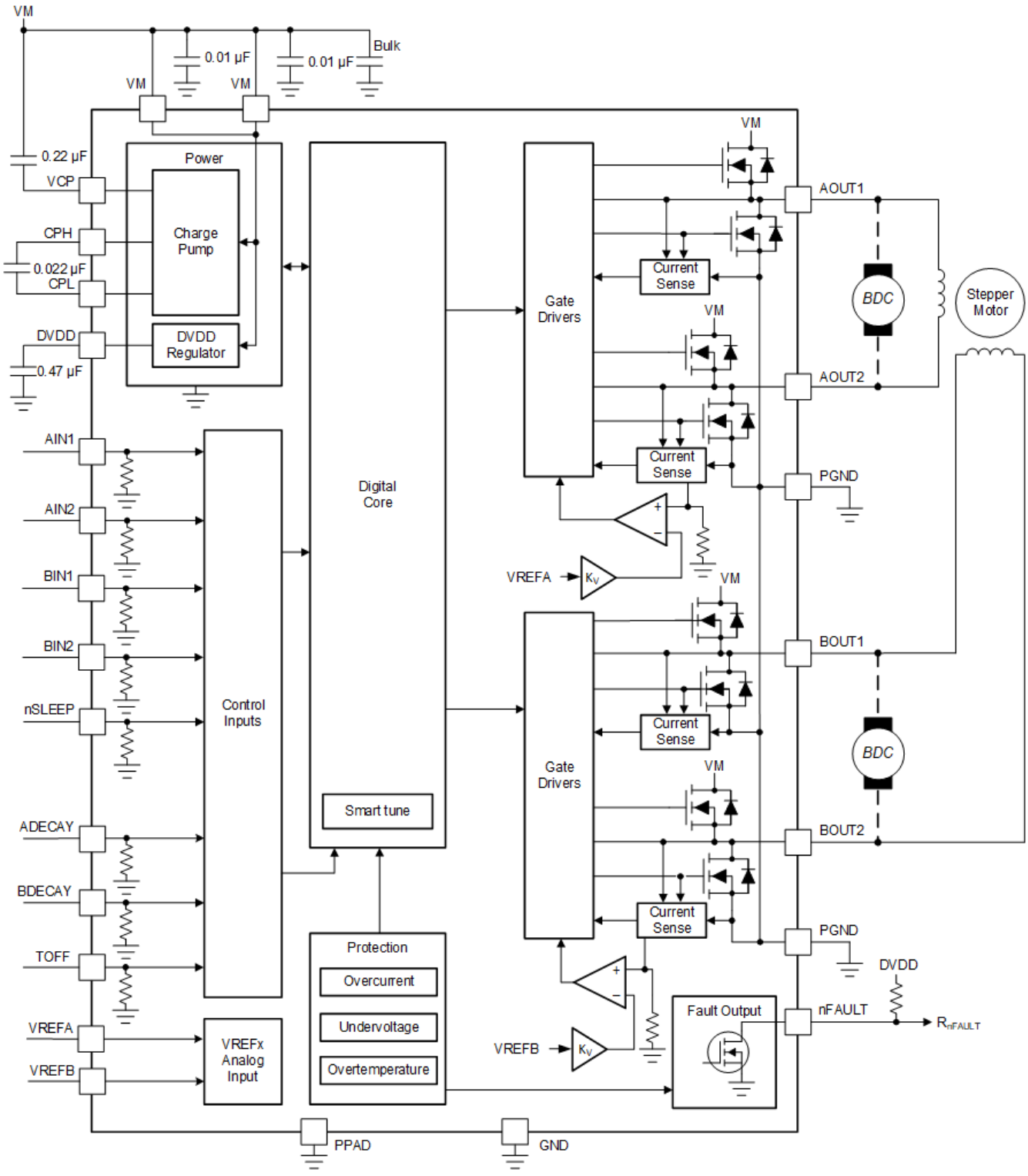


Figure 7-2. DRV8426P Block Diagram

7.3 Feature Description

The following table shows the recommended values of the external components for the driver.

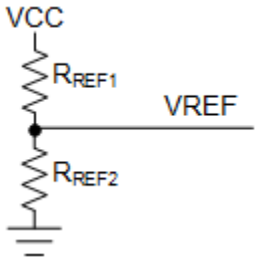


Figure 7-3. Resistor divider connected to the VREF pins

Table 7-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	Two X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM2}	VM	PGND	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X7R, 0.22-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.022-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor
R_{nFAULT}	VCC	nFAULT	>4.7-kΩ resistor
R_{REF1}	VREFx	VCC	Resistor to limit chopping current. It is recommended that the value of parallel combination of R_{REF1} and R_{REF2} should be less than 50-kΩ.
R_{REF2} (Optional)	VREFx	GND	

VCC is not a pin on the device, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to DVDD.VCC is not a pin on the DRV8932, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to DVDD.

7.3.1 PWM Motor Drivers

The DRV8426E and DRV8426P contain drivers for two full H-bridges. Figure 7-4 shows a block diagram of the circuitry.

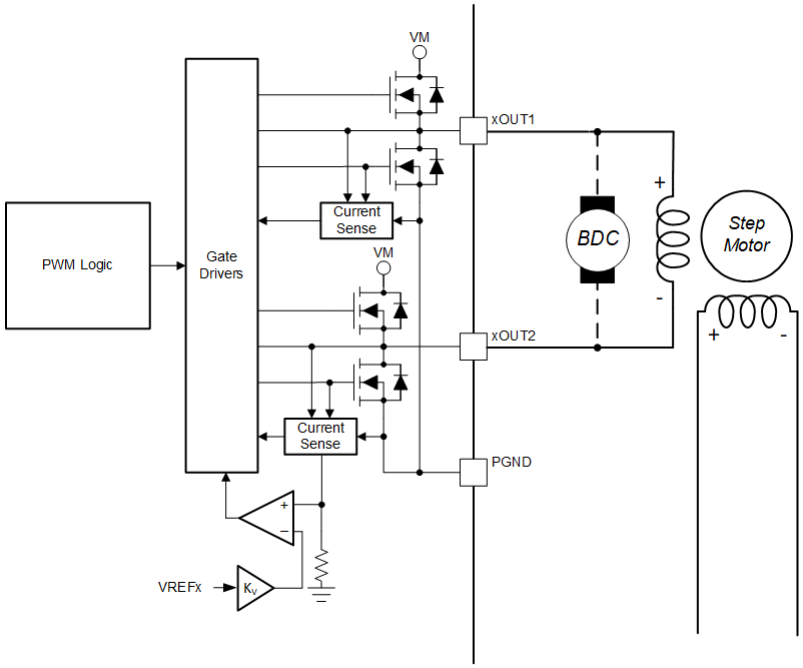


Figure 7-4. PWM Motor Driver Block Diagram

7.3.2 Bridge Control

The DRV8426E is controlled using a PH/EN interface. Table 7-2 gives the full H-bridge state. Note that this table does not take into account the current control built into the DRV8426E. Positive current is defined in the direction of xOUT1 to xOUT2.

Table 7-2. DRV8426E (PH/EN) Control Interface

nSLEEP	xEN	xPH	xOUT1	xOUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep mode; H-bridge disabled Hi-Z
1	0	X	Hi-Z	Hi-Z	H-bridge disabled Hi-Z
1	1	0	L	H	Reverse (current xOUT2 to xOUT1)
1	1	1	H	L	Forward (current xOUT1 to xOUT2)

The DRV8426P is controlled using a PWM interface. Table 7-3 gives the full H-bridge state. Note that this table does not take into account the current control built into the DRV8426P. Positive current is defined in the direction of xOUT1 to xOUT2.

Table 7-3. DRV8426P (PWM) Control Interface

nSLEEP	xIN1	xIN2	xOUT1	xOUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep mode; H-bridge disabled Hi-Z
1	0	0	L	L	Brake; low-side slow decay
1	0	1	L	H	Reverse (current xOUT2 to xOUT1)
1	1	0	H	L	Forward (current xOUT1 to xOUT2)
1	1	1	H	H	Brake; high-side slow decay

7.3.3 Current Regulation

The current through the motor windings is regulated by an adjustable, off-time PWM current-regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold, the bridge enters a decay mode for a period of time determined by the TOFF pin setting to decrease the current. After the off-time expires, the bridge is re-enabled, starting another PWM cycle.

Table 7-4. Off-Time Settings

TOFF	OFF-TIME t_{OFF}
0	7 µs
1	16 µs
Hi-Z	24 µs
330kΩ to GND	32 µs

The TOFF pin configures the PWM OFF time for all decay modes except smart tune ripple control. The OFF time settings can be changed on the fly. After a OFF time setting change, the new OFF time is applied after a 10 µs de-glitch time.

The current regulation threshold is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. To generate the reference voltage for the comparator, the VREFx input is attenuated by a factor of Kv.

The current regulation threshold (I_{REG}) can be calculated as I_{REG} (A) = V_{REFx} (V) / K_V (V/A) = V_{REFx} (V) / 2.2 (V/A).

7.3.4 Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 7-5, Item 1.

Once the current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, once the current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. Fast decay mode is shown in Figure 7-5, item 2. In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 7-5, Item 3.

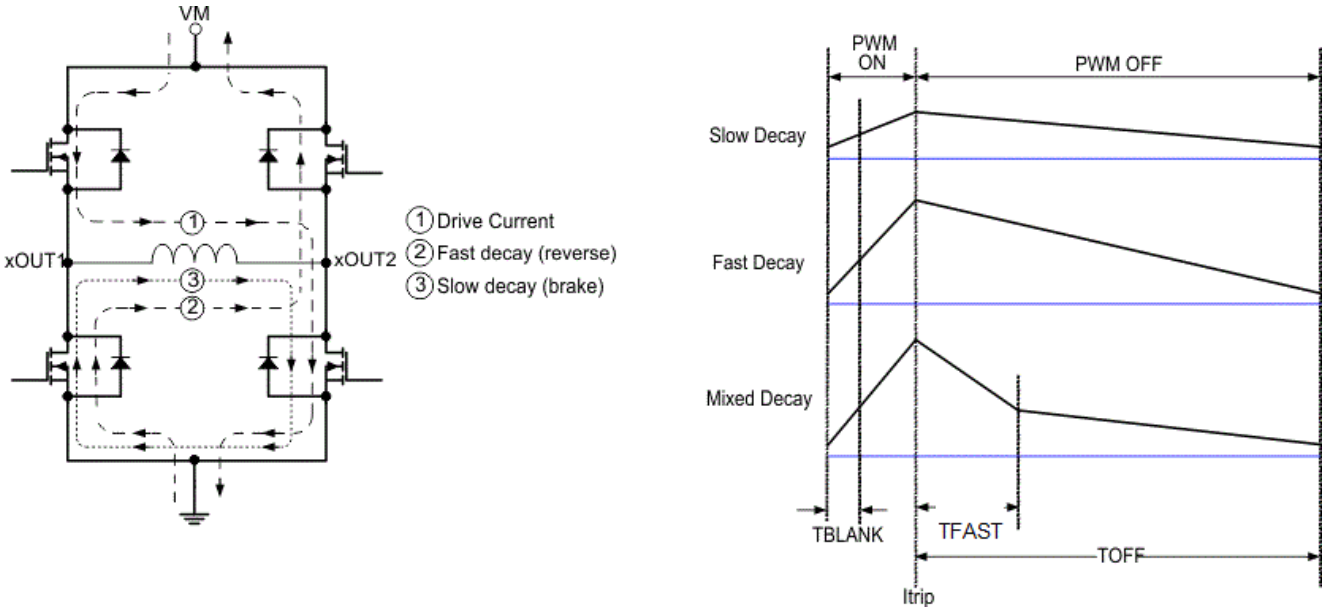


Figure 7-5. Decay Modes

The decay mode is selected by setting the quad-level ADECAY and BDECAY pins as shown in Table 7-5.

Table 7-5. Decay Mode Settings

xDECAY	DECAY MODE
0	Smart tune Dynamic Decay
1	Smart tune Ripple Control
Hi-Z	Mixed decay: 30% fast
330k to GND	Fast decay

The ADECAY pin sets the decay mode for H-bridge A (AOUT1, AOUT2), and the BDECAY pin sets the decay mode for H-bridge B (BOUT1, BOUT2).

7.3.4.1 Mixed Decay

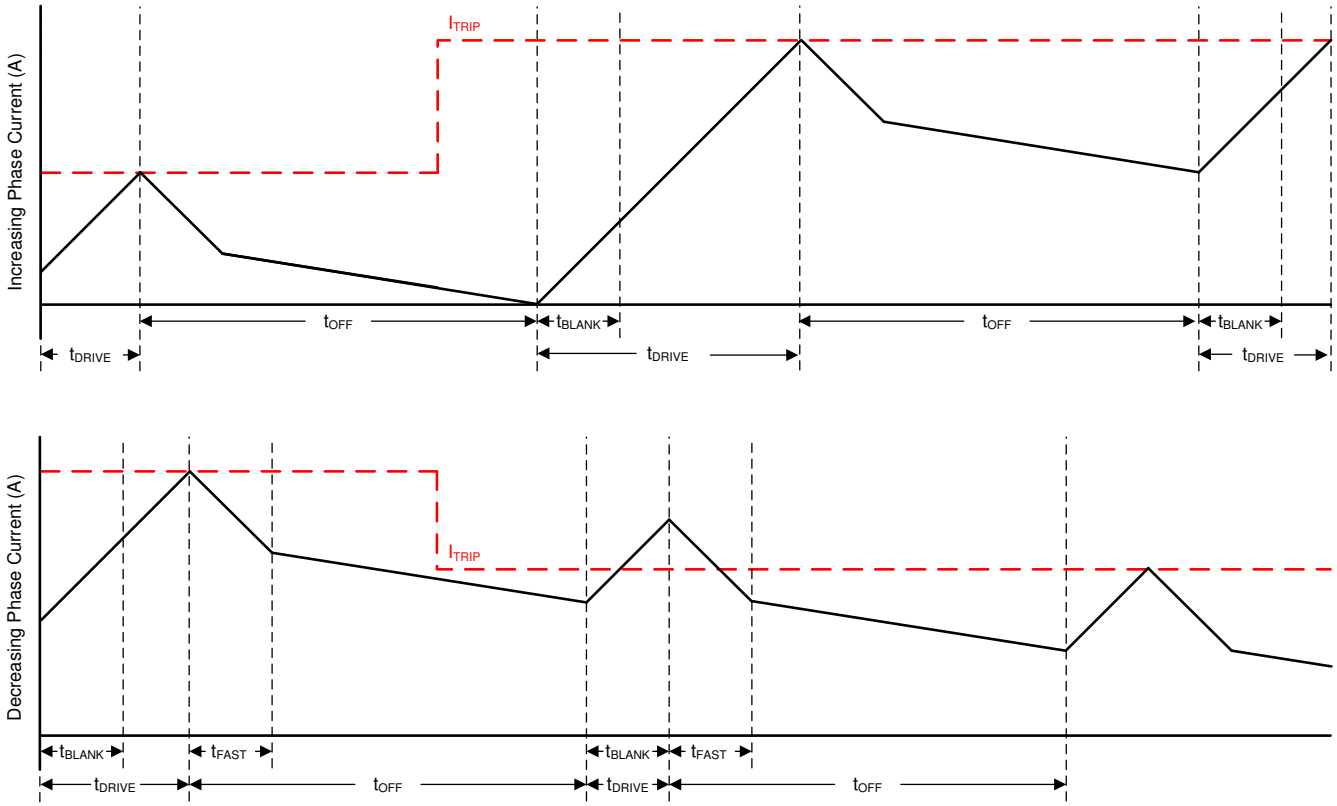


Figure 7-6. Mixed Decay Mode

Mixed decay begins as fast decay for 30% of t_{OFF}, followed by slow decay for the remainder of t_{OFF}.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

7.3.4.2 Fast Decay

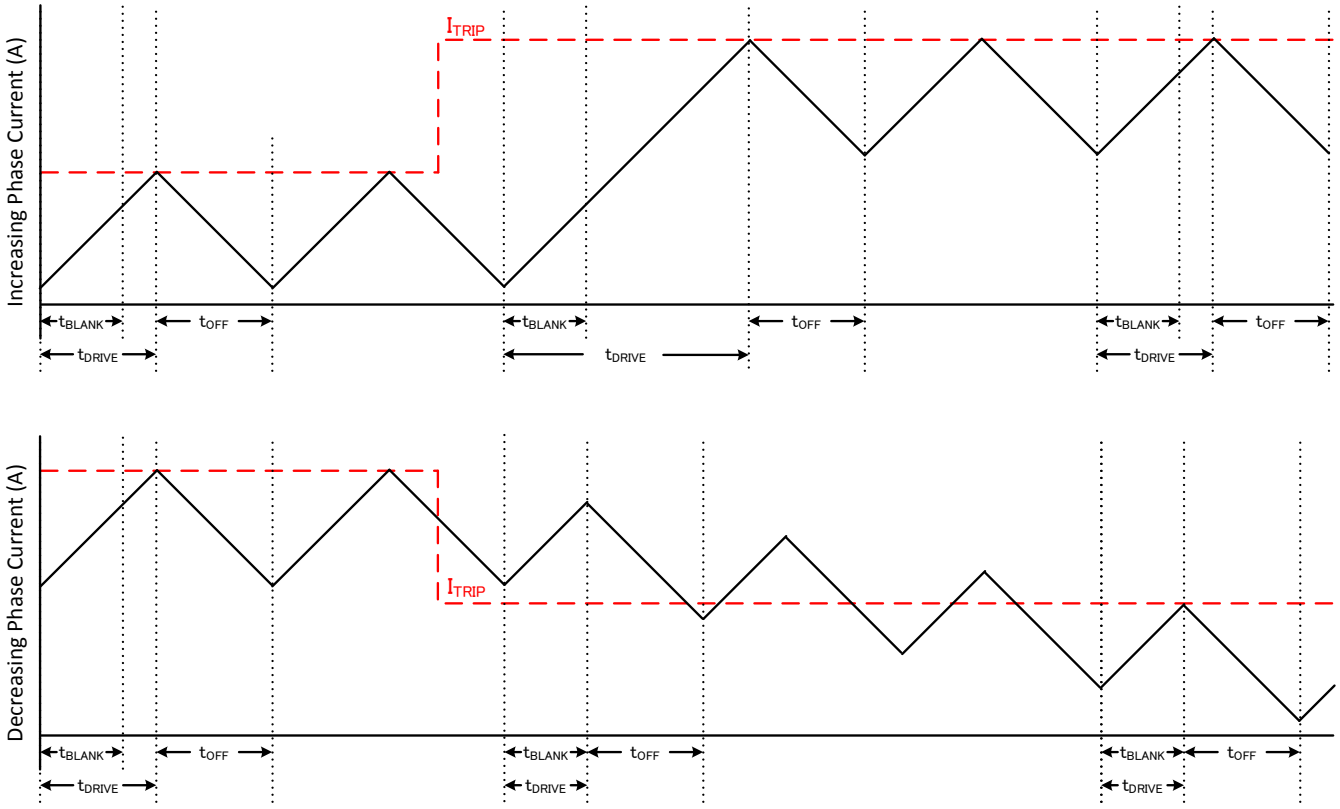


Figure 7-7. Fast/Fast Decay Mode

During fast decay, the polarity of the H-bridge is reversed. The H-bridge will be turned off as current approaches zero in order to prevent current flow in the reverse direction.

Fast decay exhibits the highest current ripple of the decay modes for a given t_{OFF}. Transition time on decreasing current steps is much faster than slow decay since the current is allowed to decrease much faster.

7.3.4.3 Smart tune Dynamic Decay

The smart tune current regulation scheme is an advanced current-regulation control method compared to traditional fixed off-time current regulation schemes. Smart tune current regulation scheme helps the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Low-current versus high-current dI/dt

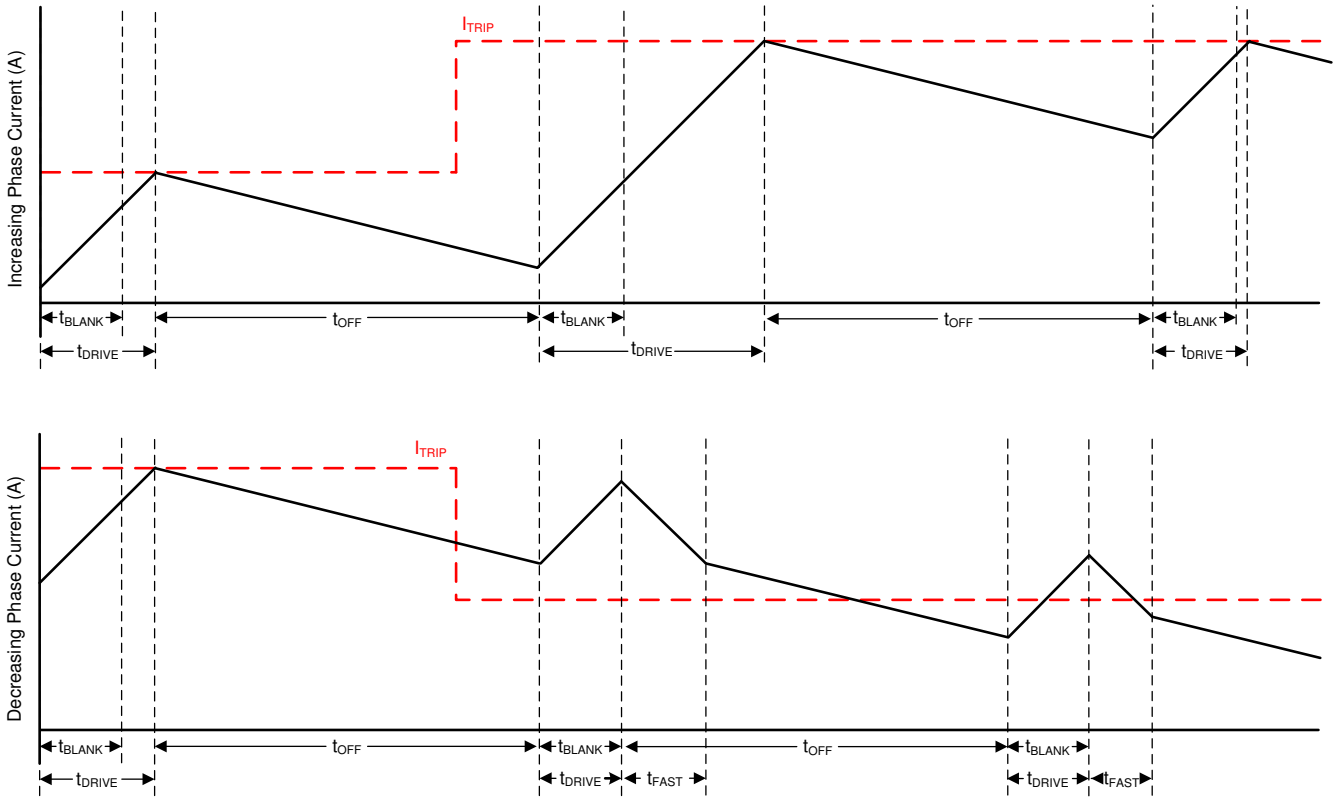


Figure 7-8. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

7.3.4.4 Smart tune Ripple Control

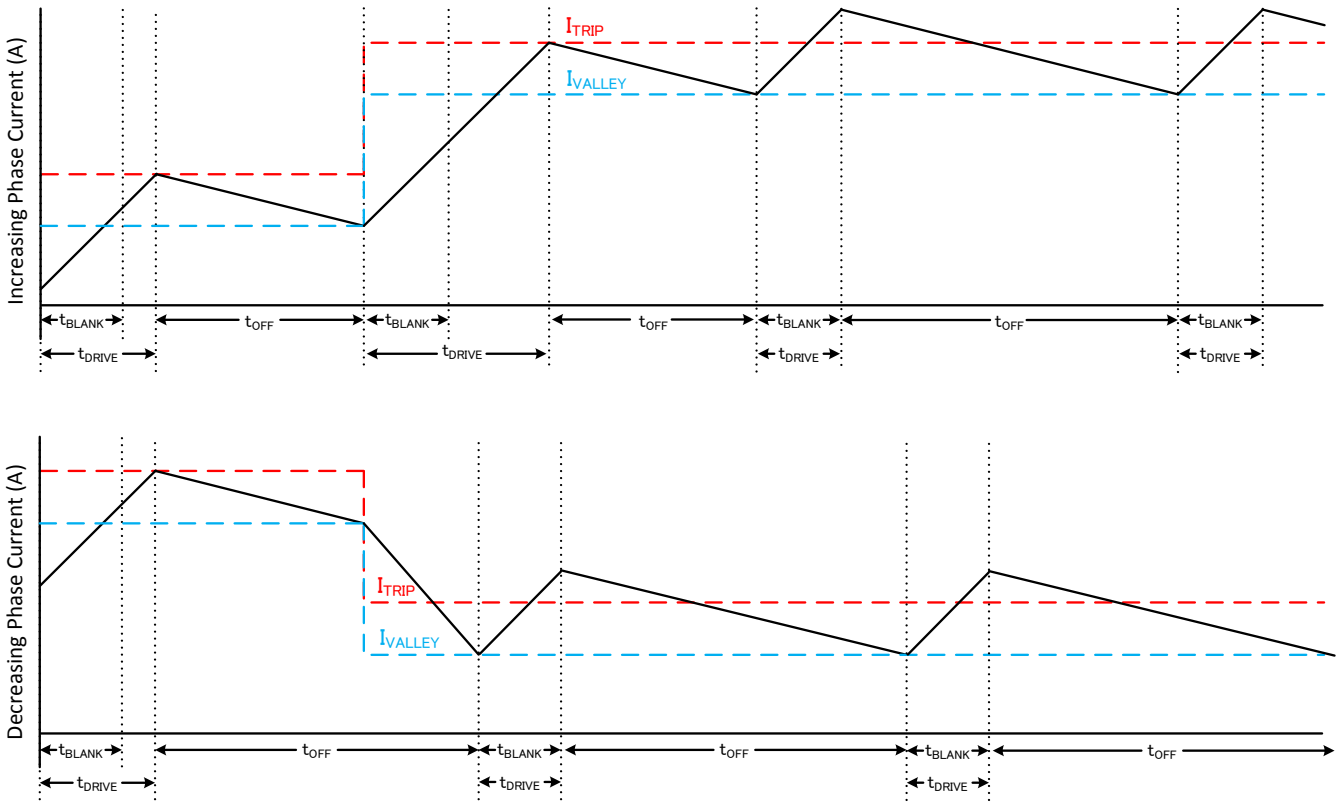


Figure 7-9. Smart tune Ripple Control Decay Mode

Smart tune Ripple Control operates by setting an I_{VALLEY} level alongside the I_{TRIP} level. When the current level reaches I_{TRIP}, instead of entering slow decay until the t_{OFF} time expires, the driver enters slow decay until I_{VALLEY} is reached. Slow decay operates similar to mode 1 in which both low-side MOSFETs are turned on allowing the current to recirculate. In this mode, t_{OFF} varies depending on the current level and operating conditions.

This method allows much tighter regulation of the current level increasing motor efficiency and system performance. Smart tune Ripple Control can be used in systems that can tolerate a variable off-time regulation scheme to achieve small current ripple in the current regulation.

The ripple current in this decay mode is 11mA + 1% of the ITRIP at a specific microstep level.

7.3.4.5 Blanking time

After the current is enabled (start of drive phase) in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM. The blanking time is approximately 1 µs.

7.3.5 Charge Pump

A charge pump is integrated to supply a high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

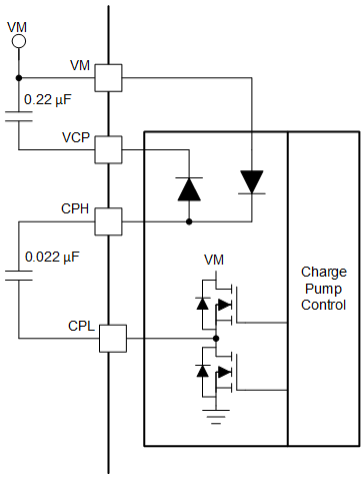


Figure 7-10. Charge Pump Block Diagram

7.3.6 Linear Voltage Regulators

A linear voltage regulator is integrated in the device. The DVDD regulator can be used to provide a reference voltage. DVDD can supply a maximum of 2 mA load. For proper operation, bypass the DVDD pin to GND using a ceramic capacitor.

The DVDD output is nominally 5-V. When the DVDD LDO current load exceeds 2 mA, the output voltage drops significantly.

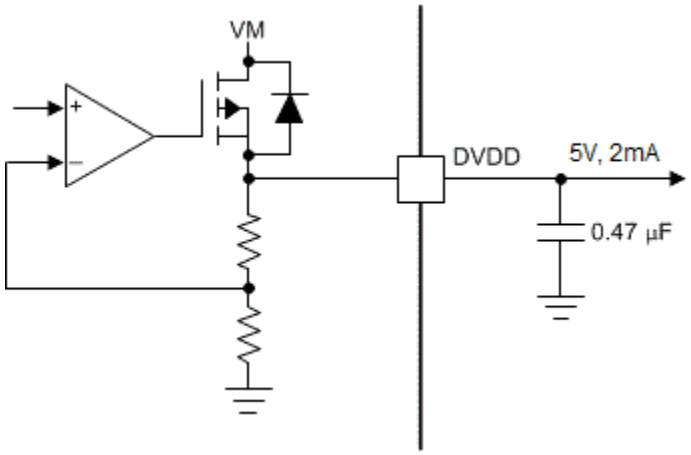


Figure 7-11. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high (that is, ADECAY, BDECAY or TOFF), tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

7.3.7 Logic and Quad-Level Pin Diagrams

Figure 7-12 gives the input structure for logic-level pins APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2 and nSLEEP:

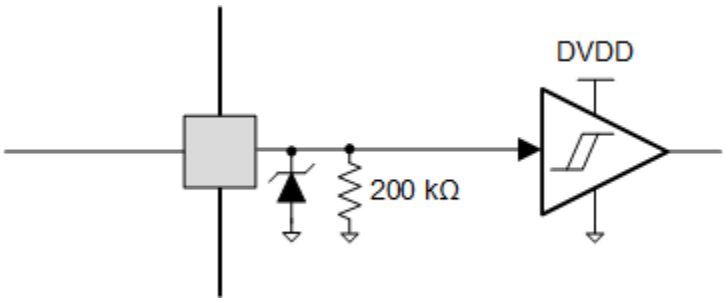


Figure 7-12. Logic-level Input Pin Diagram

Quad-level logic pins TOFF, ADECAY, and BDECAY have the following structure as shown in Figure 7-13.

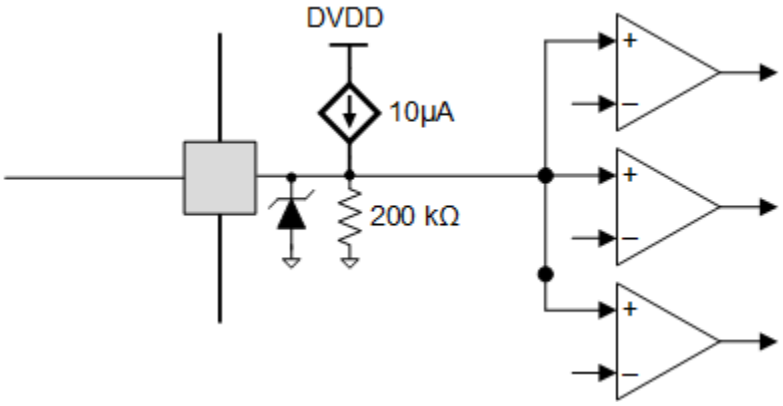


Figure 7-13. Quad-Level Input Pin Diagram

7.3.7.1 nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5-V, 3.3-V or 1.8-V supply. When a fault is detected, the nFAULT pin will be logic low. nFAULT pin will be high after power-up. For a 5-V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3-V or 1.8-V pullup, an external supply must be used.

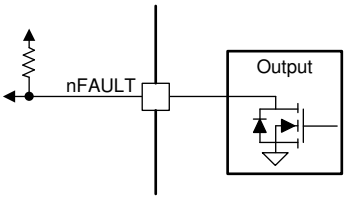


Figure 7-14. nFAULT Pin

7.3.8 Protection Circuits

The devices are fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events.

7.3.8.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO-threshold voltage for the voltage supply, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump is disabled in this condition.

Normal operation resumes (motor-driver operation and nFAULT released) when the VM undervoltage condition is removed.

7.3.8.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed.

7.3.8.3 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, the FETs in that particular H-bridge are disabled and the nFAULT pin is driven low. The charge pump remains active during this condition. Once the OCP condition is removed, normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

7.3.8.4 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit (T_{OTSD}) all MOSFETs in the H-bridge are disabled, and the nFAULT pin is driven low. After the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$), normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

7.3.8.5 Fault Condition Summary

Table 7-6. Fault Condition Summary

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	nFAULT	Disabled	Disabled	Reset (V_{DVDD} < 3.9 V)	Automatic: VM > V_{UVLO}
VCP undervoltage (CPUV)	VCP < V_{CPUV}	nFAULT	Disabled	Operating	Operating	VCP > V_{CPUV}
Overcurrent (OCP)	I_{OUT} > I_{OCP}	nFAULT	Disabled	Operating	Operating	Latched
Thermal Shutdown (OTSD)	T_J > T_{TSD}	nFAULT	Disabled	Disabled	Operating	Latched

7.4 Device Functional Modes

7.4.1 Sleep Mode (nSLEEP = 0)

The state of the device is managed by the nSLEEP pin. When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.2 Operating Mode (nSLEEP = 1)

When the nSLEEP pin is high, and VM > UVLO, the device enters the active mode. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.3 nSLEEP Reset Pulse

A fault can be cleared through a quick nSLEEP pulse. This pulse width must be greater than 20 µs and shorter than 40 µs. If nSLEEP is low for longer than 40 µs but less than 120 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram. This reset pulse does not affect the status of the charge pump or other functional blocks.

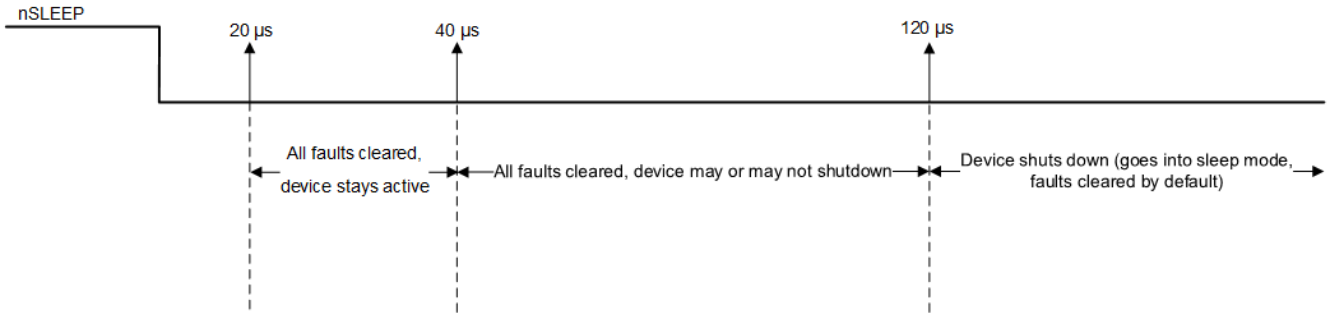


Figure 7-15. nSLEEP Reset Pulse

7.4.4 Functional Modes Summary

Table 7-7 lists a summary of the functional modes.

Table 7-7. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	Logic
Sleep mode	4.5 V < VM < 33 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled
Operating	4.5 V < VM < 33 V	nSLEEP pin = 1	Operating	Operating	Operating	Operating

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8426E/P are used in brushed or stepper motor control.

8.2 Typical Application

In this application, the device is configured to drive bidirectional currents through two external loads (such as two brushed DC motors) using H-bridge configuration. The H-bridge polarity and duty cycle are controlled from the external controller to the xEN/xIN1 and xPH/xIN2 pins.

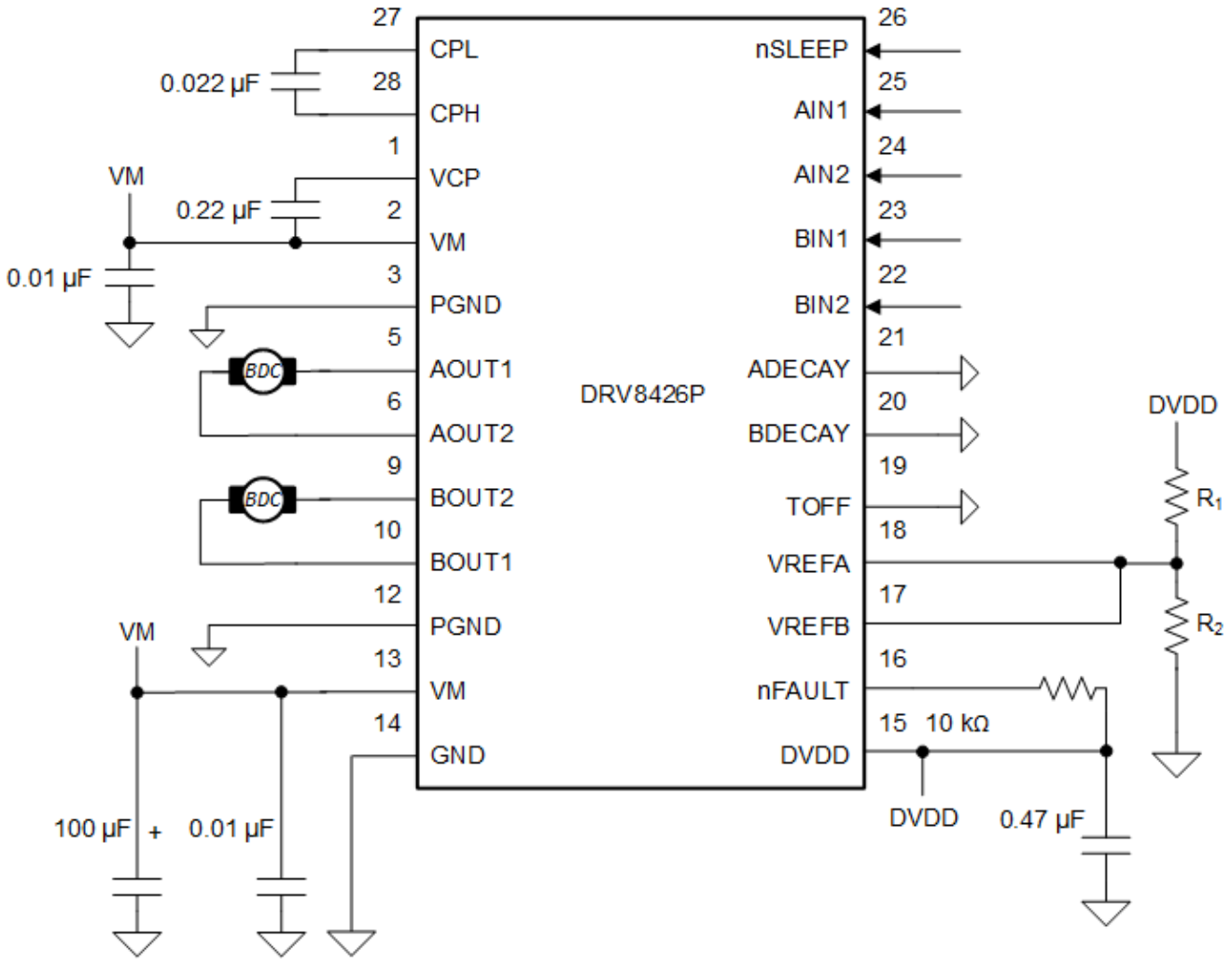


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

Table 8-1 lists the design input parameters for system design.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	3.7 Ω
Motor winding inductance	L_L	6.5 mH
Switching Frequency	f_{PWM}	40 kHz
Regulated Current for Each Motor	I_{REG}	1 A

8.2.2 Detailed Design Procedure

8.2.2.1 Current Regulation

When an output load is connected to the VM supply, the load current can be regulated to the ITRIP level. The ITRIP current level for OUT1 and OUT2 outputs is controlled by the VREF12 pin, and the ITRIP level for OUT3 and OUT4 outputs is controlled by the VREF34 pin. The ITRIP current (ITRIP) can be calculated as ITRIP (A) = VREF (V) / 2.2 (V/A). The VREF voltage can be programmed by connecting resistor dividers from DVDD pin to ground. Both VREF pins can be tied together to program the same ITRIP current for all four output channels.

8.2.2.2 Power Dissipation and Thermal Calculation

The output current and power dissipation capabilities of the device are heavily dependent on the PCB design and external system conditions. This section provides some guidelines for calculating these values.

Total power dissipation (P_{TOT}) for the device is composed of three main components. These are the power MOSFET $R_{DS(ON)}$ (conduction) losses, the power MOSFET switching losses and the quiescent supply current dissipation. While other factors may contribute additional power losses, these other items are typically insignificant compared to the three main items.

$P_{TOT} = P_{COND} + P_{SW} + P_Q$

For loads connected to VM, assuming that all the outputs are loaded with same current, total conduction loss can be expressed as -

$P_{COND} = 4 \times (I_{OUT})^2 \times R_{DS(ONL)}$

As the high-side and low-side MOSFETs of the DRV8935 have the same on-resistance, the conduction loss will be independent of the duty cycle of the input PWM or the amount of PWM off-time. It should be noted that $R_{DS(ON)}$ has a strong correlation with the device temperature. A curve showing the normalized $R_{DS(ON)}$ with temperature can be found in the Typical Characteristics curves.

$P_{COND} = 4 \times (1.5\text{-A})^2 \times 0.165\text{-}\Omega = 1.485\text{-W}$

P_{SW} can be calculated from the nominal supply voltage (VM), regulated output current (I_{OUT}), switching frequency (f_{PWM}) and the device output rise (t_{RISE}) and fall (t_{FALL}) time specifications.

Assuming that all the four outputs are switching simultaneously -

$P_{SW} = 4 \times (P_{SW\_RISE} + P_{SW\_FALL})$

$P_{SW\_RISE} = 0.5 \times VM \times I_{OUT} \times t_{RISE} \times f_{PWM}$

$P_{SW\_FALL} = 0.5 \times VM \times I_{OUT} \times t_{FALL} \times f_{PWM}$

$P_{SW\_RISE} = 0.5 \times 24\ V \times 1.5\ A \times 100\ ns \times 40\ kHz = 0.072\ W$

$P_{SW\_FALL} = 0.5 \times 24\ V \times 1.5\ A \times 100\ ns \times 40\ kHz = 0.072\ W$

$P_{SW} = 4 \times (0.072W + 0.072W) = 0.576\ W$

P_Q can be calculated from the nominal supply voltage (VM) and the I_{VM} current specification.

$P_Q = VM \times I_{VM} = 24\ V \times 5\ mA = 0.12\ W$

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss.

$P_{TOT} = P_{COND} + P_{SW} + P_Q = 1.485\text{-W} + 0.576\text{-W} + 0.12\text{-W} = 2.181\text{-W}$

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as

$T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 31 °C/W for the HTSSOP package and 40.7 °C/W for the VQFN package.

Assuming 25°C ambient temperature, the junction temperature for the HTSSOP package is calculated as -

$T_J = 25°C + (2.181\text{-W} \times 31°C/W) = 92.6\ °C$

The junction temperature for the VQFN package is calculated as -

$T_J = 25°C + (2.181\text{-W} \times 40.7°C/W) = 113.8\ °C$

It should be ensured that the device junction temperature is within the specified operating region.

8.2.2.2.1 Application Curves

CH3 = VM (10V/div), CH1 = nFAULT (3V/div), CH5 = nSLEEP (3V/div), CH7 = I_{REG} (1A/div)

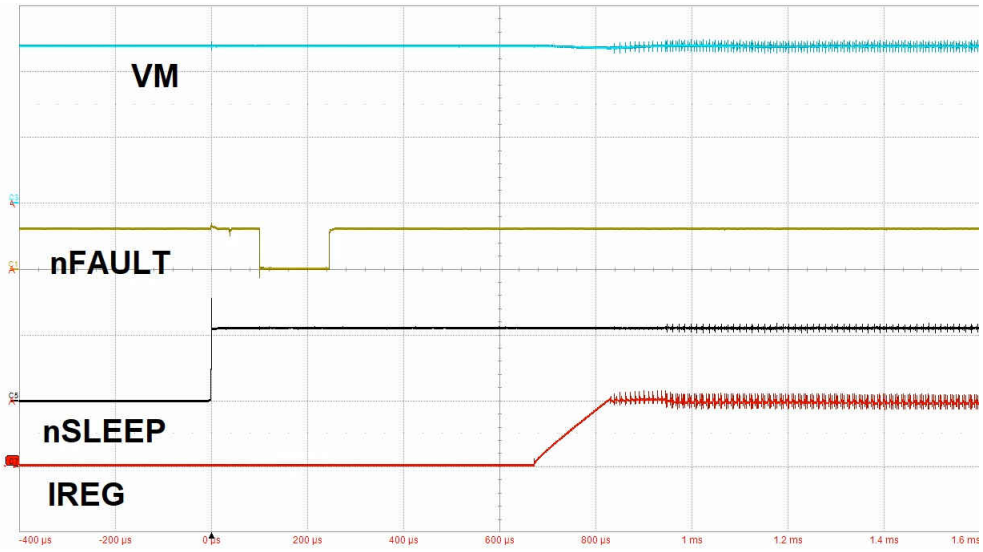


Figure 8-2. Device Power-up with nSLEEP

CH3 = VM (10V/div), CH1 = nFAULT (3V/div), CH5 = nSLEEP (3V/div), CH7 = I_{REG} (1A/div)

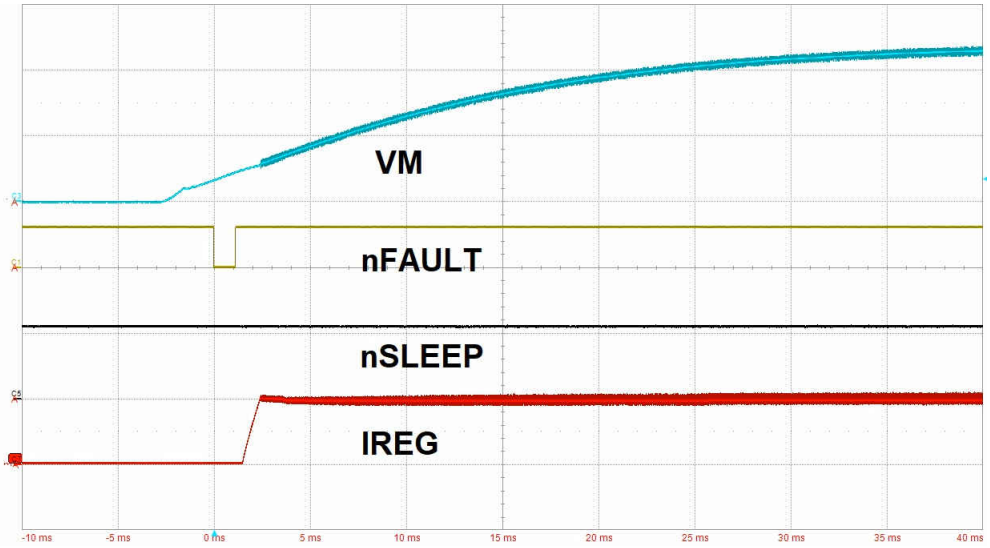


Figure 8-3. Device Power-up with Supply Voltage (VM) Ramp

CH1 = IN1 (3V/div), CH7 = I_{REG} (1A/div), CH3 = AOUT1 (24V/div), CH2 = AOUT2 (24V/div)

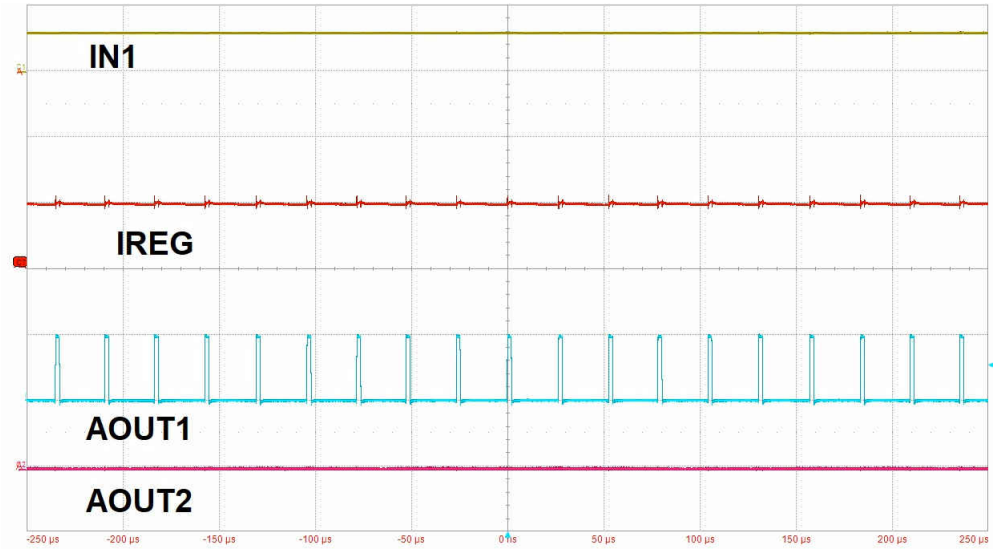


Figure 8-4. Driver Full On Operation with Current Regulation

8.3 Alternate Application

The following design procedure can be used to configure the DRV8426E/P to drive a stepper motor.

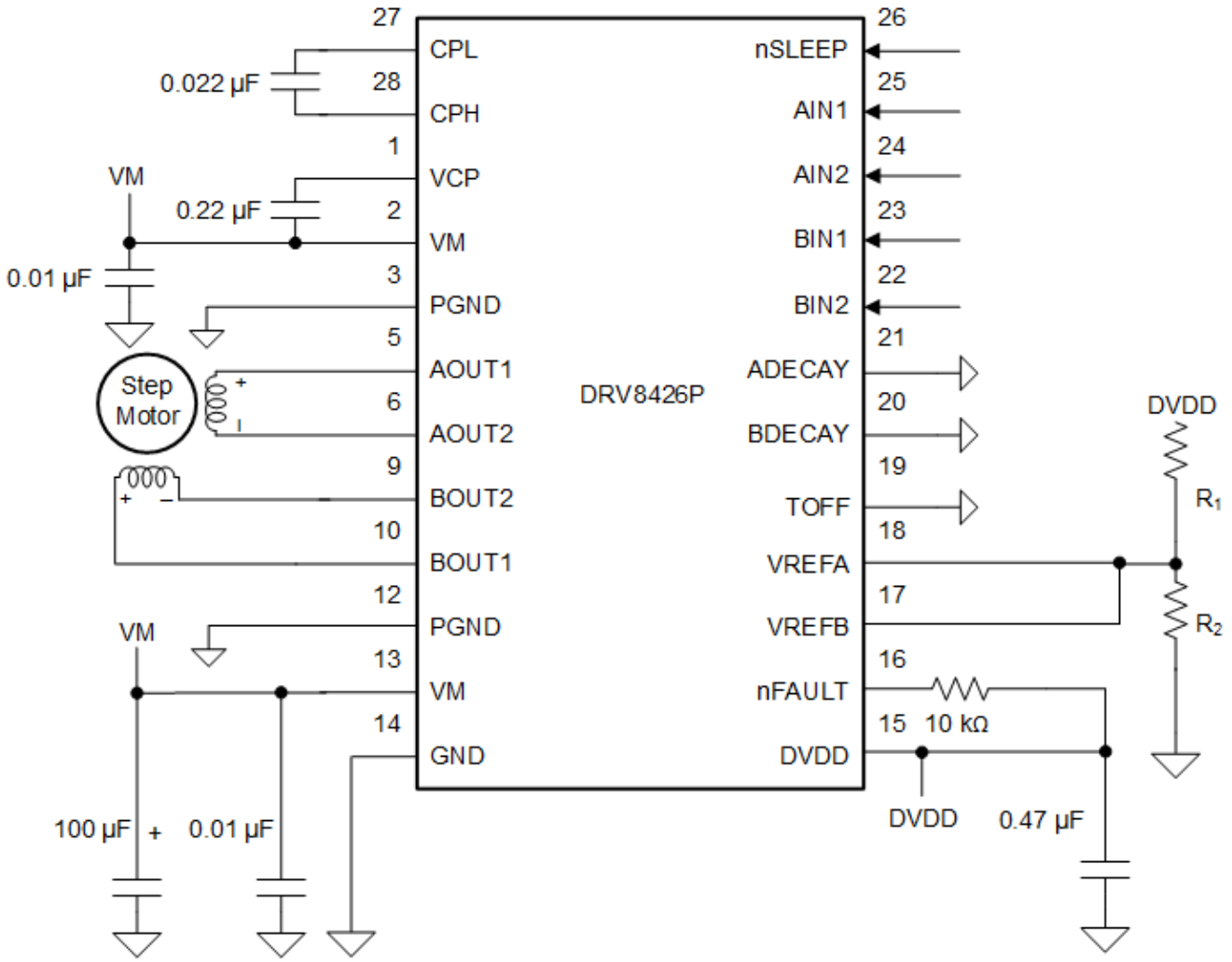


Figure 8-5. Alternate Application Schematic

8.3.1 Design Requirements

Table 8-2 gives design input parameters for system design.

Table 8-2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	6 Ω/phase
Motor winding inductance	L_L	4.1 mH/phase
Motor Full Step Angle	θ_{step}	1.8°/step
Target microstepping level	n_m	1/2 step
Target motor speed	v	90 rpm
Target full-scale current	I_{FS}	1 A

8.3.2 Detailed Design Procedure

8.3.2.1 Current Regulation

In a stepper motor, the full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the VREFx voltage. The maximum allowable voltage on the VREFx pins is 3.3 V. DVDD can be used to provide VREFx through a resistor divider.

I_{FS} (A) = V_{REF} (V) / 2.2 (V/A)

Note

The I_{FS} current must also follow Equation 1 to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{FS}\ (A) < \frac{VM\ (V)}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega)} \quad (1)$$

8.3.2.2 Power Dissipation and Thermal Calculation

The output current and power dissipation capabilities of the device are heavily dependent on the PCB design and external system conditions. This section provides some guidelines for calculating these values.

Total power dissipation for the device is composed of three main components. These are the power MOSFET $R_{DS(ON)}$ (conduction) losses, the power MOSFET switching losses and the quiescent supply current dissipation. While other factors may contribute additional power losses, these other items are typically insignificant compared to the three main items.

$P_{TOT} = P_{COND} + P_{SW} + P_Q$

For loads connected to VM, assuming that all the outputs are loaded with same current, total conduction loss can be expressed as -

P_{COND} = 4 x (I_{OUT})2 x $R_{DS(ONL)}$

As the high-side and low-side MOSFETs of the DRV8932 have the same on-resistance, the conduction loss will be independent of the duty cycle of the input PWM or the amount of PWM off-time. It should be noted that $R_{DS(ON)}$ has a strong correlation with the device temperature. A curve showing the normalized $R_{DS(ON)}$ with temperature can be found in the Typical Characteristics curves.

P_{COND} = 4 x $(0.6\text{-A})^2$ x 0.45-Ω = 0.648-W

P_{SW} can be calculated from the nominal supply voltage (VM), regulated output current (I_{OUT}), switching frequency (f_{PWM}) and the device output rise (t_{RISE}) and fall (t_{FALL}) time specifications. Assuming that all the four outputs are switching simultaneously -

$P_{SW} = 4 \times (P_{SW\_RISE} + P_{SW\_FALL})$

$P_{SW\_RISE} = 0.5 \times VM \times I_{OUT} \times t_{RISE} \times f_{PWM}$

$P_{SW\_FALL} = 0.5 \times VM \times I_{OUT} \times t_{FALL} \times f_{PWM}$

P_{SW_RISE} = 0.5 x 24 V x 0.6 A x 100 ns x 40 kHz = 0.0288 W

P_{SW_FALL}= 0.5 x 24 V x 0.6 A x 100 ns x 40 kHz = 0.0288 W

P_{SW} = 4 x (0.0288W + 0.0288W) = 0.2304 W

P_Q can be calculated from the nominal supply voltage (VM) and the I_{VM} current specification.

$P_Q = VM \times I_{VM}$ = 24 V x 5 mA = 0.12 W

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss.

$P_{TOT} = P_{COND} + P_{SW} + P_Q = 0.648\text{-W} + 0.2304\text{-W} + 0.12\text{-W} = 0.9984\text{-W}$

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as

$T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 33 °C/W for the HTSSOP package and 43 °C/W for the VQFN package.

Assuming 25°C ambient temperature, the junction temperature for the HTSSOP package is calculated as -

$T_J = 25°C + (0.9984\text{-W} \times 33°C/W) = 57.95\ °C$

The junction temperature for the VQFN package is calculated as -

$T_J = 25°C + (0.9984\text{-W} \times 43°C/W) = 67.93\ °C$

It should be ensured that the device junction temperature is within the specified operating region.

8.3.2.2.1 Decay Modes

The device supports several different decay modes: fast decay, mixed decay, and smart tune. The current through the motor windings is regulated using an adjustable fixed-time-off scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the device will place the winding in one of the decay modes for TOFF. After TOFF, a new drive phase starts.

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply (VM) range from 4.5 V to 33 V. A 0.01-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the device as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

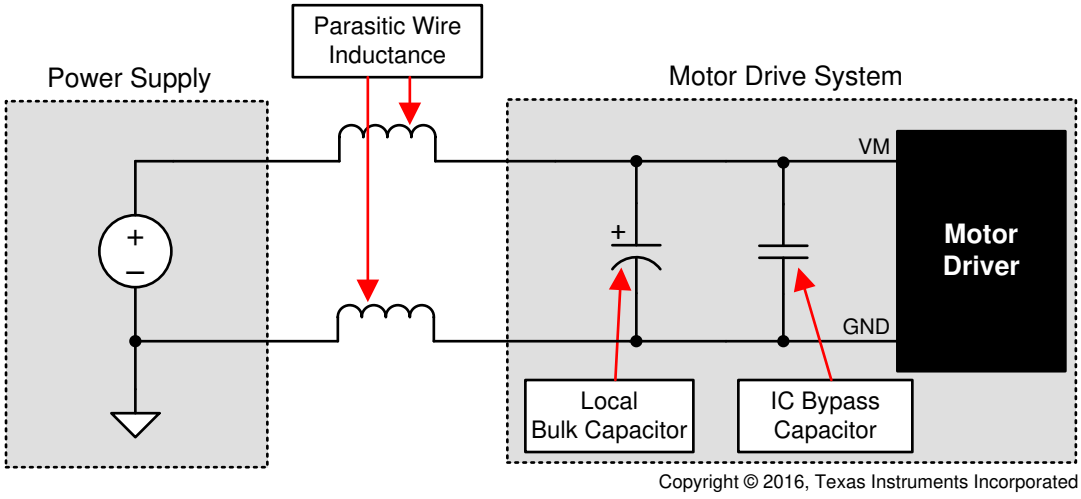


Figure 9-1. Example Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to PGND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device PGND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.022 µF rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.22 µF rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 0.47 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.

The thermal PAD must be connected to system ground.

10.1.1 Layout Example

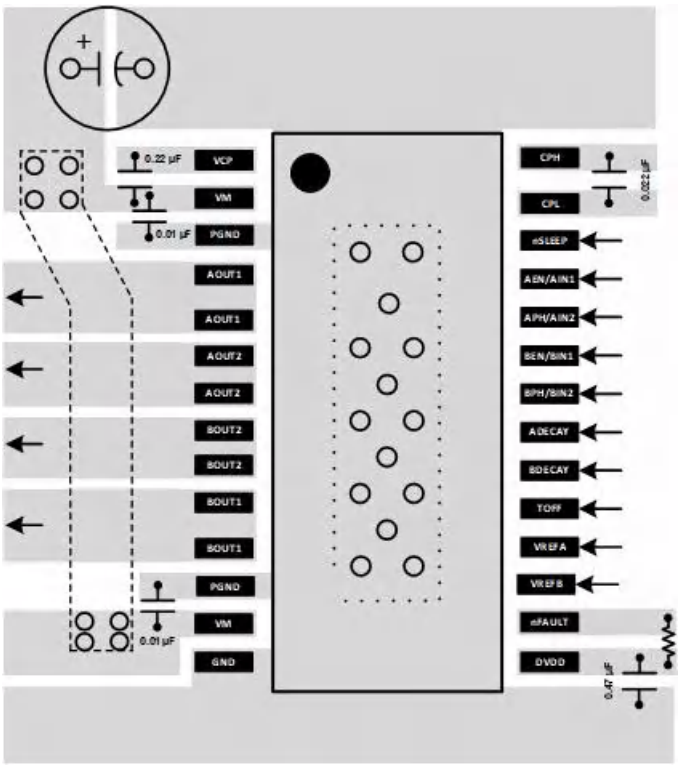


Figure 10-1. HTSSOP Layout Example

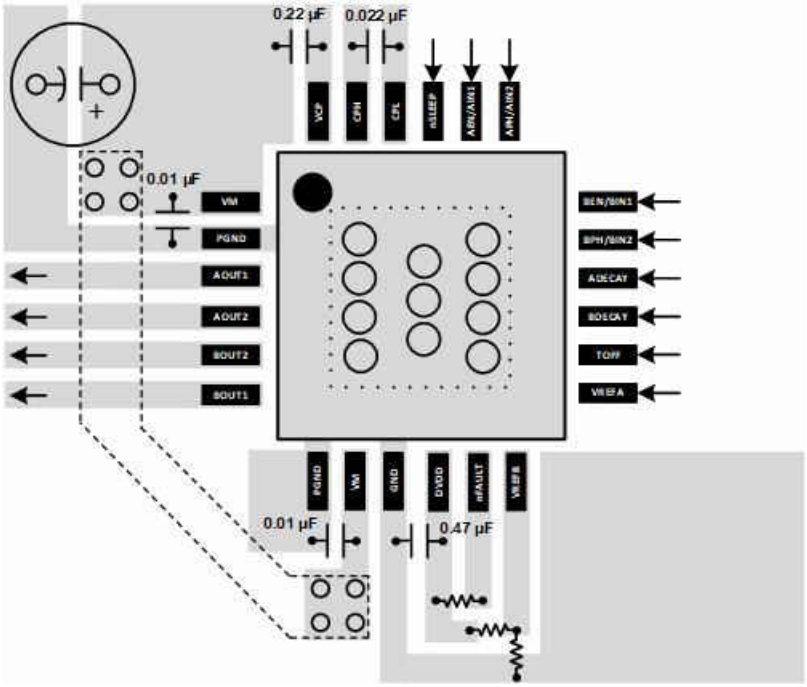


Figure 10-2. QFN Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *High Resolution Microstepping Driver With the DRV88xx Series* application report

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 11-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DRV8426E	Click here	Click here	Click here	Click here	Click here
DRV8426P	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

11.5 Trademarks

All trademarks are the property of their respective owners.

12 Mechanical, Packaging, and Orderable Information

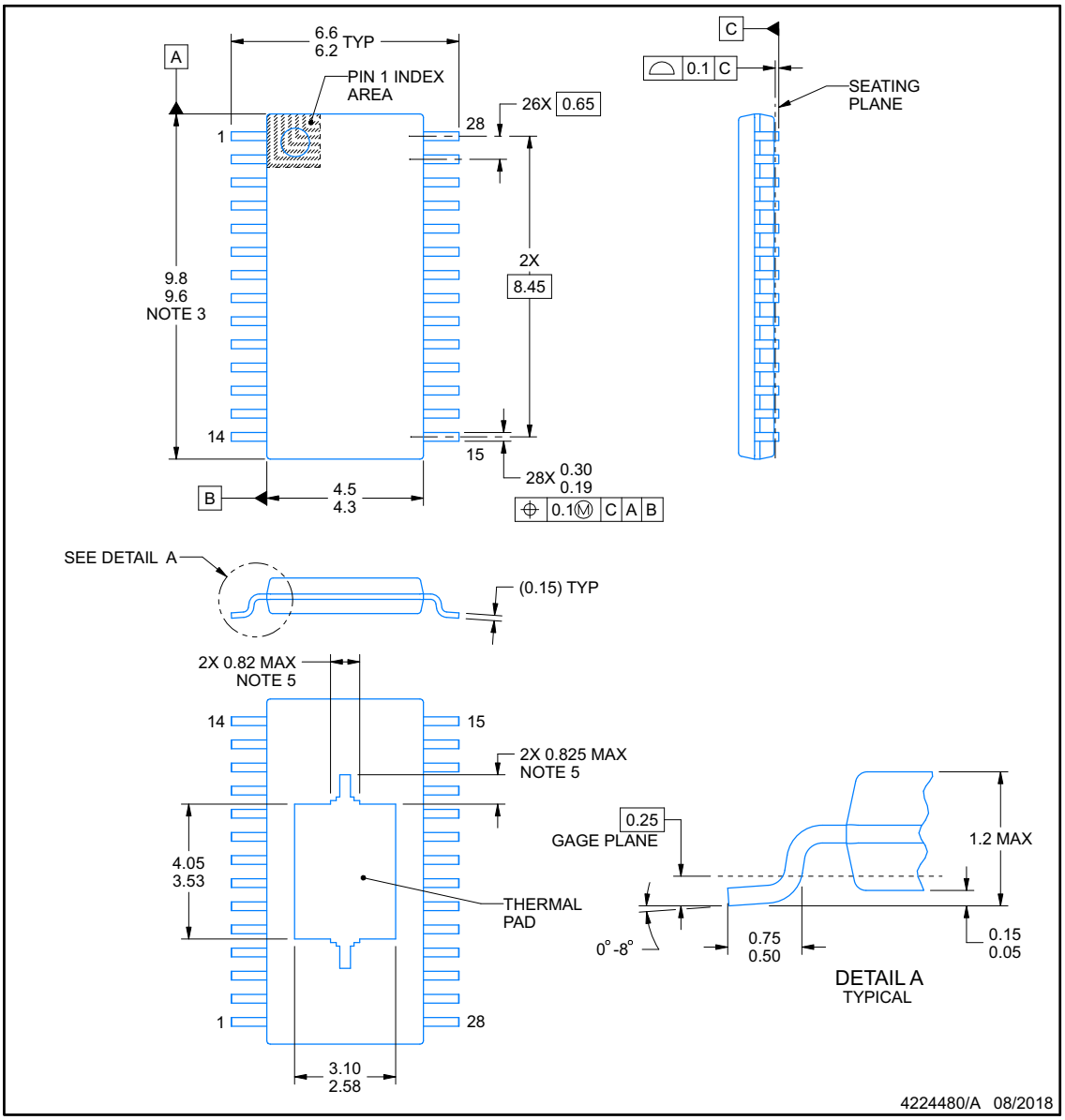
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

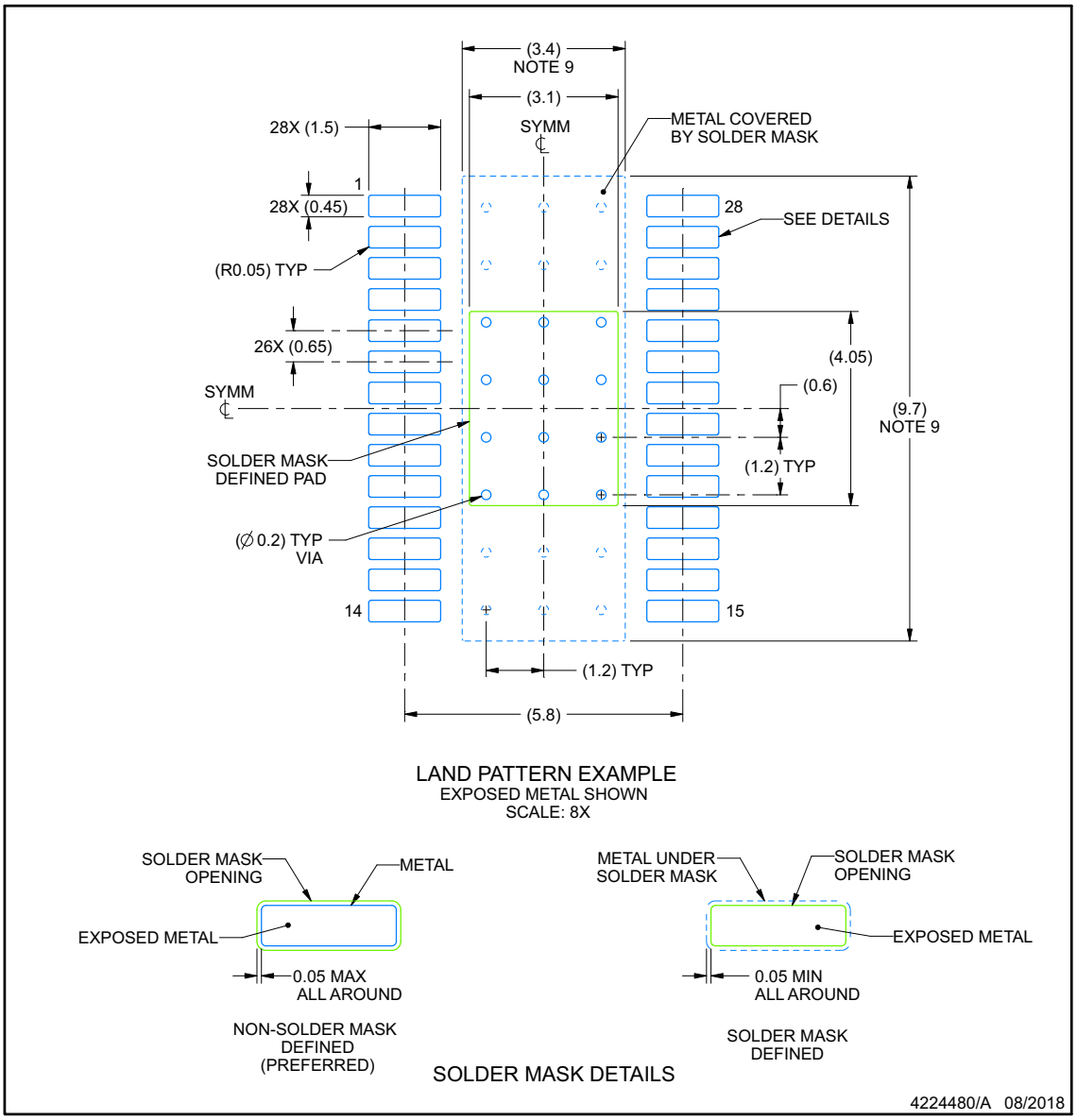
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



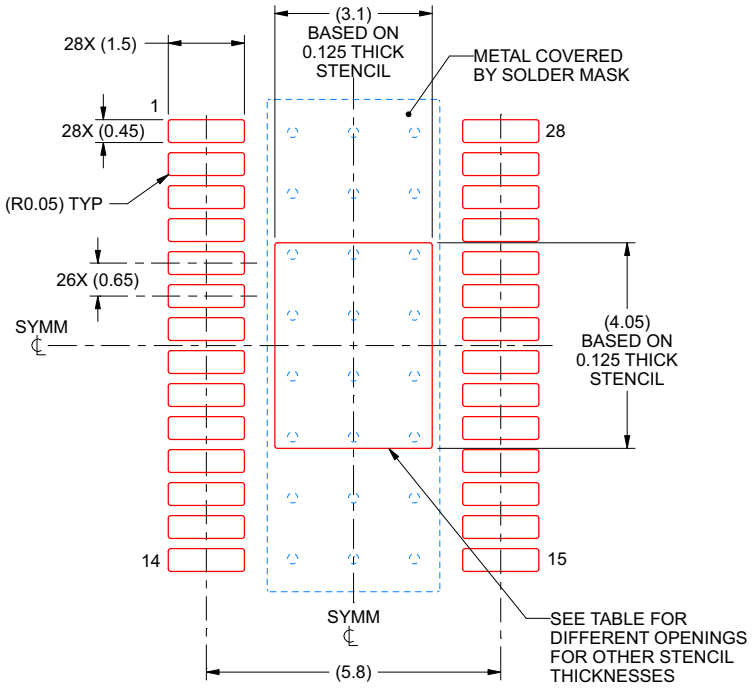
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0028M — **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 4.53
0.125	3.10 X 4.05 (SHOWN)
0.15	2.83 X 3.70
0.175	2.62 X 3.42

4224480/A 08/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8426EPWPR	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8426E	Samples
DRV8426ERGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8426E	Samples
DRV8426PPWPR	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8426P	Samples
DRV8426PRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8426P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

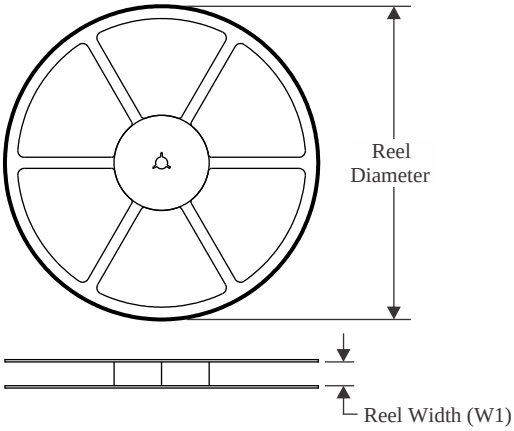
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

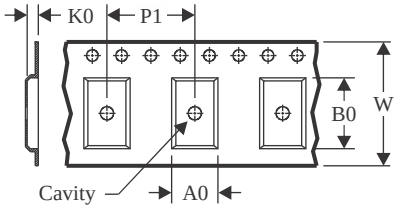
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

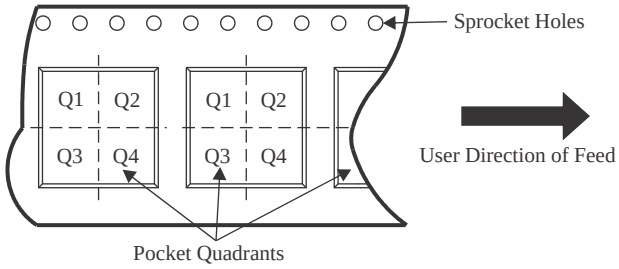


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

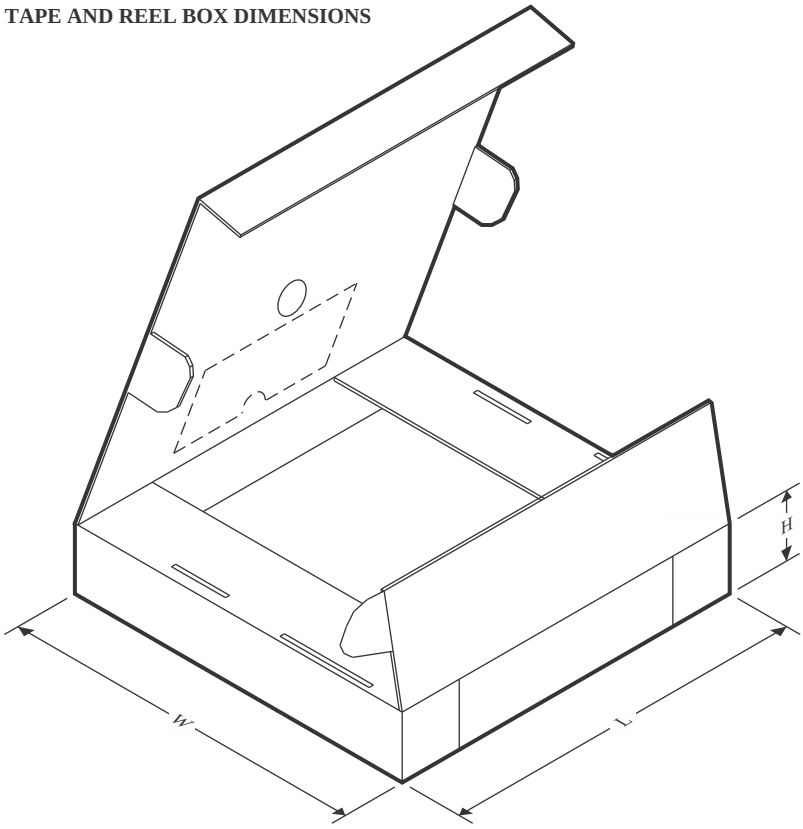
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8426EPWPR	HTSSOP	PWP	28	2500	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
DRV8426ERGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV8426PPWPR	HTSSOP	PWP	28	2500	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
DRV8426PRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8426EPWPR	HTSSOP	PWP	28	2500	356.0	356.0	35.0
DRV8426ERGER	VQFN	RGE	24	3000	367.0	367.0	35.0
DRV8426PPWPR	HTSSOP	PWP	28	2500	356.0	356.0	35.0
DRV8426PRGER	VQFN	RGE	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

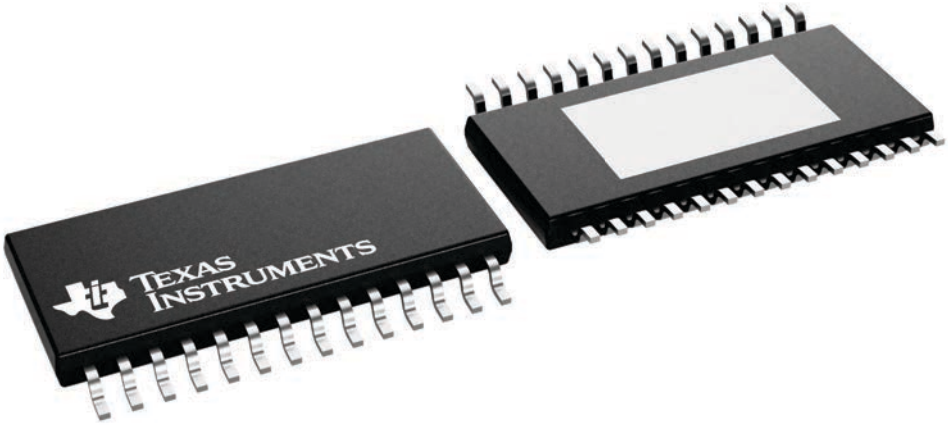
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

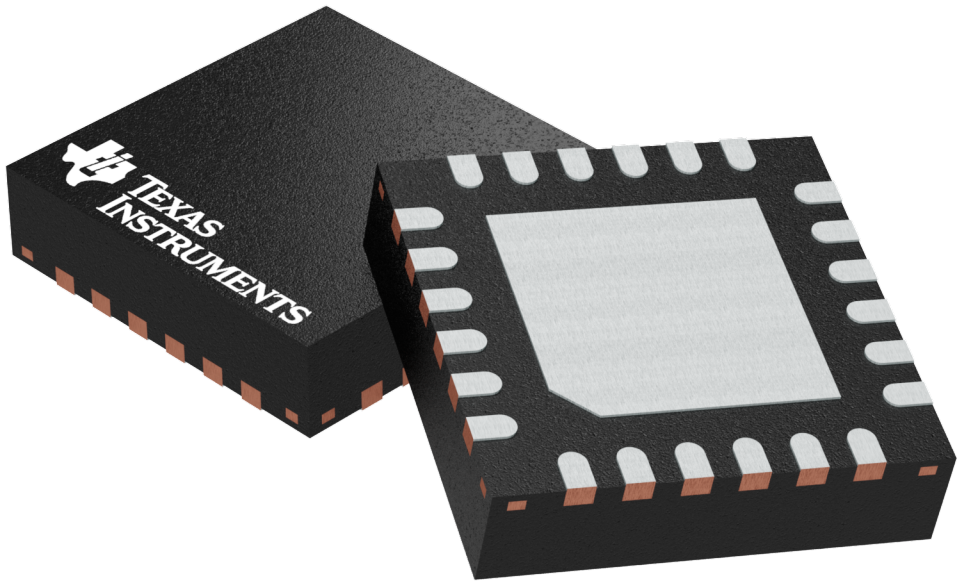


4224765/B

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

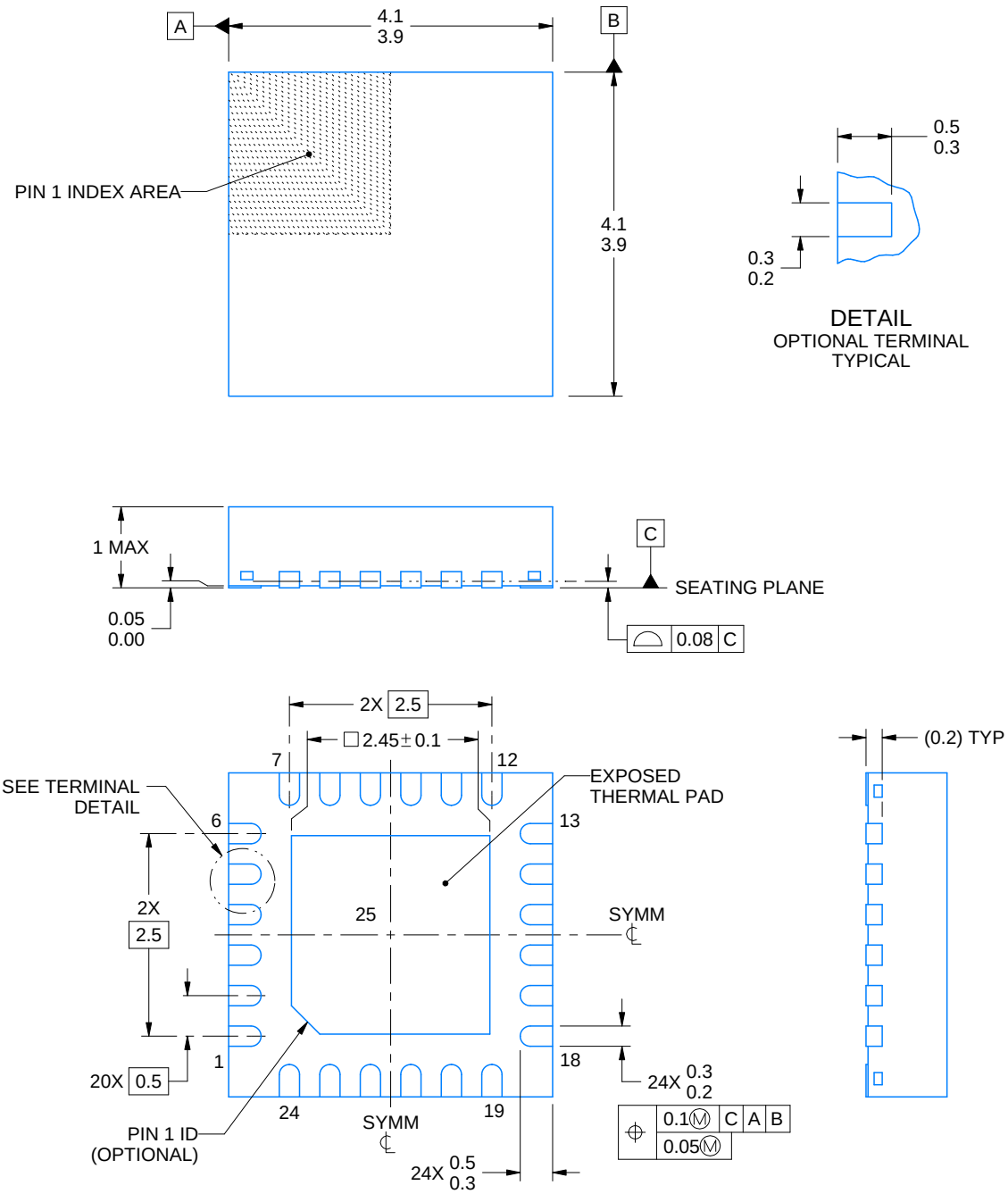
4204104/H

PACKAGE OUTLINE

RGE0024B

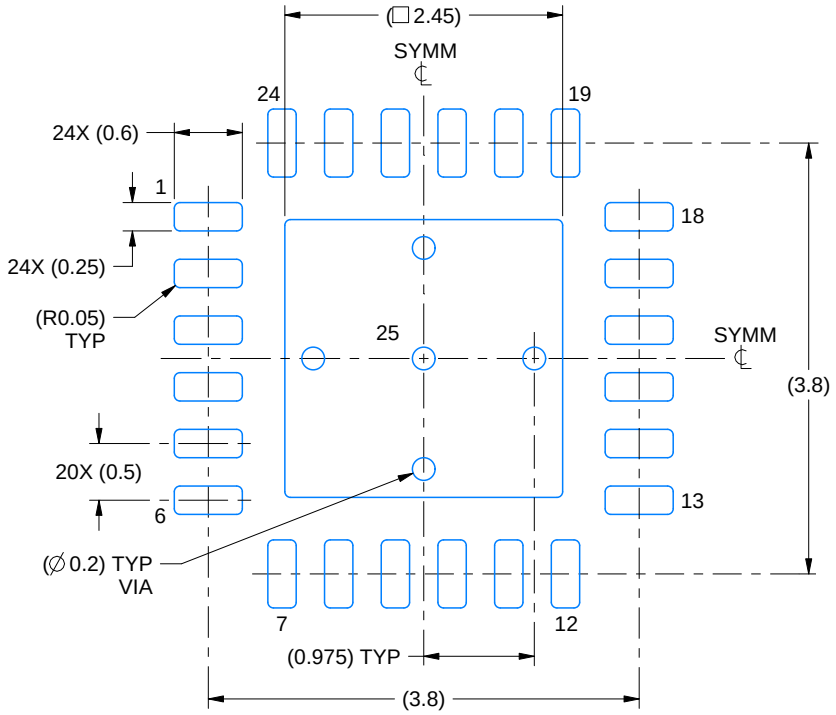
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

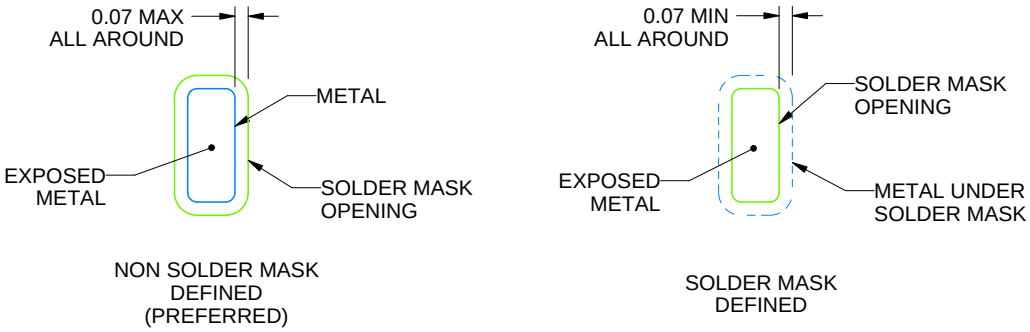


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

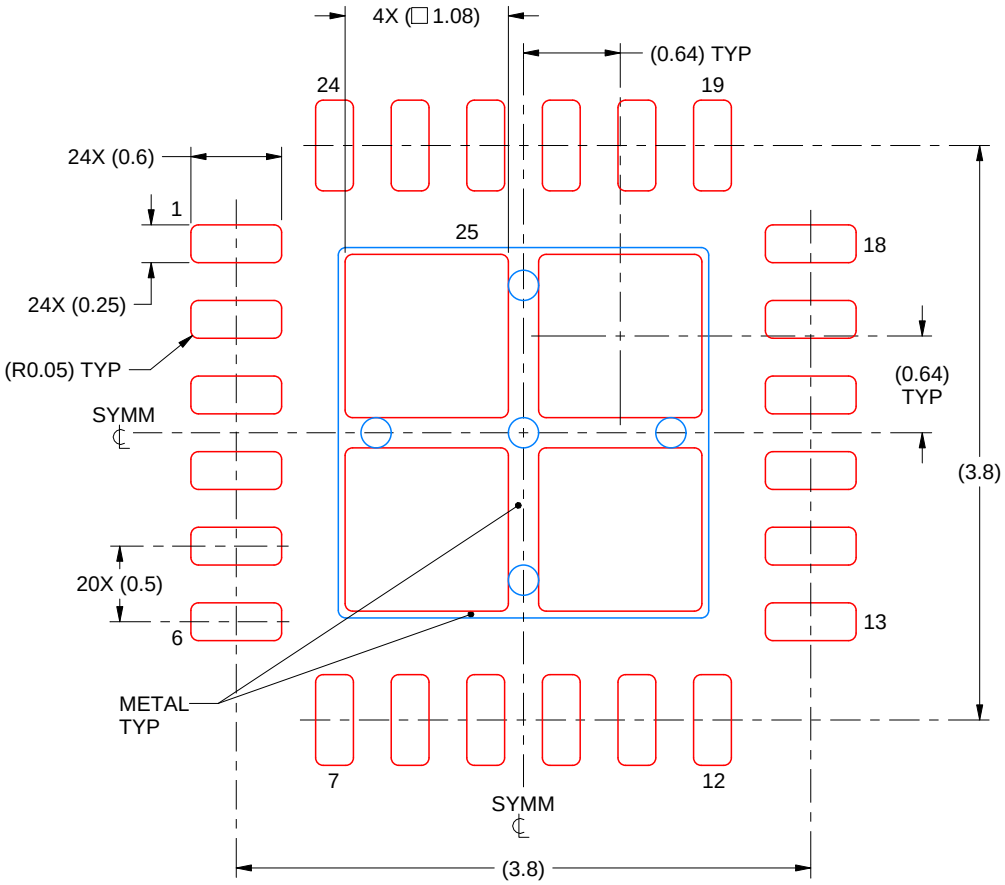


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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