TPS7A6650H-Q1 40-V, Ultralow-$I_{(q)}$, 150°C-Ambient-Temperature Regulator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature: –40°C to 150°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4
- 4-V to 40-V Wide Vin Input Voltage Range With up to 45-V Transient
- Output Current: 50 mA
- Low Quiescent Current, $I_{(q)}$:
  - 2 µA when EN = Low (Shutdown Mode)
  - 12 µA Typical at Light Loads
- Low ESR Ceramic Output Stability Capacitor (2.2 µF–100 µF)
- 130-mV Dropout Voltage at 50 mA (Typical, $V_{(Vin)}$ = 4 V)
- Fixed 5-V Output Voltage
- Low Input Voltage Tracking
- Integrated Power-On Reset
  - Programmable Reset-Pulse Delay
  - Open-Drain Reset Output
- Integrated Fault Protection
  - Thermal Shutdown
  - Short-Circuit Protection
- 8-Pin MSOP-DGN Package

2 Applications

- Powertrain Sensor Module
- Infotainment Systems With Sleep Mode
- Body Control Modules
- Always-On Battery Applications
  - Gateway Applications
  - Remote Keyless Entry Systems
  - Immobilizers

3 Description

The TPS7A6650H-Q1 is a low-dropout linear regulator designed for up to 40-V Vin operations. With only 12-µA quiescent current at no load, it is quite suitable for standby microprocessor control-unit systems, especially in automotive applications.

The device features integrated short-circuit and overcurrent protection. The device implements reset delay on power up to indicate the output voltage is stable and in regulation. One can program the delay with an external capacitor. A low-voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold-crank conditions.

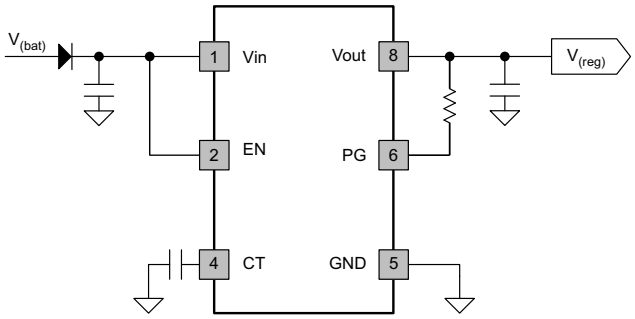
The device operates in the –40°C to 150°C temperature range, which makes it well suited for power supplies in various automotive applications.

Device Information(1)

DEVICE NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A6650H-Q1	HVSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Hardware-Enable Option



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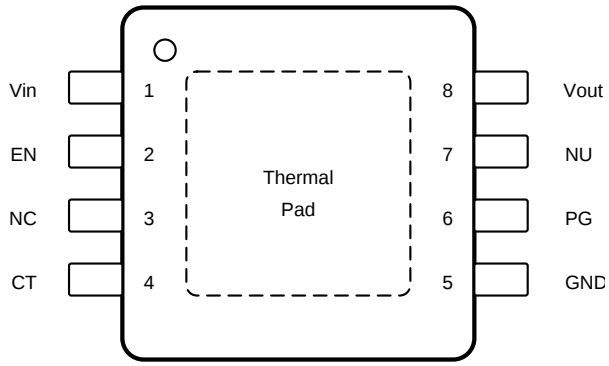
4 Revision History

DATE	REVISION	NOTES
November 2015	*	Initial release

5 Pin Configuration and Functions

8-Pin HVSSOP
DGN Package
Top View



NC – No internal connection

NU – Make no external connection

Pin Functions

PIN NAME	PIN NO.	TYPE	DESCRIPTION
CT	4	O	Reset-pulse delay adjustment. Connect this pin via a capacitor to GND
EN	2	I	Enable pin. The device enters the standby state when the enable pin becomes lower than the threshold.
NU	7	I	Not-used pin; make no external connection
GND	5	G	Ground reference
NC	3	—	Not-connected pin
PG	6	O	Output ready. This open-drain pin must connect to Vout via an external resistor. The output voltage going below threshold pulls it down.
Vin	1	P	Input power-supply voltage
Vout	8	O	Output voltage
—	—	—	Thermal pad

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Vin, EN	Unregulated input (2) (3)	–0.3	45	V
Vout	Regulated output	–0.3	7	V
CT		–0.3	25	V
PG		–0.3	Vout	V
T_J	Operating junction temperature range	–40	160	°C
T_{stg}	Storage temperature range	–65	160	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND
(3) Absolute maximum voltage, withstand 45 V for 200 ms

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]		±4000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±1000	
			Corner pins (1, 4, 5, and 8)	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Vin	Unregulated input	4	40	V
EN		0	40	V
CT		0	20	V
Vout		1.5	5.5	V
PG	Low voltage (I/O)	0	5.5	V
T_A	Operating ambient temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS7A6650H-Q1 DGN (HVSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance[2]	37.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

6.5 Electrical Characteristics

$V_{(Vin)}$ = 14 V, 1 mΩ < ESR < 2 Ω, T_J = –40°C to 160°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (Vin)						
$V_{(Vin)}$	Input voltage	I_O = 1 mA	5.5		40	V
$I_{(q)}$	Quiescent current	$V_{(Vin)}$ = 5.5 V to 40 V, EN = ON, I_O = 0.2 mA		12	22	µA
$I_{(Sleep)}$	Input sleep current	No load current and EN = OFF			4	µA
$I_{(EN)}$	EN pin current	$V_{(EN)}$ = 40 V			1	µA
$V_{(VinUVLO)}$	Undervoltage detection	Ramp $V_{(Vin)}$ down until output turns OFF			2.6	V
$V_{(UVLOhys)}$	Undervoltage hysteresis			1		V
ENABLE INPUT (EN)						
V_{IL}	Logic input low level		0		0.4	V
V_{IH}	Logic input high level		1.7			V

Electrical Characteristics (continued)

$V_{(Vin)}$ = 14 V, 1 mΩ < ESR < 2 Ω, T_J = –40°C to 160°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REGULATED OUTPUT (Vout)						
$V_{(Vout)}$	Regulated output	I_O = 1 mA, T_J = 25°C	–1%		1%	
		$V_{(Vin)}$ = 6 V to 40 V, I_O = 1 mA to 50 mA	–2%		2%	
$V_{(line-reg)}$	Line regulation	$V_{(Vin)}$ = 5.5 V to 40 V, I_O = 50 mA			5	mV
$V_{(load-reg)}$	Load regulation	I_O = 1 mA to 50 mA			20	mV
$V_{(dropout)}$	Dropout voltage	$V_{(dropout)} = V_{(Vin)} – V_{(Vout)}$, I_{OUT} = 50 mA		130	240	mV
I_O	Output current	$V_{(Vout)}$ in regulation	0		50	mA
$I_{(lreg-CL)}$	Output current limit	$V_{(Vout)}$ short to ground		500	800	mA
PSRR	Power supply ripple rejection(1)	$V_{(Vin)}$ = 12 V, I_L = 10 mA, output capacitance = 2.2 µF,				
		$V_{(Vin)}$ = 12 V, I_L = 10 mA, output capacitance = 2.2 µF, frequency = 100 Hz		60		dB
		$V_{(Vin)}$ = 12 V, I_L = 10 mA, output capacitance = 2.2 µF, frequency = 100 kHz		40		dB
RESET (PG)						
V_{OL}	Reset output, low voltage	I_{OL} = 0.5 mA			0.4	V
I_{lkg}	Leakage current	Reset pulled Vout through 10-kΩ resistor			1	µA
$V_{(TH-POR)}$	Power-on-reset threshold	$V_{(Vout)}$ increasing	89.6	91.6	93.6	% of Vout
$V_{(Thres)}$	Hysteresis			2		% of Vout
RESET DELAY (CT)						
$I_{(Chg)}$	Delay-capacitor charging current	$V_{(CT)}$ = 0 V		1.4		µA
$V_{(th)}$	Threshold to release PG high			1		V
OPERATING TEMPERATURE RANGE						
T_J	Junction temperature		–40		160	°C
$T_{(shutdown)}$	Junction shutdown temperature			175		°C
$T_{(hyst)}$	Hysteresis of thermal shutdown			20		°C

(1) Design information – Not tested

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

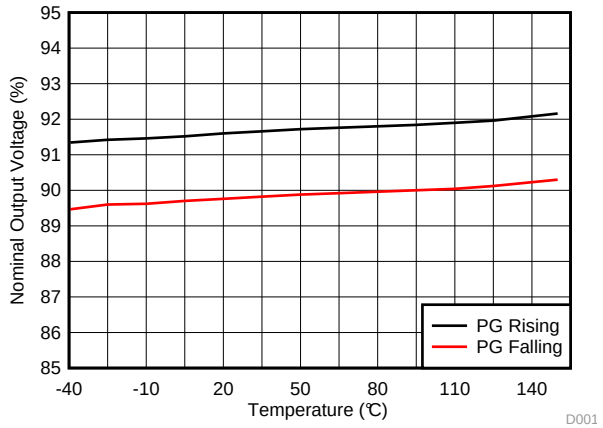
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING FOR RESET (PG)						
$t_{(POR)}$	Power-on-reset delay	Where C = delay capacitor value; capacitance C = 100 nF(1)	50	100	180	ms
$t_{(POR-fixed)}$		No capacitor on pin	100	290	650	µs
$t_{(Deglitch)}$	Reset deglitch time		20	250		µs

(1) This information only is not tested in production and equation basis is (C × 1) / 1 × 10^{-6} = t_d (delay time).
Where C = Delay capacitor value. Capacitance C range = 100 pF to 100 nF.

6.7 Qualification Summary

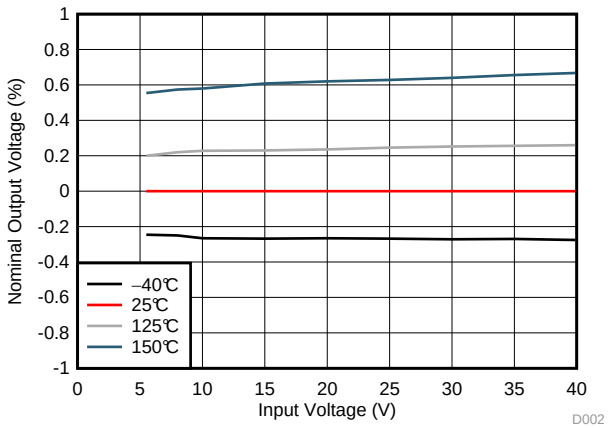
The TPS7A6650H-Q1 device has passed all the Grade 0 level qualification items required in AEC-Q100 with one exception: High temperature storage lifetime (HTSL). For the HTSL item, the Grade 0 level requirement is passing 175ºC for 1000 hours of stress. For this device, it passed at 160°C for 1000 hours stress.

6.8 Typical Characteristics



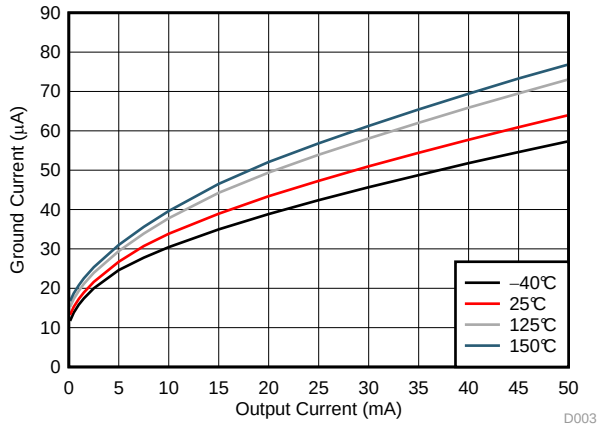
Vin = 14 V No Load

Figure 1. Power-Good Threshold Voltage vs Temperature



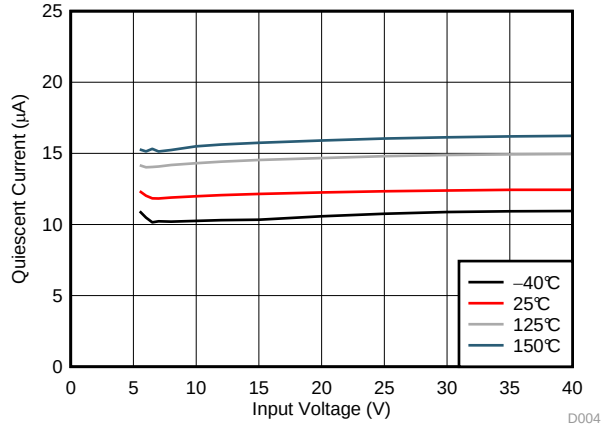
Vin = 14 V I_L = 1 mA

Figure 2. Line Regulation



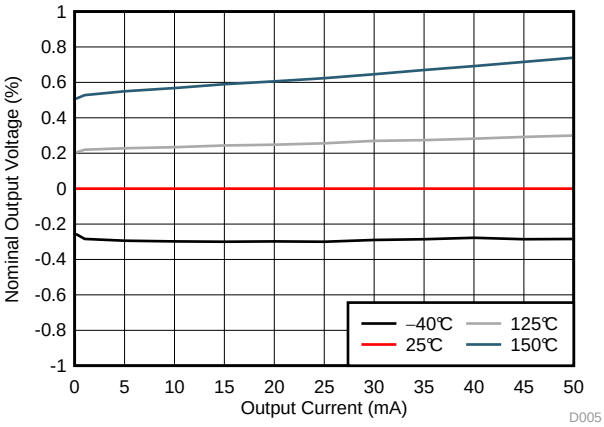
Vin = 14 V

Figure 3. Ground Current vs Output Current



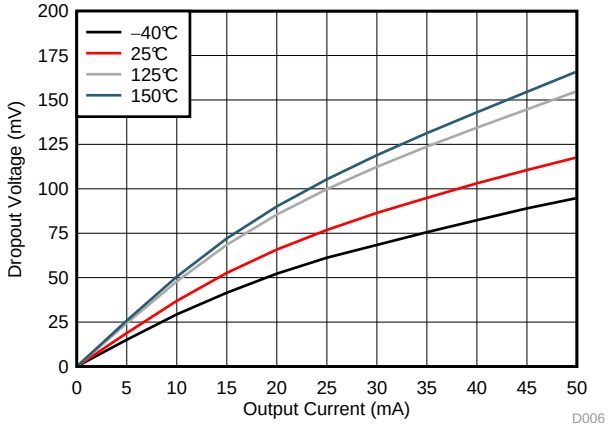
I_L = 0

Figure 4. Quiescent Current vs Input Voltage



Vin = 14 V

Figure 5. Load Regulation



Vin = 4 V

Figure 6. Dropout Voltage vs Output Current

Typical Characteristics (continued)

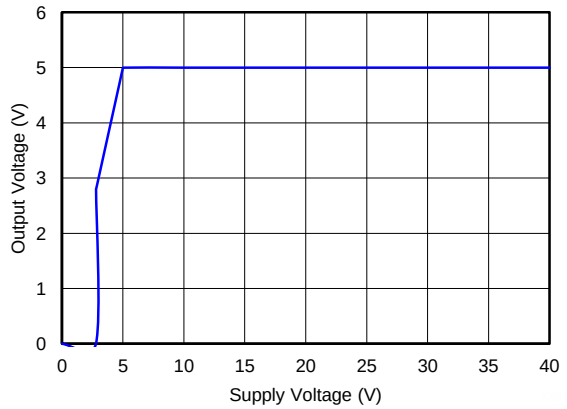


Figure 7. Output Voltage vs Supply Voltage (Fixed 5-V Version, I_L = 0)

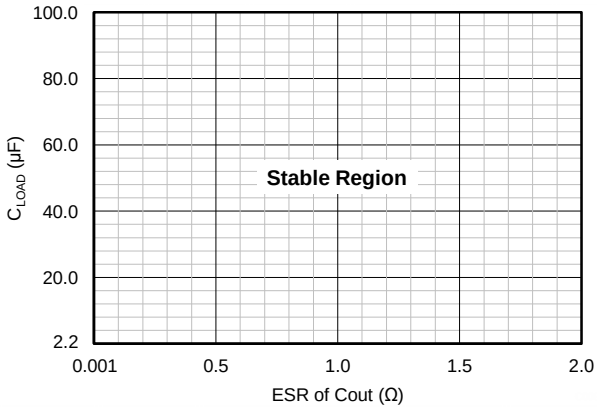


Figure 8. Load Capacitance vs ESR Stability

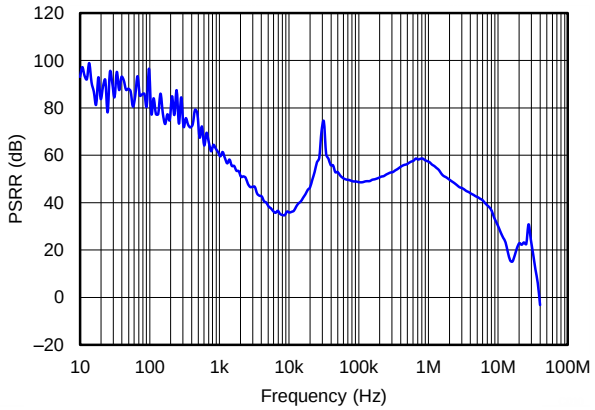


Figure 9. Power-Supply Rejection Ratio vs Frequency

All oscilloscope waveforms were taken at room temperature.

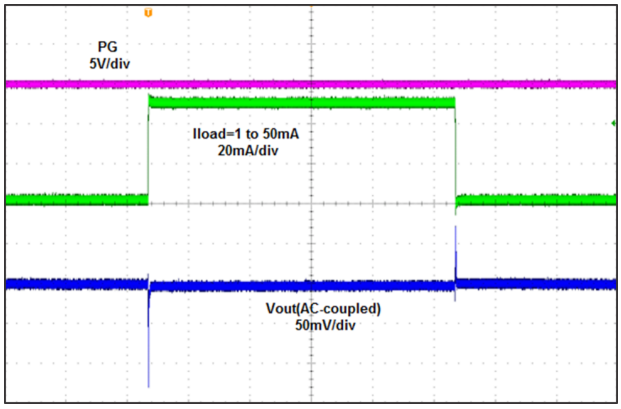


Figure 10. Load Transient Response, 10 ms/div

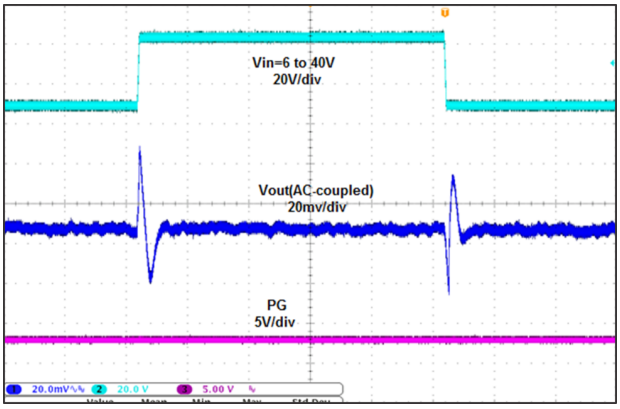


Figure 11. Line Transient Response, I_L = 1 mA, 1 V/µs

Typical Characteristics (continued)

All oscilloscope waveforms were taken at room temperature.

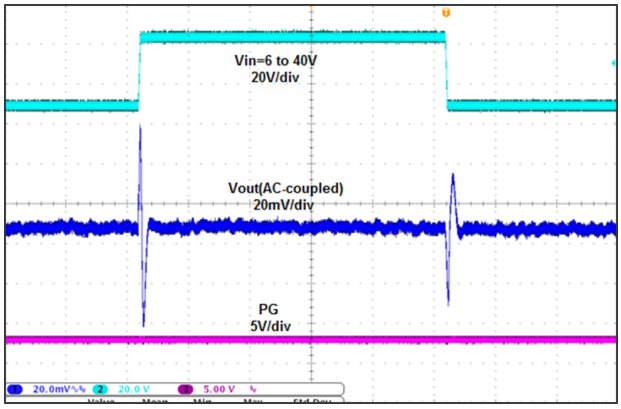


Figure 12. Line Transient Response, I_L = 10 mA, 1 V/µs

7 Detailed Description

7.1 Overview

This product is a combination of a low-dropout linear regulator with reset function. The power-on reset initializes once the Vout output exceeds 91.6% of the target value. The power-on-reset delay is a function of the value set by an external capacitor on the CT pin before releasing the PG pin high.

7.2 Functional Block Diagram

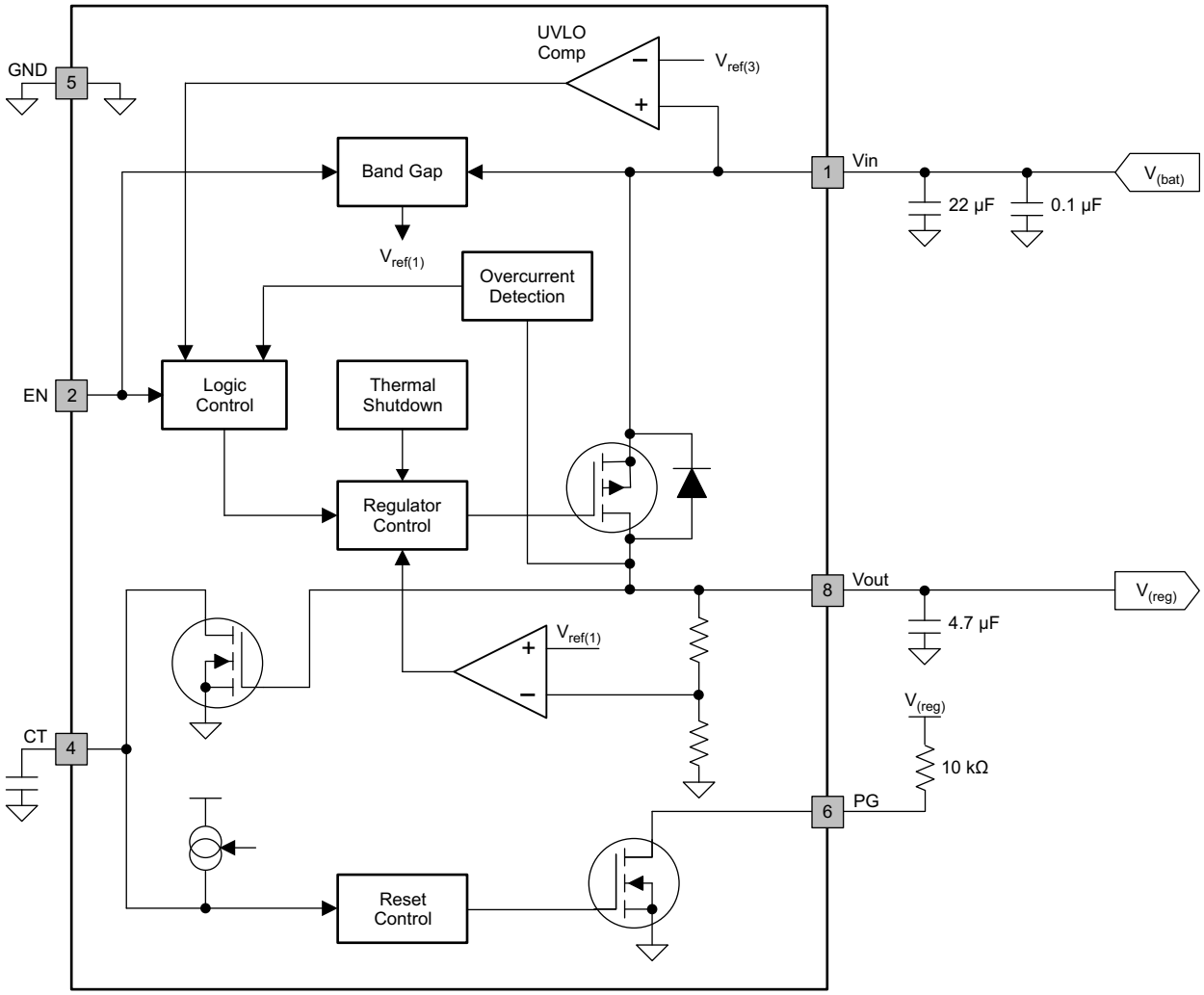


Figure 13. TPS7A6650H-Q1 Functional Block Diagram

7.3 Feature Description

7.3.1 Enable (EN)

This is a high-voltage-tolerant pin; high input activates the device and turns the regulator ON. One can connect this input to the Vin pin for self-bias applications.

7.3.2 Regulated Output (Vout)

This is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft start incorporated to control initial current through the pass element and the output capacitor.

Feature Description (continued)

In the event the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

7.3.3 Power-On Reset (PG)

This is an output with an external pullup resistor to the regulated supply. The output remains low until the regulated Vout has exceeded approximately 90% of the set value and the power-on-reset delay has expired. The on-chip oscillator presets the delay. The regulated output falling below the 90% level asserts this output low after a short de-glitch time of approximately 250 µs (typical).

7.3.4 Reset Delay Timer (CT)

An external capacitor on this pin sets the timer delay before the reset pin is asserted high. The constant output current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator. If this pin is open, the default delay time is 290 µs (typ). After releasing the PG pin high, the capacitor on this pin discharges, thus allowing the capacitor to charge from approximately 0.2 V for the next power-on-reset delay-timer function.

An external capacitor, CT, defines the reset-pulse delay time, $t_{(POR)}$, with the charge time of:

$$t_{(POR)} = \frac{C_{(CT)} \times 1\,V}{1\,\mu A} \quad (1)$$

The power-on reset initializes once the output $V_{(Vout)}$ exceeds 91.6% of the programmed value. The power-on-reset delay is a function of the value set by an external capacitor on the CT pin before the releasing of the PG pin high.

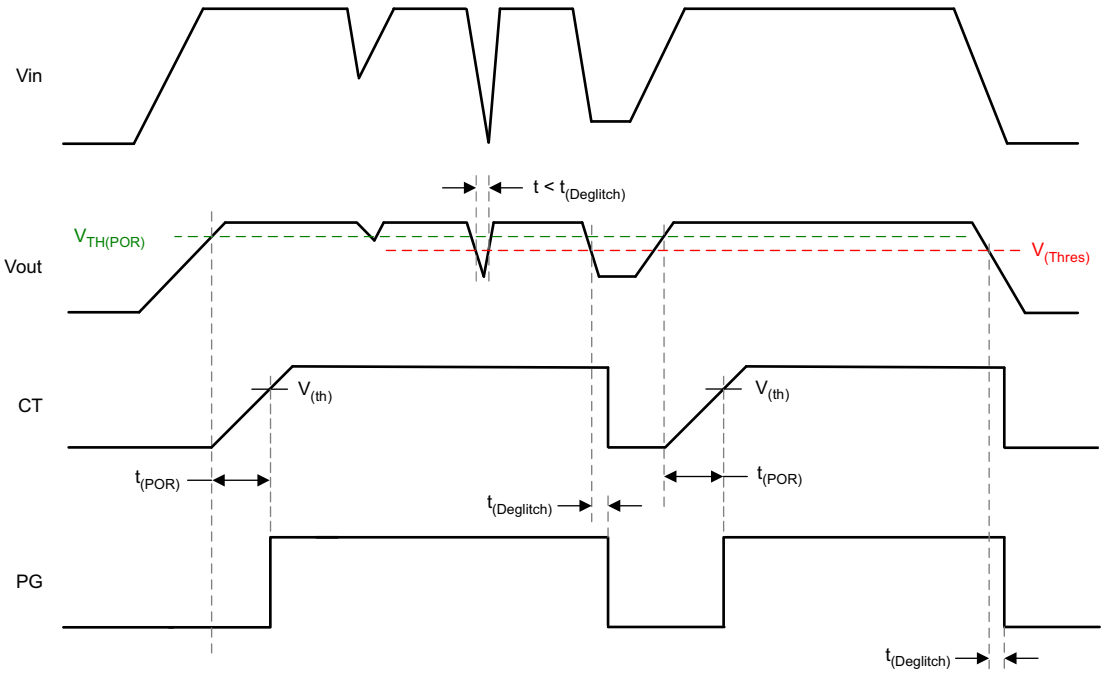


Figure 14. Conditions for Activation of Reset

Feature Description (continued)

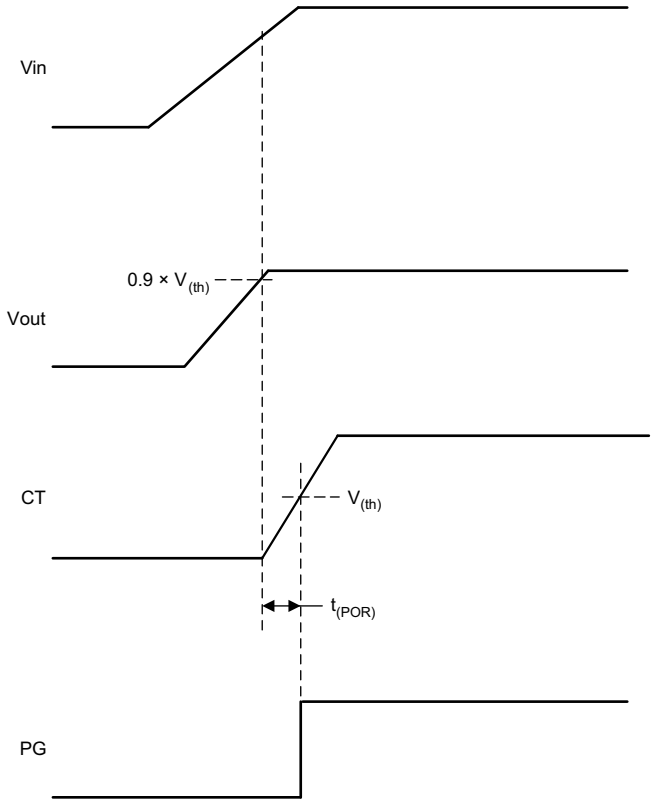


Figure 15. External Programmable Reset Delay

7.3.5 Undervoltage Shutdown

There is an internally fixed undervoltage shutdown threshold. Undervoltage shutdown activates when the input voltage on Vin drops below $V_{(VinUVLO)}$. This ensures the regulator is not latched into an unknown state during low input supply voltage. If the input voltage has a negative transient which drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence once the input voltage is above the required levels.

7.3.6 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current (I_O) and switch resistance ($R_{(SW)}$). This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold-crank conditions.

7.3.7 Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point, the output turns on again.

Thermal protection disables the output when the junction temperature rises to approximately 175°C, allowing the device to cool. Cooling of the junction temperature to approximately 155°C enables the output circuitry. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Feature Description (continued)

The purpose of the design of the internal protection circuitry of the TPS7A6650H-Q1 is for protection against overload conditions, not as a replacement for proper heat-sinking. Continuously running the TPS7A6650H-Q1 device into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Operation With $V_{(VIN)}$ < 4 V

The devices operate with input voltages above 4 V. The maximum UVLO voltage is 2.6 V, and the devices operate at an input voltage above 4 V. The devices can also operate at lower input voltages; no minimum UVLO voltage is specified. At input voltages below the actual UVLO voltage, the devices do not operate.

7.4.2 Operation With EN Control

The enable rising edge threshold voltage is 1.7 V (maximum). With the EN pin held above that voltage and the input voltage above 4 V, the device becomes active. The enable falling edge is 0.4 V (minimum). Holding the EN pin below that voltage disables the device, thus reducing the IC quiescent current.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A6650H-Q1 device is a 150-mA low-dropout linear regulator designed for up to 40-V Vin operation with only 12-µA quiescent current at no load.

8.2 Typical Application

Figure 16 shows a typical application circuits for the TPS7A6650H-Q1. One may use different values of external components, depending on the end application. An application may require a larger output capacitor during fast load steps in order to prevent reset from occurring. TI recommends a low-ESR ceramic capacitor with dielectric of type X7R or X8R.

8.2.1 TPS7A6650H-Q1 Typical Application

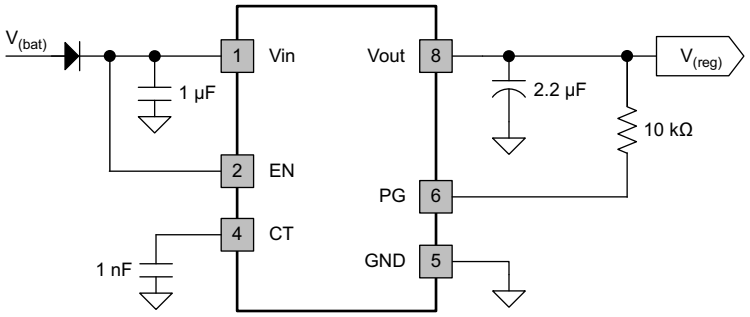


Figure 16. Typical Application Schematic for TPS7A6650H-Q1

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the design parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4 V to 40 V
Output voltage	5 V
Output current rating	50 mA
Output capacitor range	2.2 µF to 100 µF
Output capacitor ESR range	1 mΩ to 2 Ω
CT capacitor range	100 pF to 100 nF

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor
- Power-up-reset delay time

8.2.1.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 10 µF. The voltage rating must be greater than the maximum input voltage.

8.2.1.2.2 Output Capacitor

The device requires an output capacitor to stablize the output voltage. The capacitor value should be between 2.2 µF and 100 µF. The ESR range should be between 1 mΩ and 2 Ω. TI recommends to selecting a ceramic capacitor with low ESR to improve the load transient response.

8.2.1.3 Application Performance Plot

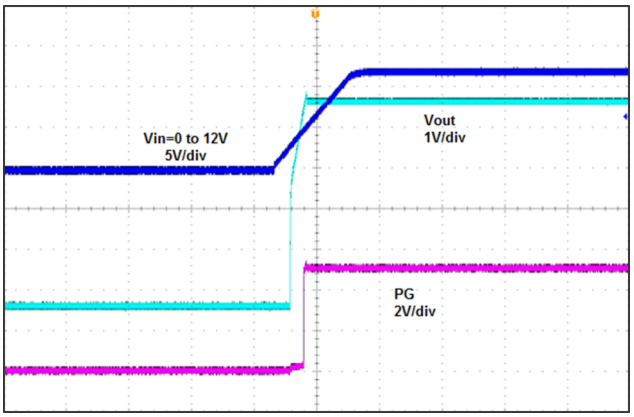


Figure 17. Power Up (5 V), 20 ms/div, I_L = 20 mA

9 Power Supply Recommendations

Design of the device is for operation from an input voltage supply with a range between 4 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7A6650H-Q1 device, TI recommends adding an electrolytic capacitor with a value of 22 µF and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

10.1.1 Package Mounting

Solder pad footprint recommendations for the TPS7A6650H-Q1 are available at the end of this product data sheet and at www.ti.com.

10.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

For the layout of TPS7A6650H-Q1, place the input and output capacitors close to the devices as shown in Figure 18. In order to enhance the thermal performance, TI recommends surrounding the device with some vias.

To improve ac performance such as PSRR, output noise, and transient response, TI recommends a board design with separate ground planes for Vin and Vout, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Minimize equivalent series inductance (ESL) and ESR in order to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance specified in this product data sheet, use the same layout pattern used for the TPS7A6650H-Q1 evaluation board, available at www.ti.com.

10.2 Layout Example

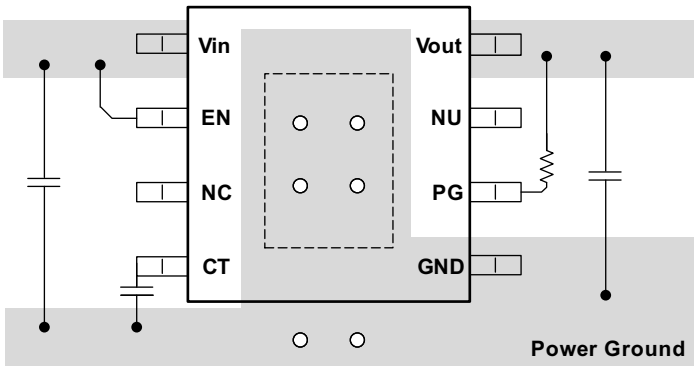


Figure 18. TPS7A6650H-Q1 Board Layout Diagram

10.3 Power Dissipation and Thermal Considerations

Calculate power dissipated in the device using Equation 2.

$$P_D = I_O \times (V_{(Vin)} - V_{(Vout)}) + I_{(q)} \times V_{(Vin)} \quad (2)$$

where:

- P_D = continuous power dissipation
- I_O = output current
- $V_{(Vin)}$ = input voltage
- $V_{(Vout)}$ = output voltage

As $I_{(q)}$ << I_O, therefore ignore the term $I_{(q)} \times V_{(Vin)}$ in Equation 2.

For a device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) using Equation 3.

Power Dissipation and Thermal Considerations (continued)

$$T_J = T_A + (R_{\theta JA} \times P_{D)}) \quad (3)$$

where:

$R_{\theta JA}$ = junction-to-ambient air thermal impedance

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_{D)}) \quad (4)$$

11 Device and Documentation Support

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.1 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A6650HQDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	13LV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

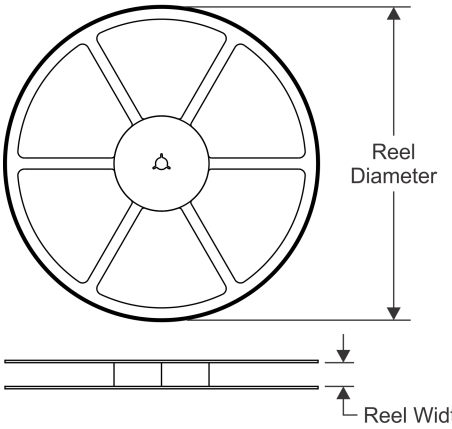
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

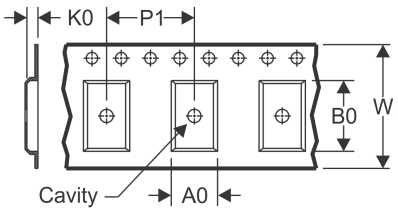
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

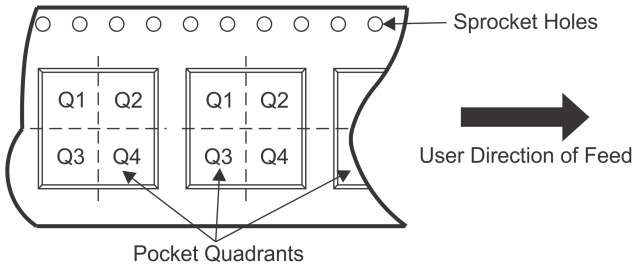


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

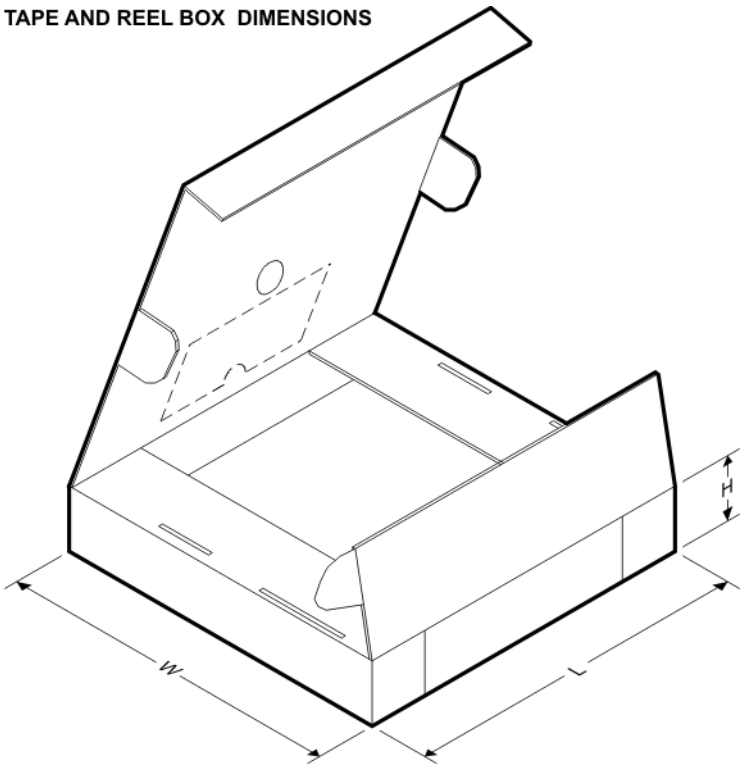
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6650HQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6650HQDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0

GENERIC PACKAGE VIEW

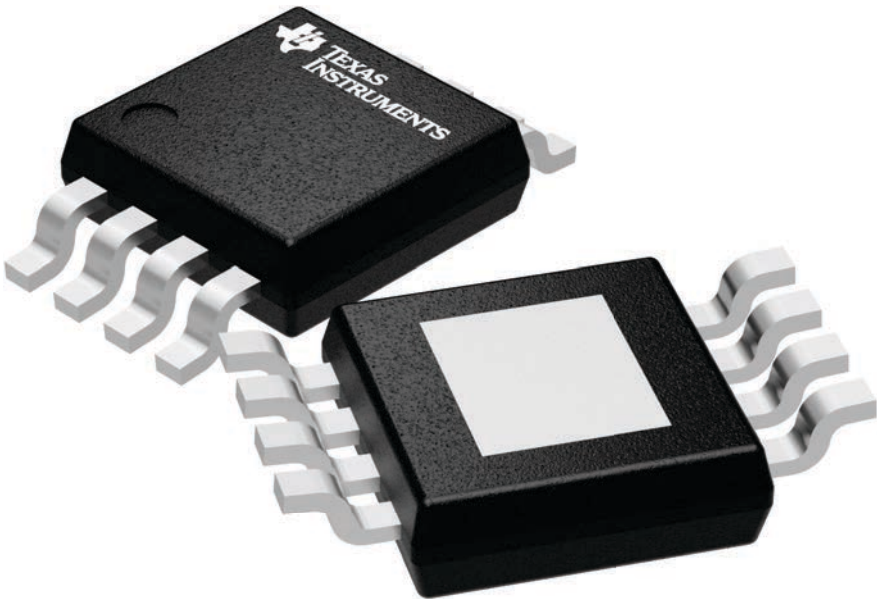
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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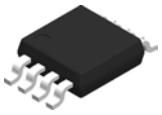
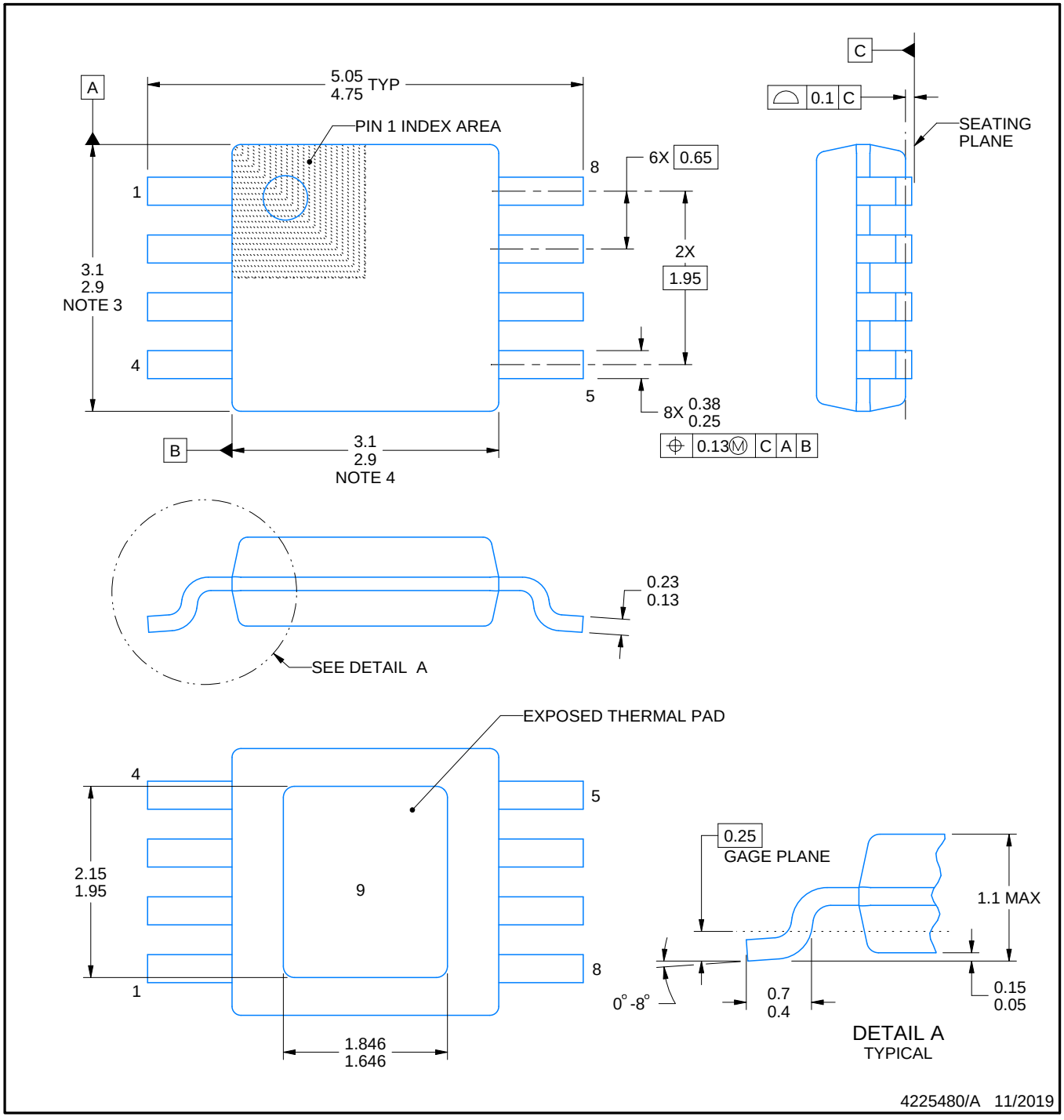
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

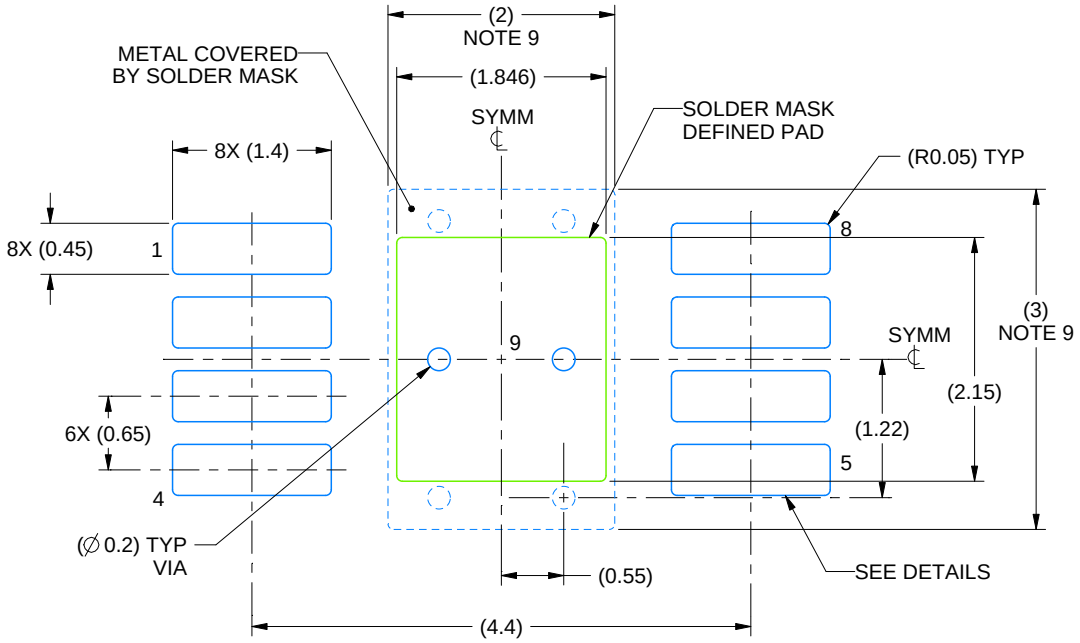
SMALL OUTLINE PACKAGE



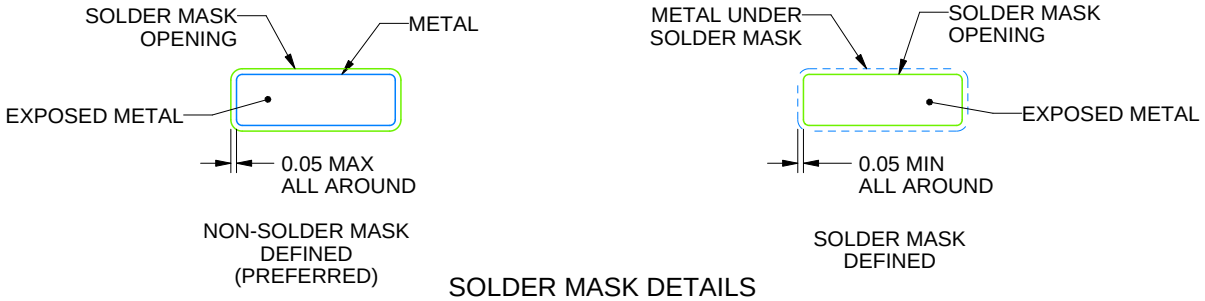
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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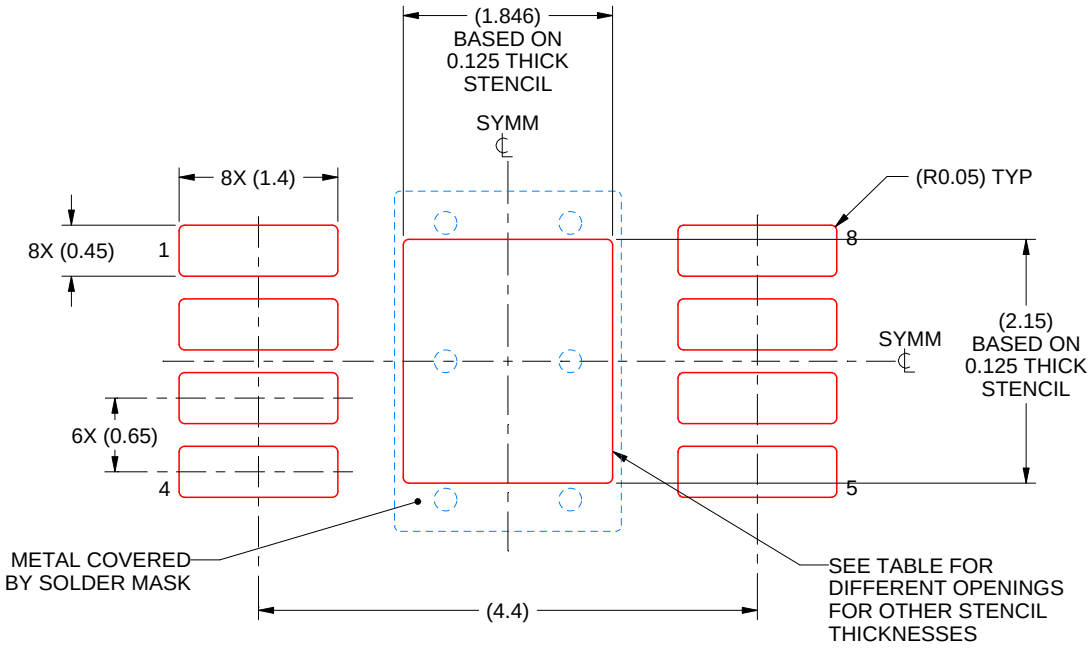
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.06 X 2.40
0.125	1.846 X 2.15 (SHOWN)
0.15	1.69 X 1.96
0.175	1.56 X 1.82

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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