

# INA333-Q1 Automotive, Zero-Drift, micro-Power Instrumentation Amplifier

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1:  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$
- **Functional Safety-Capable**
  - [Documentation available to aid functional safety system design](#)
- Low offset voltage: 25  $\mu\text{V}$  (maximum),  $G \geq 100$
- Low drift: 0.1  $\mu\text{V}/^{\circ}\text{C}$ ,  $G \geq 100$
- Low noise: 50  $\text{nV}/\sqrt{\text{Hz}}$ ,  $G \geq 100$
- High CMRR: 96 dB (minimum),  $G \geq 10$
- Low input bias current: 280 pA (maximum)
- Supply range: 1.8 V to 5.5 V
- Input voltage:  $(V-) + 0.1\text{ V}$  to  $(V+) - 0.1\text{ V}$
- Output range:  $(V-) + 0.05\text{ V}$  to  $(V+) - 0.05\text{ V}$
- Low quiescent current: 50  $\mu\text{A}$
- Operating temperature:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- RFI filtered inputs
- Package: 8-pin VSSOP

## 2 Applications

- [Powertrain torque sensor](#)
- [Powertrain pressure sensor](#)
- [Powertrain temperature sensor](#)
- [Powertrain knock sensor](#)
- [Vehicle occupant detection sensor](#)
- [Driver vital sign monitoring](#)
- Control-panel, force-sensor-based switches

## 3 Description

The INA333-Q1 is a low-power, precision instrumentation amplifier offering excellent accuracy. The three-op-amp design, small size, and low power make this device an excellent choice for automotive applications that require precise measurements, such as current leakage detection. This INA333-Q1 is also a great choice for applications that use resistive bridge sensors.

A single external resistor sets any gain from 1 to 1000. The INA333-Q1 is designed to use an industry-standard gain equation:  $G = 1 + (100\text{ k}\Omega / R_G)$ .

The INA333-Q1 provides very low offset voltage (25  $\mu\text{V}$ ,  $G \geq 100$ ), excellent offset voltage drift (0.1  $\mu\text{V}/^{\circ}\text{C}$ ,  $G \geq 100$ ), and high common-mode rejection (96 dB at  $G \geq 10$ ). The device operates with power supplies as low as 1.8 V ( $\pm 0.9\text{ V}$ ), and quiescent current is only 50  $\mu\text{A}$ . Auto-calibration techniques maintain excellent precision over the automotive temperature range. The INA333-Q1 provides a very low peak-to-peak noise of 1  $\mu\text{V}$ .

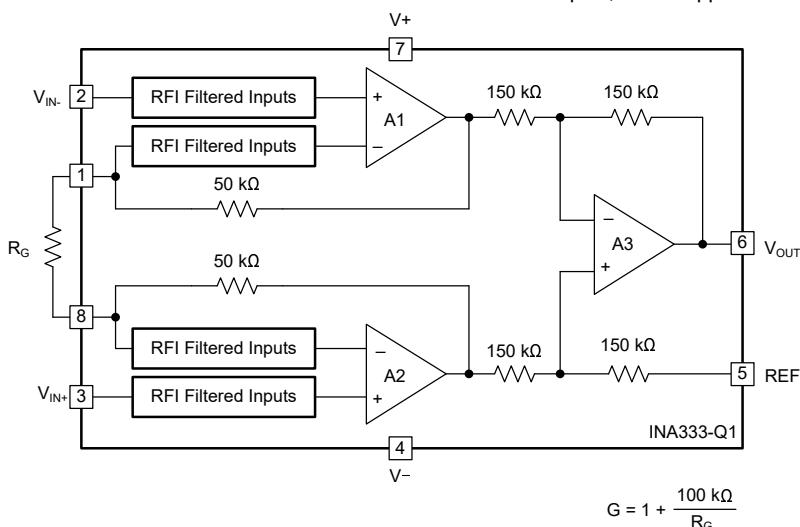
The INA333-Q1 device is available in an 8-pin VSSOP package and is specified over the  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
INA333-Q1	VSSOP (8)	3 mm × 4.9 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



**Simplified Schematic**



## Table of Contents

<b>1 Features</b> .....	1	7.4 Device Functional Modes.....	13
<b>2 Applications</b> .....	1	<b>8 Application and Implementation</b> .....	14
<b>3 Description</b> .....	1	8.1 Application Information.....	14
<b>4 Revision History</b> .....	2	8.2 Typical Application.....	15
<b>5 Pin Configuration and Functions</b> .....	3	8.3 Power Supply Recommendations.....	20
<b>6 Specifications</b> .....	4	8.4 Layout.....	20
6.1 Absolute Maximum Ratings.....	4	<b>9 Device and Documentation Support</b> .....	21
6.2 ESD Ratings.....	4	9.1 Device Support.....	21
6.3 Recommended Operating Conditions.....	4	9.2 Documentation Support.....	22
6.4 Thermal Information.....	4	9.3 Receiving Notification of Documentation Updates.....	22
6.5 Electrical Characteristics.....	5	9.4 Support Resources.....	22
6.6 Typical Characteristics.....	7	9.5 Trademarks.....	22
<b>7 Detailed Description</b> .....	13	9.6 Electrostatic Discharge Caution.....	22
7.1 Overview.....	13	9.7 Glossary.....	22
7.2 Functional Block Diagram.....	13	<b>10 Mechanical, Packaging, and Orderable Information</b> .....	22
7.3 Feature Description.....	13		

## 4 Revision History

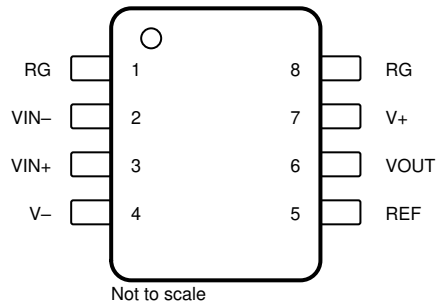
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision A (May 2020) to Revision B (June 2023)</b>	<b>Page</b>
• Added functional safety feature bullets.....	1
• Changed four resistors in front-page figure from 150 Ω to 150 kΩ.....	1
• Changed four resistors in functional block diagram from 150 Ω to 150 kΩ.....	13

---

<b>Changes from Revision * (October 2019) to Revision A (May 2020)</b>	<b>Page</b>
• Changed device from advanced information (preview) to production data (active) .....	1

## 5 Pin Configuration and Functions



**Figure 5-1. DGK Package, 8-Pin VSSOP (Top View)**

**Table 5-1. Pin Functions**

PIN		TYPE	DESCRIPTION
NAME	NO.		
REF	5	Input	Reference input. This pin must be driven by low impedance or connected to ground.
RG	1, 8	—	Gain setting pins. For gains greater than 1, place a gain resistor between pins 1 and 8.
V+	7	—	Positive supply
V-	4	—	Negative supply
VIN+	3	Input	Positive input
VIN-	2	Input	Negative input
VOUT	6	Output	Output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>S</sub>	Supply voltage	Single-supply, V <sub>S</sub> = (V <sub>+</sub> )		7	V
		Dual-supply, V <sub>S</sub> = (V <sub>+</sub> ) – (V <sub>–</sub> )		±3.5	
	Input voltage	Common-mode	(V <sub>–</sub> ) – 0.3	(V <sub>+</sub> ) + 0.3	V
		Differential		(V <sub>+</sub> ) – (V <sub>–</sub> ) + 0.2	
	Input current			±10	mA
	Output short circuit <sup>(2)</sup>		Continuous	Continuous	
T <sub>A</sub>	Operating temperature		–55	150	°C
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		–65	150	°C

- (1) Operation outside of *Absolute Maximum Ratings* may cause permanent damage to the device. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Short-circuit to ground, one amplifier per package.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 HBM ESD classification level 2 <sup>(1)</sup>	±2000	V
		Charge device model (CDM), per AEC Q100-011 CDM ESD classification level C5	±750	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>S</sub>	Supply voltage		1.8	5.5	V
T <sub>A</sub>	Operating temperature		–40	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		INA333-Q1	UNIT
		DGK (VSSOP)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	169.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	62.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	90.3	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	7.6	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	88.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

at  $V_S = 1.8\text{ V to }5.5\text{ V}$  at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = V_S / 2$ , and  $G = 1$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>INPUT<sup>(1)</sup></b>							
$V_{OSI}$	Input stage offset voltage <sup>(2)</sup>				$\pm 10$	$\pm 25$	$\mu\text{V}$
		vs temperature, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$				$\pm 0.1$	$\mu\text{V}/^\circ\text{C}$
$V_{OSO}$	Output stage offset voltage <sup>(2)</sup>				$\pm 25$	$\pm 110$	$\mu\text{V}$
		vs temperature, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$				$\pm 0.5$	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio			90	102		dB
$Z_{id}$	Differential impedance			100    3			$\text{G}\Omega \parallel \text{pF}$
$Z_{ic}$	Common-mode impedance			100    3			$\text{G}\Omega \parallel \text{pF}$
$V_{CM}$	Common-mode voltage	$V_O = 0\text{ V}$		$(V-) + 0.1$		$(V+) - 0.1$	V
CMRR	Common-mode rejection ratio	DC to 60 Hz, $V_S = 5.5\text{ V}$ , $V_{CM} = (V-) + 0.1\text{ V to } (V+) - 0.1\text{ V}$	$G = 1$	78	90		dB
			$G = 10$	96	110		
			$G = 100$	96	115		
			$G = 1000$	96	115		
<b>INPUT BIAS CURRENT</b>							
$I_B$	Input bias current				$\pm 70$	$\pm 280$	$\mu\text{A}$
		$T_A = -40^\circ\text{C to }+125^\circ\text{C}$			See <a href="#">Figure 6-26</a>		$\mu\text{A}/^\circ\text{C}$
$I_{OS}$	Input offset current				$\pm 50$	$\pm 280$	$\mu\text{A}$
		$T_A = -40^\circ\text{C to }+125^\circ\text{C}$			See <a href="#">Figure 6-28</a>		$\mu\text{A}/^\circ\text{C}$
<b>INPUT VOLTAGE NOISE</b>							
$e_{NI}$	Input voltage noise	$G = 100$ , $R_S = 0\ \Omega$	$f = 10\text{ Hz}$	50			$\text{nV}/\sqrt{\text{Hz}}$
			$f = 100\text{ Hz}$	50			
			$f = 1\text{ kHz}$	50			
			$f = 0.1\text{ Hz to }10\text{ Hz}$	1		$\mu\text{V}_{PP}$	
$I_n$	Input current noise	$f = 10\text{ Hz}$		100		$\text{fA}/\sqrt{\text{Hz}}$	
		$f = 0.1\text{ Hz to }10\text{ Hz}$		2		$\text{pA}_{PP}$	
<b>GAIN</b>							
	Gain equation			$1 + (100\text{ k}\Omega / R_G)$			V/V
G	Gain			1		1000	V/V
GE	Gain error	$V_S = 5.5\text{ V}$ , $(V-) + 100\text{ mV} \leq V_O \leq (V+) - 100\text{ mV}$	$G = 1$	$\pm 0.01$	$\pm 0.1$		%
			$G = 10$	$\pm 0.05$	$\pm 0.25$		
			$G = 100$	$\pm 0.07$	$\pm 0.25$		
			$G = 1000$	$\pm 0.25$	$\pm 0.5$		
	Gain vs temperature	$T_A = -40^\circ\text{C to }+125^\circ\text{C}$		$\pm 1$	$\pm 5$		$\text{ppm}/^\circ\text{C}$
		$G > 1$ <sup>(3)</sup>		$\pm 15$	$\pm 50$		
	Gain nonlinearity	$G = 1\text{ to }1000$ $V_S = 5.5\text{ V}$ , $(V-) + 100\text{ mV} \leq V_O \leq (V+) - 100\text{ mV}$		10			ppm
<b>OUTPUT</b>							
	Output voltage swing from rail	$V_S = 5.5\text{ V}$		40	50		mV
	Capacitive load drive			500			pF
$I_{SC}$	Short-circuit current	Continuous to common		-40, +5			mA

### 6.5 Electrical Characteristics (continued)

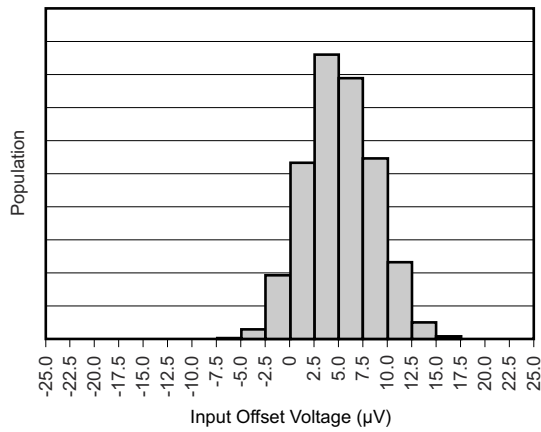
at  $V_S = 1.8\text{ V to }5.5\text{ V}$  at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = V_S / 2$ , and  $G = 1$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>FREQUENCY RESPONSE</b>							
BW	Bandwidth, -3 dB	G = 1			150		kHz
		G = 10			35		
		G = 100			3.5		
		G = 1000			350		Hz
SR	Slew rate	$V_S = 5\text{ V}$ , $V_O = 4\text{-V step}$	G = 1		0.16		V/ $\mu\text{s}$
			G = 100		0.05		
$t_s$	Settling time to 0.01%	$V_{STEP} = 4\text{ V}$	G = 1		50		$\mu\text{s}$
			G = 100		400		
	Settling time to 0.001%	$V_{STEP} = 4\text{ V}$	G = 1		60		
			G = 100		500		
	Overload recovery	50% overdrive			75		$\mu\text{s}$
<b>REFERENCE INPUT</b>							
$R_{IN}$	Input impedance				300		k $\Omega$
	Voltage range			V-		V+	V
<b>POWER SUPPLY</b>							
$I_Q$	Quiescent current	$V_{IN} = V_S / 2$			50	75	$\mu\text{A}$
		$T_A = -40^\circ\text{C to }+125^\circ\text{C}$				80	

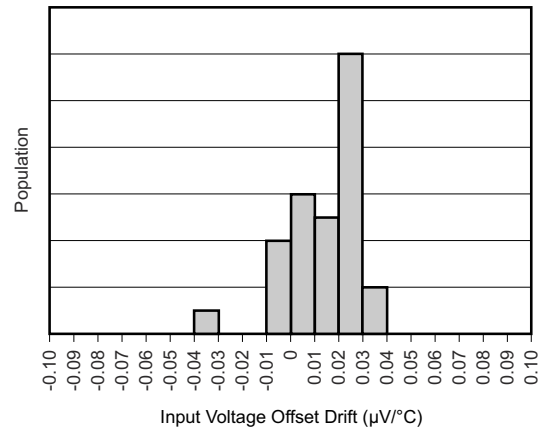
- (1) Total  $V_{OS}$ , referred-to-input =  $(V_{OSI}) + (V_{OSO} / G)$ .
- (2) RTI = Referred-to-input.
- (3) Does not include effects of external resistor  $R_G$ .

## 6.6 Typical Characteristics

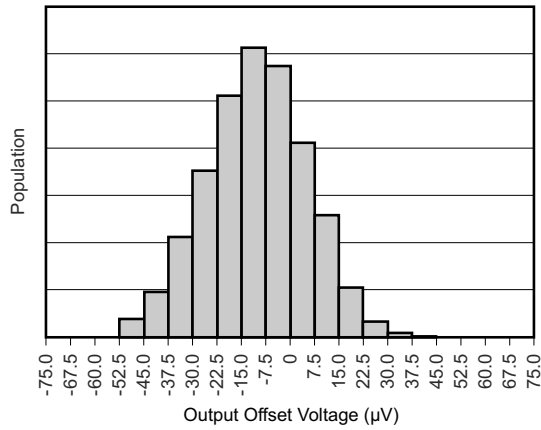
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = \text{midsupply}$ , and  $G = 1$  (unless otherwise noted)



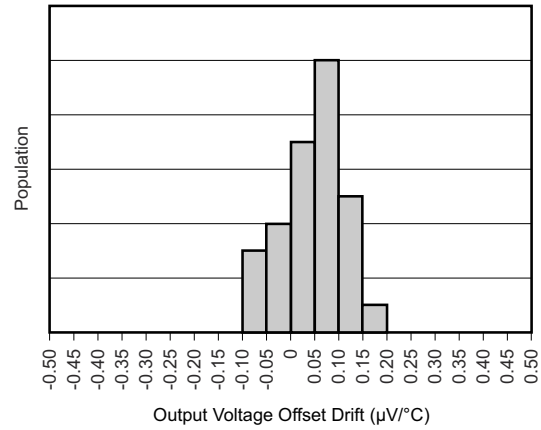
**Figure 6-1. Input Offset Voltage**



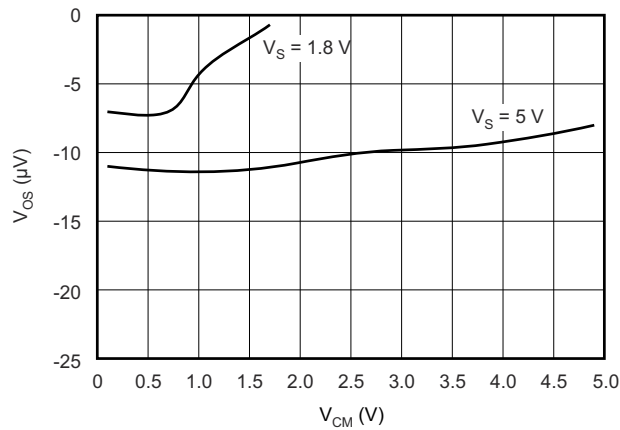
**Figure 6-2. Input Voltage Offset Drift ( $-40^\circ\text{C}$  to  $125^\circ\text{C}$ )**



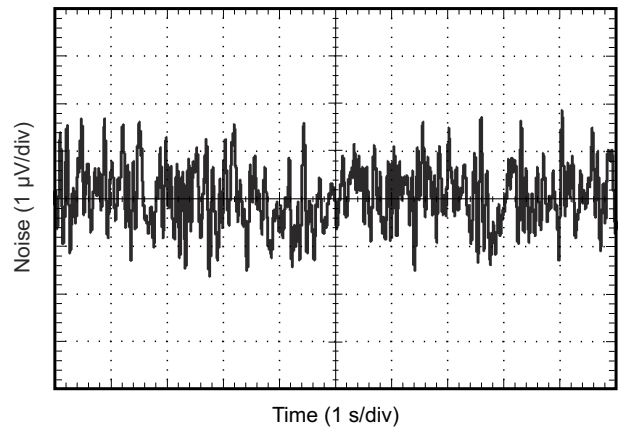
**Figure 6-3. Output Offset Voltage**



**Figure 6-4. Output Voltage Offset Drift ( $-40^\circ\text{C}$  to  $125^\circ\text{C}$ )**



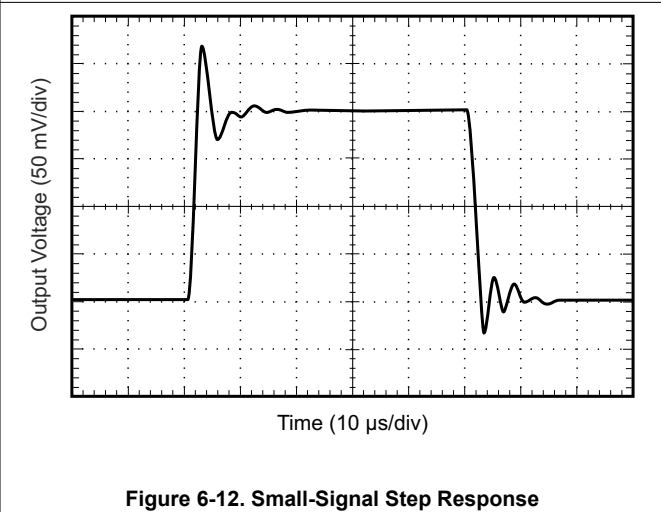
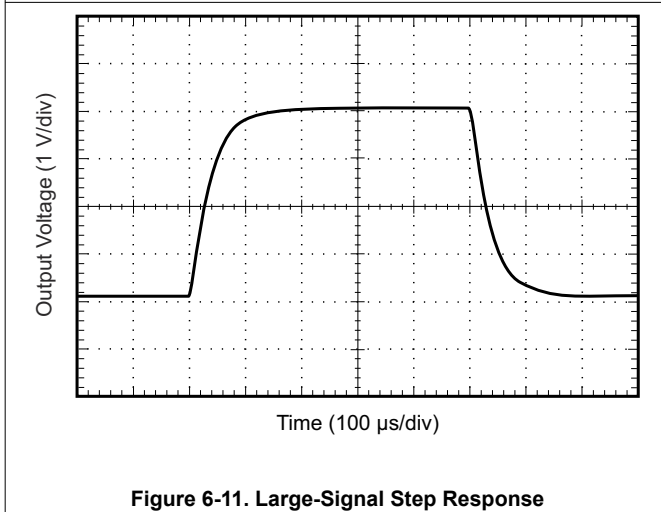
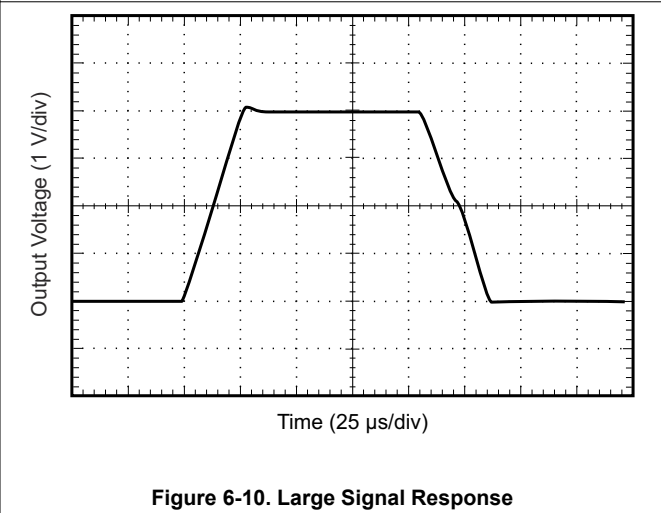
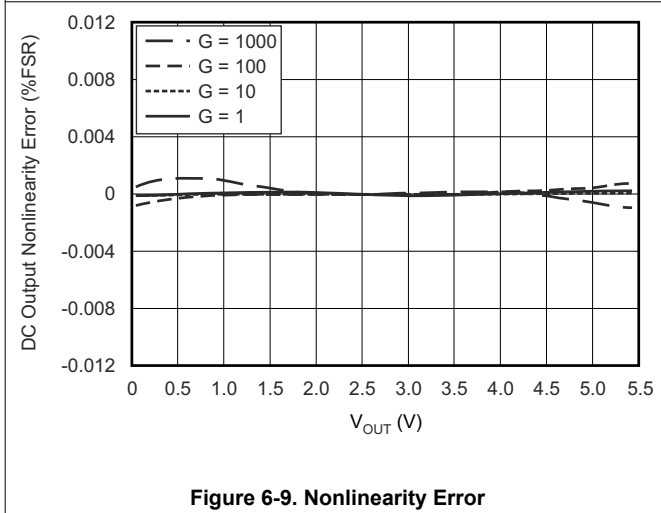
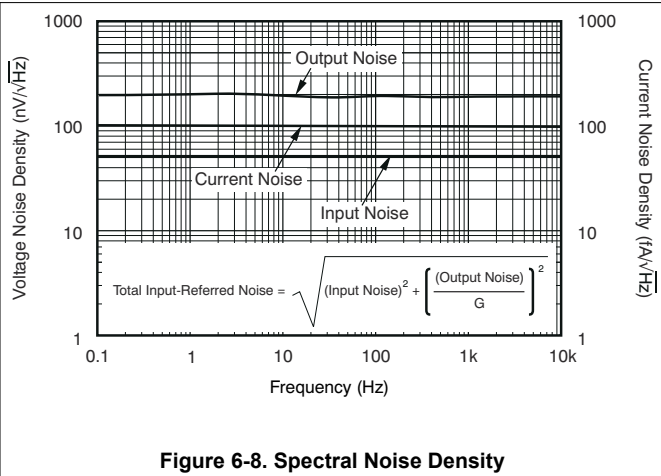
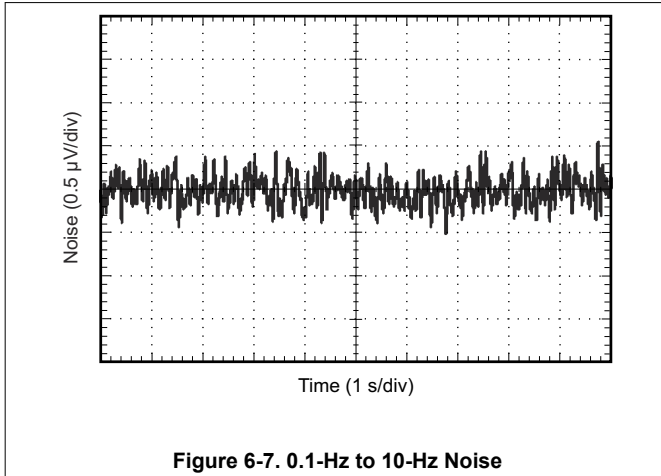
**Figure 6-5. Offset Voltage vs Common-Mode Voltage**



**Figure 6-6. 0.1-Hz to 10-Hz Noise**

## 6.6 Typical Characteristics (continued)

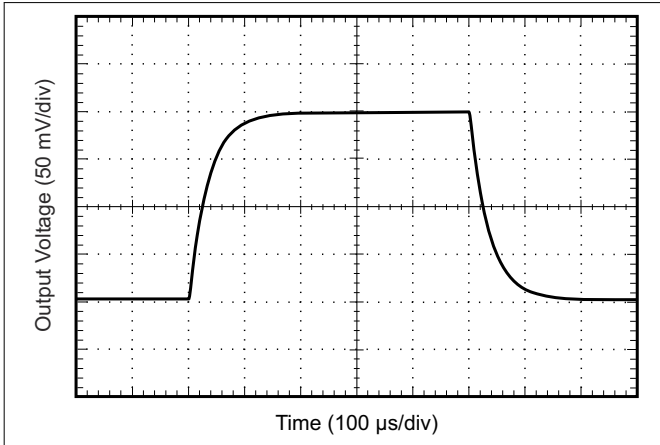
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = \text{midsupply}$ , and  $G = 1$  (unless otherwise noted)



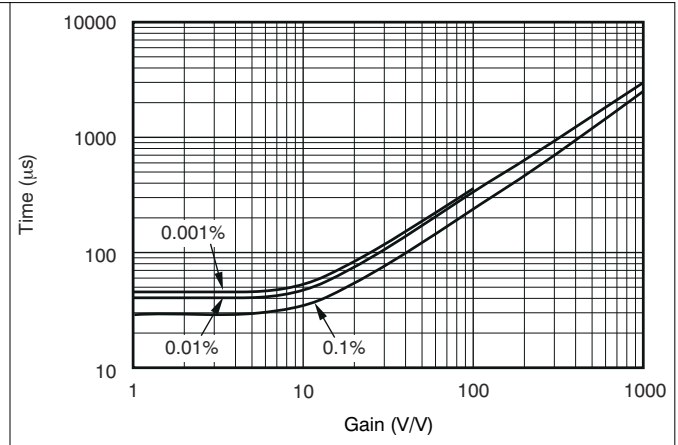


## 6.6 Typical Characteristics (continued)

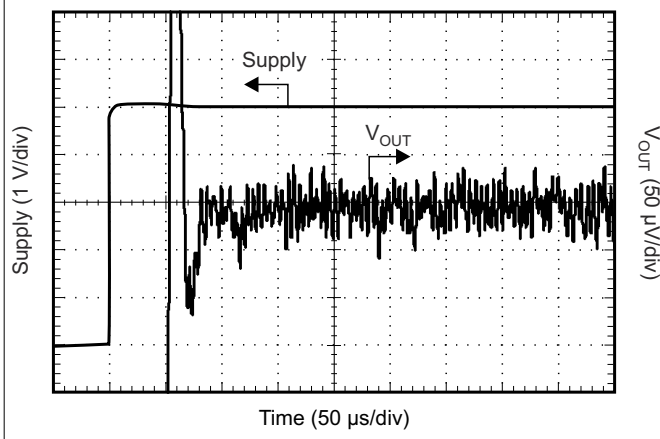
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = \text{midsupply}$ , and  $G = 1$  (unless otherwise noted)



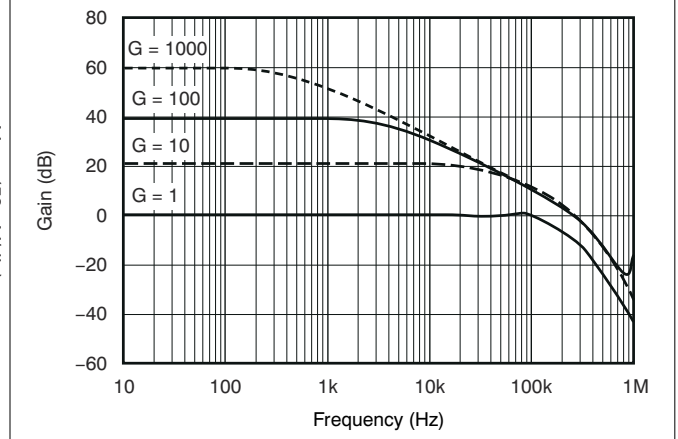
**Figure 6-13. Small-Signal Step Response**



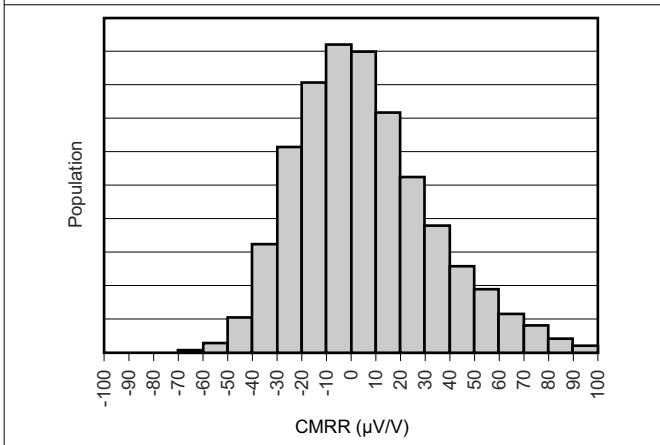
**Figure 6-14. Settling Time vs Gain**



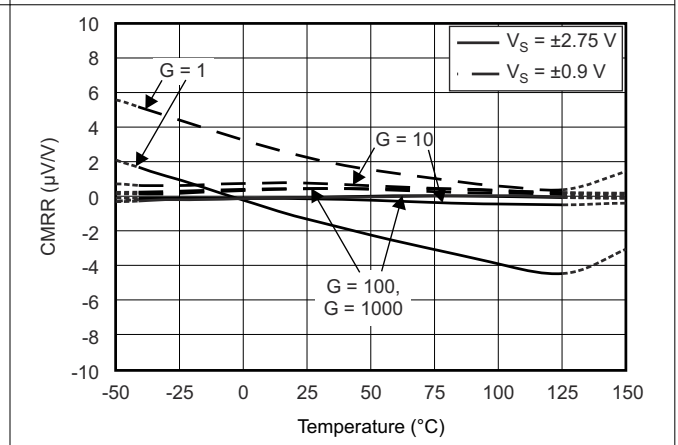
**Figure 6-15. Start-Up Settling Time**



**Figure 6-16. Gain vs Frequency**



**Figure 6-17. Common-Mode Rejection Ratio**



**Figure 6-18. Common-Mode Rejection Ratio vs Temperature**

## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = \text{midsupply}$ , and  $G = 1$  (unless otherwise noted)

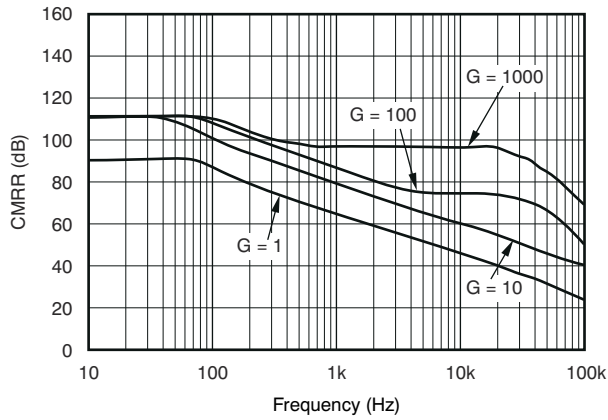


Figure 6-19. Common-Mode Rejection Ratio vs Frequency

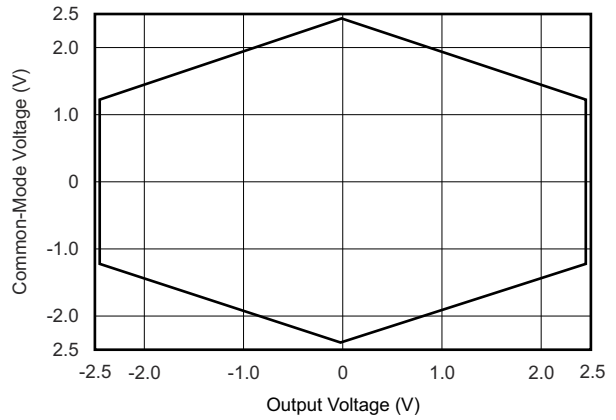


Figure 6-20. Typical Common-Mode Range vs Output Voltage

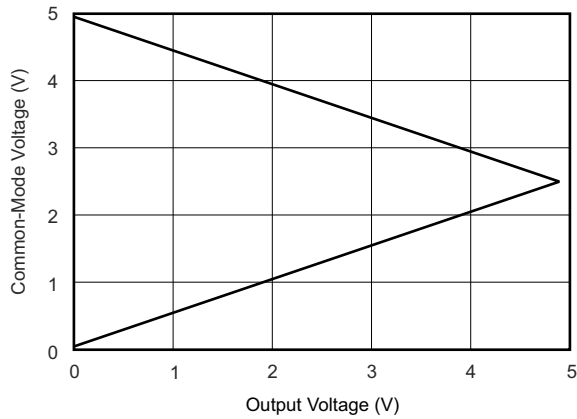


Figure 6-21. Typical Common-Mode Range vs Output Voltage

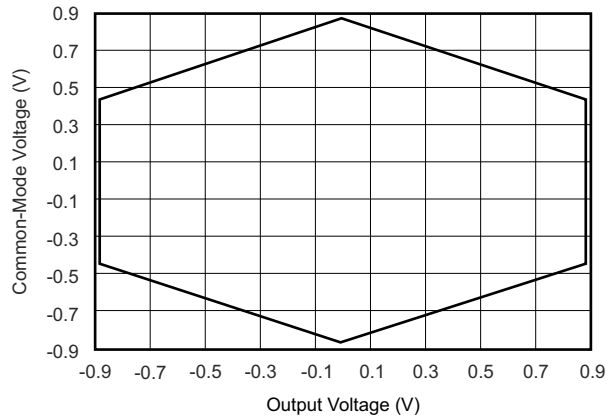


Figure 6-22. Typical Common-Mode Range vs Output Voltage

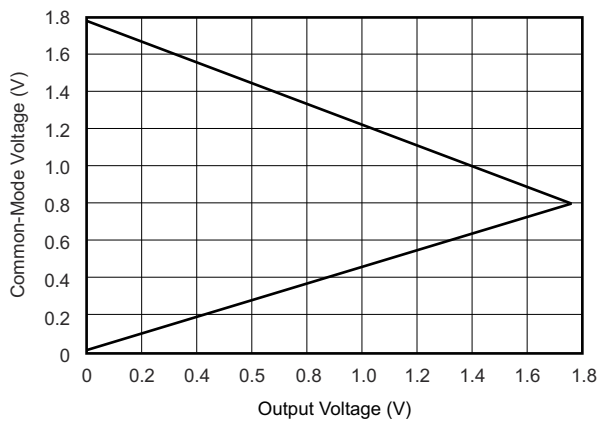


Figure 6-23. Typical Common-Mode Range vs Output Voltage

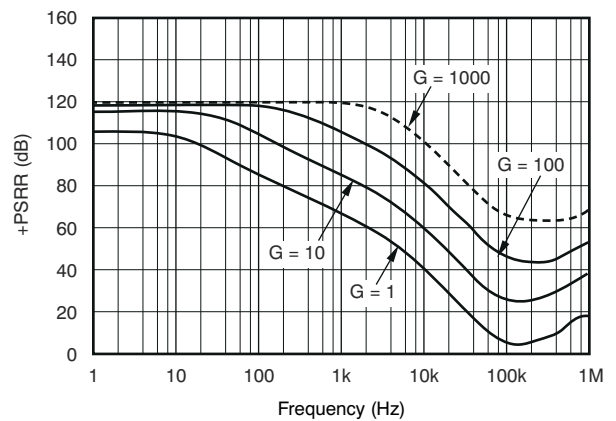
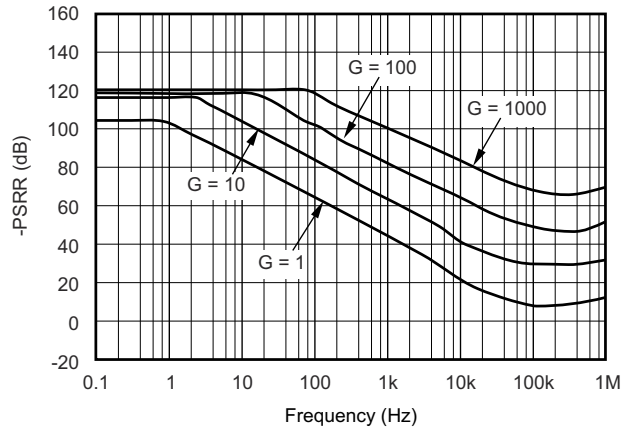


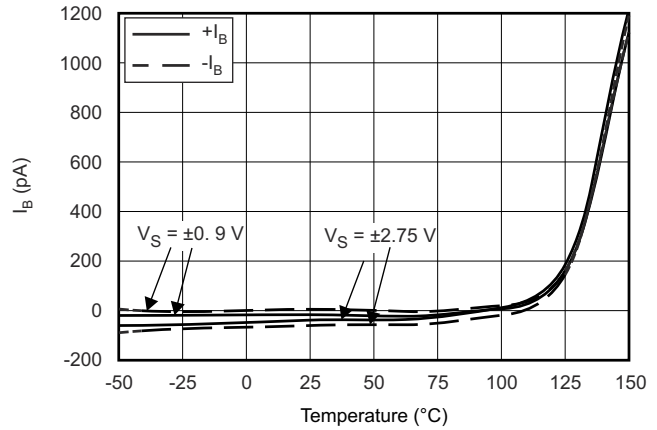
Figure 6-24. Positive Power-Supply Rejection Ratio

## 6.6 Typical Characteristics (continued)

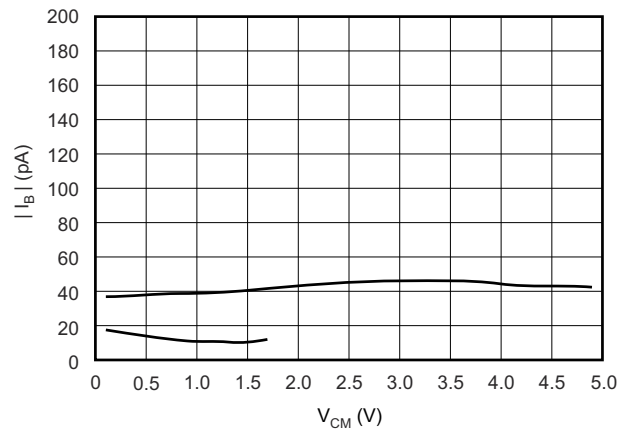
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = \text{midsupply}$ , and  $G = 1$  (unless otherwise noted)



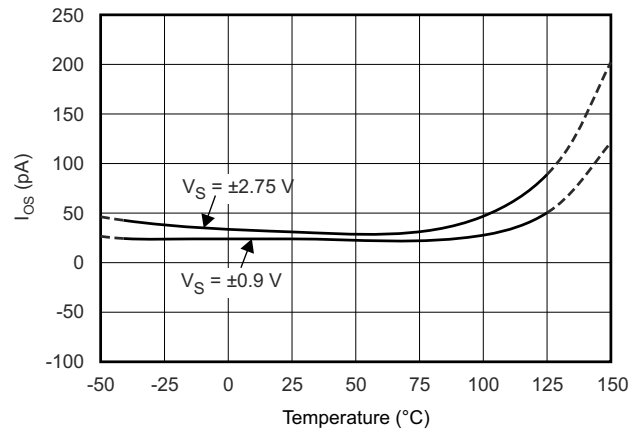
**Figure 6-25. Negative Power-Supply Rejection Ratio**



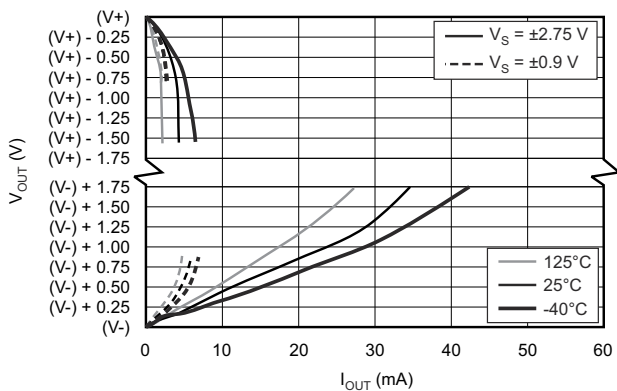
**Figure 6-26. Input Bias Current vs Temperature**



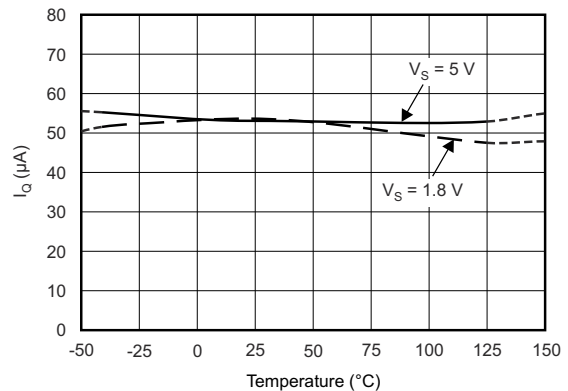
**Figure 6-27. Input Bias Current vs Common-Mode Voltage**



**Figure 6-28. Input Offset Current vs Temperature**



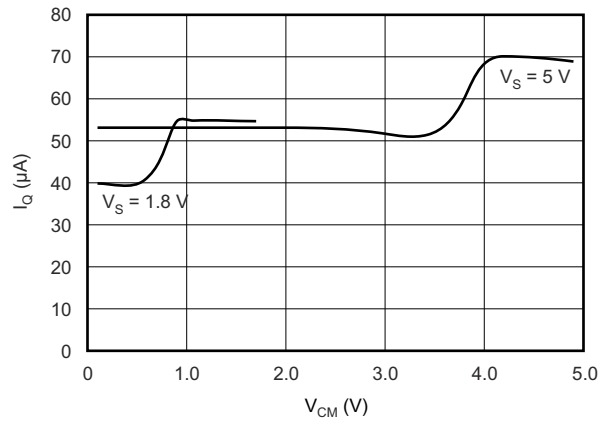
**Figure 6-29. Output Voltage Swing vs Output Current**



**Figure 6-30. Quiescent Current vs Temperature**

### 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = \text{midsupply}$ , and  $G = 1$  (unless otherwise noted)



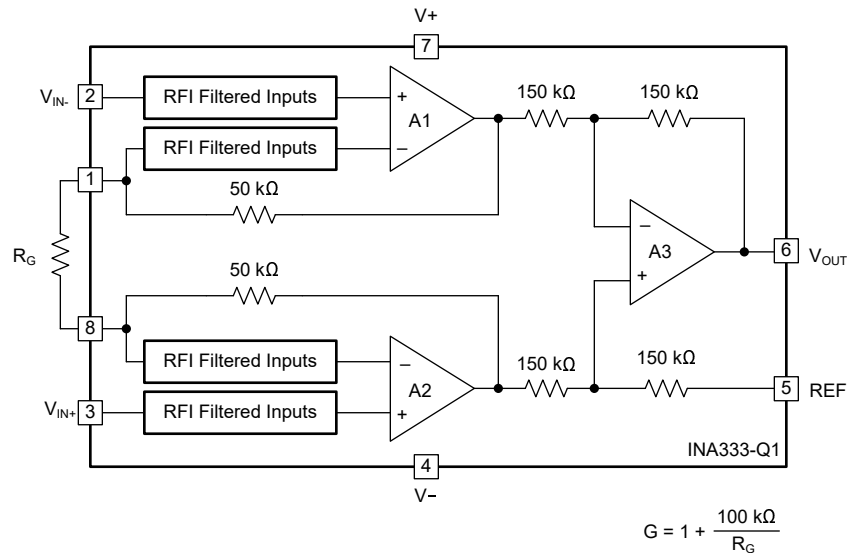
**Figure 6-31. Quiescent Current vs Common-Mode Voltage**

## 7 Detailed Description

### 7.1 Overview

The INA333-Q1 is a monolithic instrumentation amplifier (INA) based on the precision zero-drift INA333-Q1 (operational amplifier) core. The INA333-Q1 also integrates laser-trimmed resistors to maintain excellent common-mode rejection and low gain error. The combination of the zero-drift amplifier core and the precision resistors allows this device to achieve outstanding dc precision, and makes the INA333-Q1 an excellent choice for many 3.3-V and 5-V automotive applications.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Internal Offset Correction

The INA333-Q1 internal operational amplifiers use an autocalibration technique with a time-continuous, 350-kHz operational amplifier in the signal path. The amplifier is zero-corrected every 8  $\mu\text{s}$  using a proprietary technique. At power up, the amplifier requires approximately 100  $\mu\text{s}$  to achieve the specified  $V_{OS}$  accuracy. This design has no aliasing or flicker noise.

#### 7.3.2 Input Protection

The input pins of the INA333-Q1 are protected with internal diodes connected to the power-supply rails. These diodes clamp and prevent the applied signal from damaging the input circuitry. If the input signal voltage exceeds the power supplies by greater than 0.3 V, limit the input signal current to less than 10 mA to protect the internal clamp diodes. This current limiting is generally done with a series input resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

### 7.4 Device Functional Modes

The INA333-Q1 has a single functional mode, and is operational when the power-supply voltage is greater than 1.8 V. The recommended maximum specified power-supply voltage for the INA333-Q1 is 5.5 V.

## 8 Application and Implementation

---

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

---

### 8.1 Application Information

The INA333-Q1 measures small differential voltages with high common-mode voltage developed between the noninverting and inverting input. The high input impedance makes the INA333-Q1 a great choice for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

#### 8.1.1 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA333-Q1 is from approximately 0.1 V below the positive supply voltage to 0.1 V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A1 and A2. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage; see [Figure 6-20](#) to [Figure 6-23](#) in [Section 6.6](#).

Input overload conditions can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the respective positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA333-Q1 is near 0 V even though both inputs are overloaded.

## 8.2 Typical Application

Figure 8-1 shows the basic connections required for operation of the INA333-Q1. Good layout practice mandates the use of bypass capacitors placed close to the device pins as shown.

The output of the INA333-Q1 is referred to the output reference (REF) pin, which is normally grounded. This connection must be low-impedance to maintain good common-mode rejection. Although 15 Ω or less of stray resistance can be tolerated while maintaining specified CMRR, small stray resistances of tens of ohms in series with the REF pin can cause noticeable degradation in CMRR.

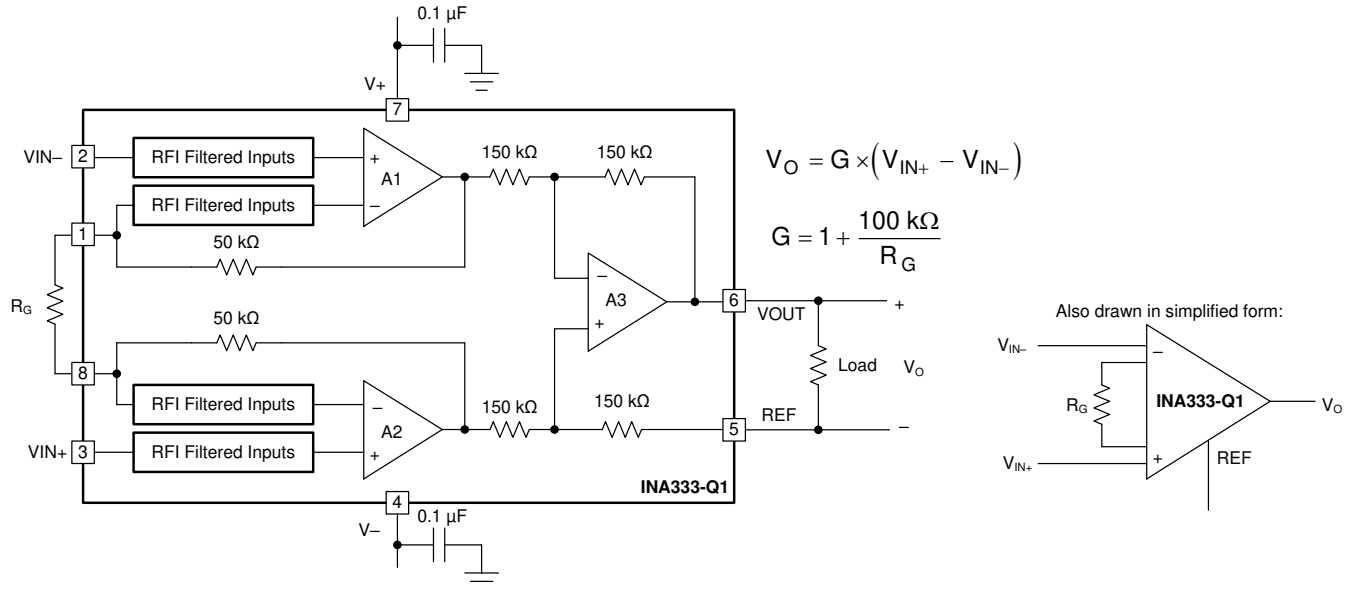


Figure 8-1. Basic Connections

### 8.2.1 Design Requirements

The device can be configured to monitor the input differential voltage when the gain of the input signal is set by external resistor  $R_G$ . The output signal references to the REF pin. The most common application is where the output is referenced to ground when no input signal is present by connecting the REF pin to ground. When the input signal increases, the output voltage at the OUT pin also increases.

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Setting the Gain

The gain of the INA333-Q1 is set by a single external resistor,  $R_G$ , connected between pins 1 and 8. The value of  $R_G$  is selected according to Equation 1:

$$G = 1 + (100 \text{ k}\Omega / R_G) \quad (1)$$

Table 8-1 lists several commonly-used gains and resistor values. The 100 kΩ in Equation 1 comes from the sum of the two internal feedback resistors of  $A_1$  and  $A_2$ . These on-chip resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA333-Q1.

The stability and temperature drift of the external gain setting resistor,  $R_G$ , also affects gain. The contribution of  $R_G$  to gain accuracy and drift can be directly inferred from Equation 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater. To maintain stability, avoid parasitic capacitance greater than a few picofarads at the  $R_G$  connections. Careful matching of any parasitics on both  $R_G$  pins maintains optimal CMRR over frequency.

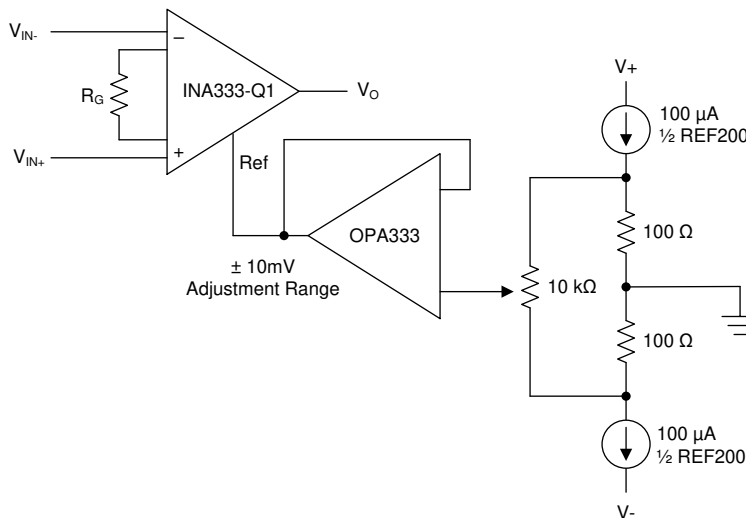
**Table 8-1. Commonly Used Gains and Resistor Values**

DESIRED GAIN	$R_G$ ( $\Omega$ )	NEAREST 1% $R_G$ ( $\Omega$ )
1	NC <sup>(1)</sup>	NC
2	100k	100k
5	25k	24.9k
10	11.1k	11k
20	5.26k	5.23k
50	2.04k	2.05
100	1.01k	1k
200	502.5	499
500	200.4	200
1000	100.1	100

(1) NC denotes no connection. When using the SPICE model, the simulation does not converge unless a resistor is connected to the  $R_G$  pins; use a very large resistor value.

### 8.2.2.2 Offset Trimming

Most applications require no external offset adjustment. However, if necessary, adjustments can be made by applying a voltage to the REF pin. Figure 8-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to REF pin is summed at the output. The operational amplifier buffer provides low impedance at the REF pin to preserve good common-mode rejection.



**Figure 8-2. Optional Trimming of Output Offset Voltage**



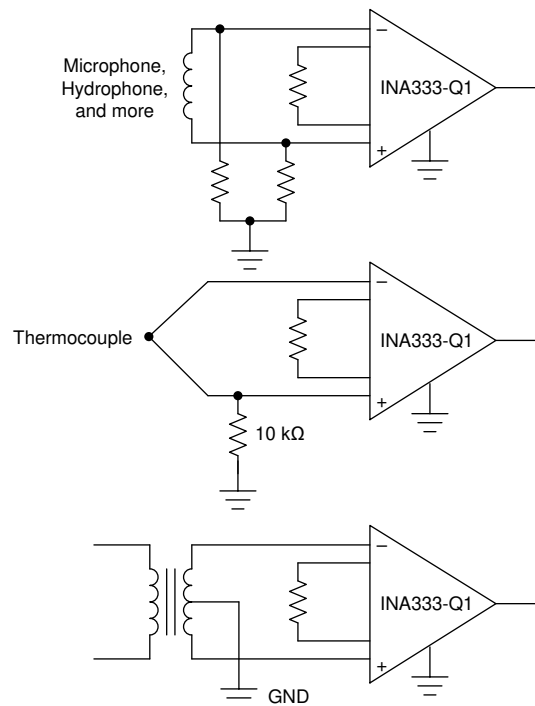
### 8.2.2.3 Noise Performance

The autocalibration technique used by the INA333-Q1 results in reduced low frequency noise, typically only  $50 \text{ nV}/\sqrt{\text{Hz}}$  ( $G = 100$ ). The spectral noise density is shown in detail in [Figure 6-8](#). The low-frequency noise of the device is approximately  $1 \mu\text{V}_{\text{PP}}$  measured from 0.1 Hz to 10 Hz ( $G = 100$ ).

### 8.2.2.4 Input Bias Current Return Path

The input impedance of the INA333-Q1 is extremely high; approximately  $100 \text{ G}\Omega$ . However, a path must be provided for the input bias current of both inputs. This input bias current is typically  $\pm 70 \text{ pA}$ . High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. [Figure 8-3](#) shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the device, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in [Figure 8-3](#)). With higher source impedance, use two equal resistors to provide a balanced input with the possible advantages of a lower input offset voltage as a result of bias current, and improved high-frequency common-mode rejection.



**Figure 8-3. Providing an Input Common-Mode Current Path**

### 8.2.2.5 Low Voltage Operation

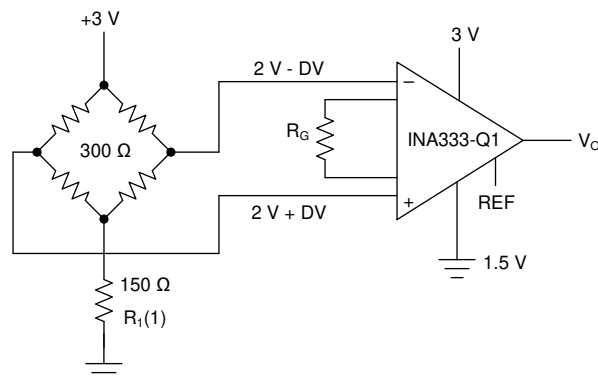
The INA333-Q1 can be operated on power supplies as low as  $\pm 0.9$  V. Most parameters vary only slightly throughout this supply voltage range; see [Section 6.6](#). Operation at a very-low supply voltage requires careful attention to make sure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. [Figure 6-20](#) to [Figure 6-23](#) show the range of linear operation for various supply voltages and gains.

### 8.2.2.6 Single-Supply Operation

The INA333-Q1 can be used on single power supplies of 1.8 V to 5.5 V. [Figure 8-4](#) shows a basic single-supply circuit. The output REF pin is connected to midsupply. Zero differential input voltage demands an output voltage of midsupply. Actual output voltage swing is limited to approximately 50 mV more than ground, when the load is referred to ground as shown. [Figure 6-29](#) shows how the output voltage swing varies with output current.

With single-supply operation,  $V_{IN+}$  and  $V_{IN-}$  must both be 0.1 V greater than ground for linear operation. For instance, the inverting input cannot be connected to ground to measure a voltage connected to the noninverting input.

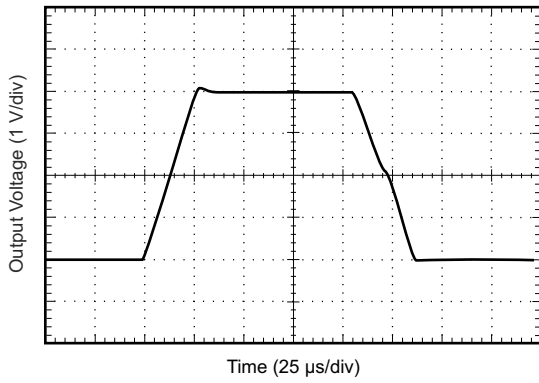
To show the issues affecting low-voltage operation, consider the circuit in [Figure 8-4](#) that shows the device operating from a single 3-V supply. A resistor in series with the low side of the bridge makes sure that the bridge output voltage is within the common-mode range of the amplifier inputs.



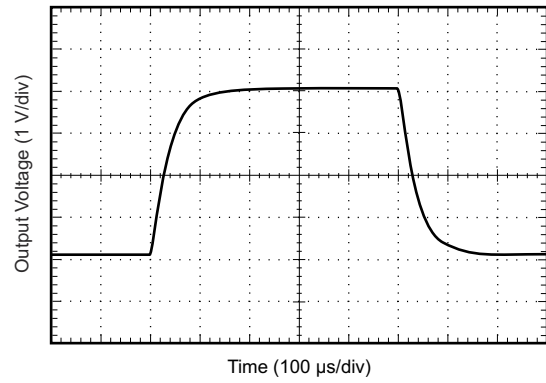
(1)  $R_1$  creates proper common-mode voltage, only for low-voltage operation; see [Section 8.2.2.6](#).

**Figure 8-4. Single-Supply Bridge Amplifier**

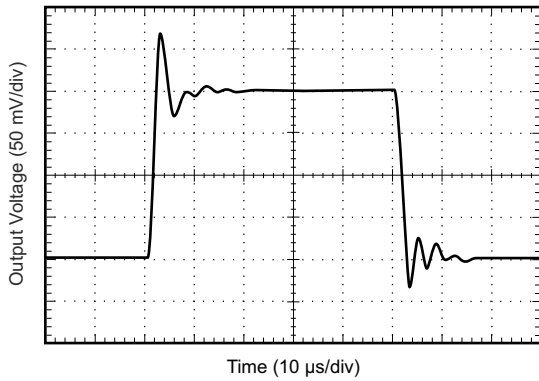
### 8.2.3 Application Curves



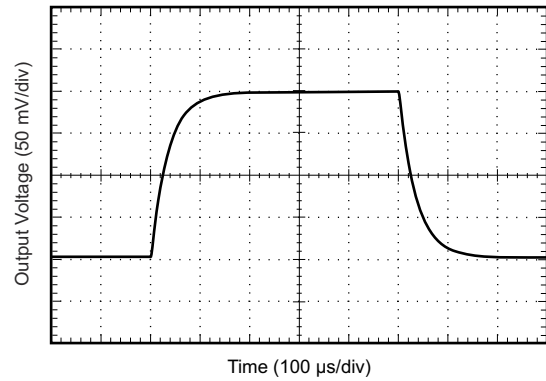
**Figure 8-5. Large Signal Response**



**Figure 8-6. Large-Signal Step Response**



**Figure 8-7. Small-Signal Step Response**



**Figure 8-8. Small-Signal Step Response**

### 8.3 Power Supply Recommendations

The minimum power supply voltage for the INA333-Q1 is 1.8 V, and the maximum power supply voltage is 5.5 V; for specified performance, 3.3 V to 5 V is recommended. Add a bypass capacitor at the input to compensate for the layout and power supply source impedance.

### 8.4 Layout

#### 8.4.1 Layout Guidelines

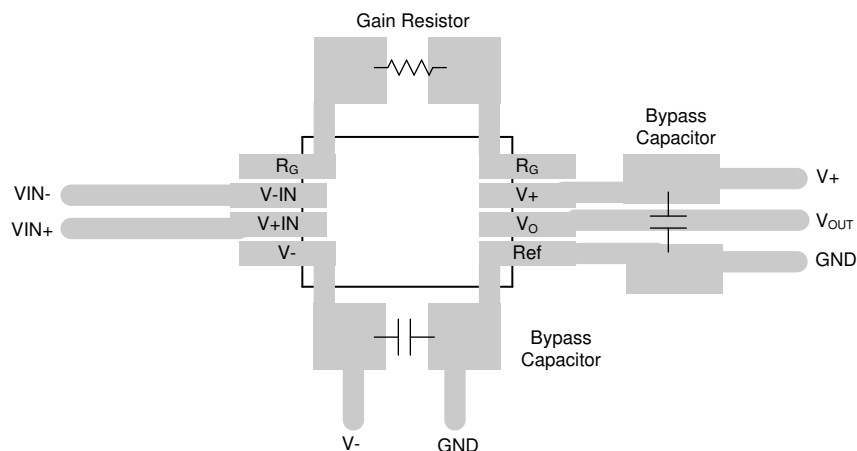
Attention to good layout practices is always recommended.

- Keep traces short.
- When possible, use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible.
- Place a 0.1- $\mu$ F bypass capacitor closely across the supply pins.

Apply these guidelines throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

Instrumentation amplifiers vary in susceptibility to radio-frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The INA333-Q1 has been specifically designed to minimize susceptibility to RFI by incorporating passive RC filters with an 8-MHz corner frequency at the  $V_{IN+}$  and  $V_{IN-}$  inputs. As a result, the INA333-Q1 demonstrates remarkably low sensitivity compared to previous-generation devices. Strong RF fields can continue to cause varying offset levels, however, and can require additional shielding.

#### 8.4.2 Layout Example



**Figure 8-9. Layout Example**

## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 Development Support

##### 9.1.1.1 TINA-TI Simulation Software (Free Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE as well as additional design capabilities.

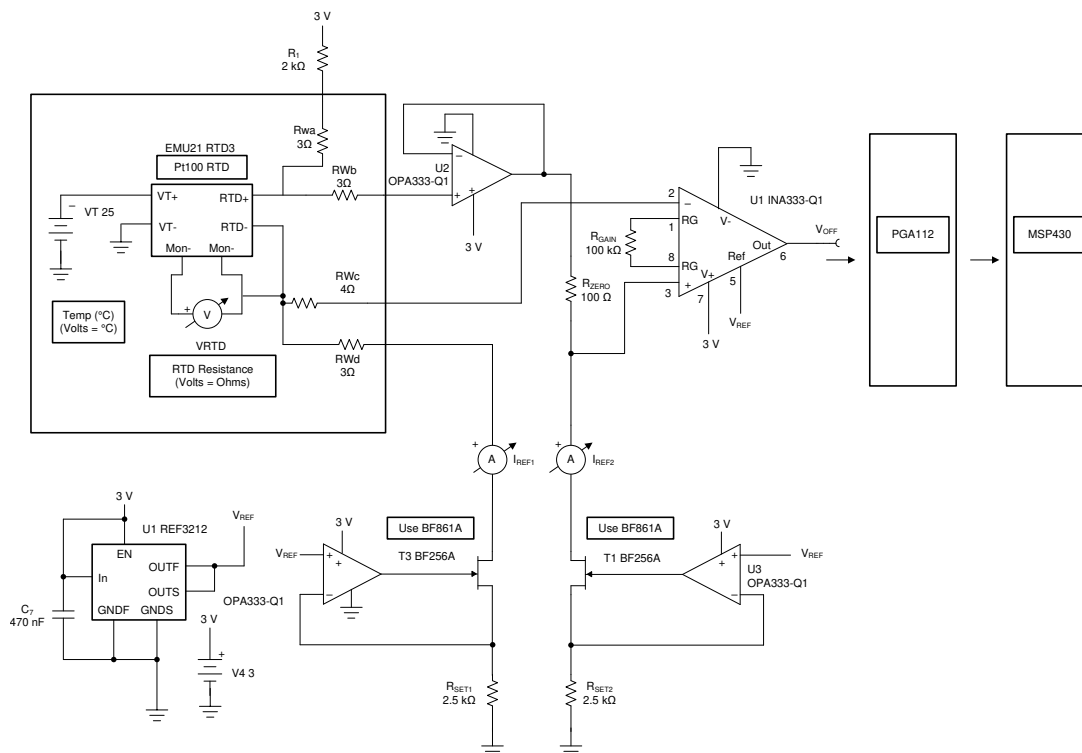
Available as a [free download](#) from the [Design tools and simulation](#) web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Virtual instruments offer users the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Figure 9-1 shows example TINA-TI circuits for the device that can be used to develop, modify, and assess the circuit design for specific applications. Links to download these simulation files are given below.

#### Note

These files require that either the TINA software (from DesignSoft) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.



NOTE: Rwa, Rwb, Rwc, and Rwd simulate wire resistance. These resistors are included to show the four-wire sense technique immunity to line mismatches. This method assumes the use of a four-wire RTD.

**Figure 9-1. Four-Wire, 3-V Conditioner for a PT100 RTD With Programmable Gain Acquisition System**

Download the TINA-TI simulation file for this circuit with the following link: [PT100 RTD](#).

## 9.2 Documentation Support

### 9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [OPA188-Q1 Precision, Low-Noise, Rail-to-Rail Output, 36-V, Zero-Drift, Automotive-Grade Operational Amplifier data sheet](#)
- Texas Instruments, [OPA333-Q1 1.8-V microPower CMOS Operational Amplifier Zero-Drift Series data sheet](#)
- Texas Instruments, [Circuit board layout techniques](#)

### 9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.4 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.5 Trademarks

TINA™ is a trademark of DesignSoft, Inc.

TINA-TI™ and TI E2E™ are trademarks of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA333QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	333Q	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF INA333-Q1 :**

- Catalog : [INA333](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA333QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA333QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated