LAN9420/LAN9420i

Single-Chip Ethernet Controller with HP Auto-MDIX Support and PCI Interface

PRODUCT FEATURES

Data Brief

Highlights

- Optimized for embedded applications with 32-bit RISC CPUs
- Integrated descriptor based scatter-gather DMA and IRQ deassertion timer effectively increase network throughput and reduce CPU loading
- Integrated Ethernet MAC with full-duplex support
- Integrated 10/100 Ethernet PHY with HP Auto-MDIX Support
- 32-bit, 33MHz, PCI 3.0 compliant interface
- Reduced power operating modes with PCI Power Management Specification 1.1 compliance
- Supports multiple audio & video streams over Ethernet

Target Applications

- Cable, satellite, and IP set-top boxes
- Digital televisions
- Digital video recorders
- Home gateways
- Digital media clients/servers
- Industrial automation systems
- Industrial/single board PC
- Kiosk/POS enterprise equipment

Key Benefits

- Integrated High-Performance 10/100 Ethernet Controller
  - — Fully compliant with IEEE802.3/802.3u
  - — Integrated Ethernet MAC and PHY
  - — 10BASE-T and 100BASE-TX support
  - — Full- and half-duplex support
  - — Full-duplex flow control
  - — Preamble generation and removal
  - — Automatic 32-bit CRC generation and checking
  - — Automatic payload padding and pad removal
  - — Loop-back modes
  - — Flexible address filtering modes
    - – One 48-bit perfect address
    - – 64 hash-filtered multicast addresses
    - – Pass all multicast
    - – Promiscuous mode
    - – Inverse filtering
    - – Pass all incoming with status report
  - — Wakeup packet support
  - — Integrated 10/100 Ethernet PHY
    - – Auto-negotiation
    - – Automatic polarity detection and correction
    - – Supports HP Auto-MDIX
    - – Supports energy-detect power down
  - — Support for 3 status LEDs
  - — Receive and transmit TCP checksum offload
- PCI Interface
  - — PCI Local Bus Specification Revision 3.0 compliant
  - — 32-bit/33-MHz PCI bus
  - — Descriptor based scatter-gather DMA enables zero-copy drivers
- Comprehensive Power Management Features
  - — Supports PCI Bus Power Management Interface Specification, Revision 1.1
  - — Supports optional wake from D3cold (via configuration strap option when Vaux is available)
  - — Wake on LAN
  - — Wake on link status change (energy detect)
  - — Magic packet wakeup
- General Purpose I/O
  - — 3 programmable GPIO pins
  - — 2 GPO pins
- Support for Optional EEPROM
  - — Serial interface provided for EEPROM
  - — Used to store PCI and MAC address configuration values
- Miscellaneous Features
  - — Big/Little/Mixed endian support for registers, descriptors, and buffers
  - — IRQ deassertion timer
  - — General purpose timer
- Single 3.3V Power Supply
  - — Integrated 1.8V regulator
- Packaging
  - — Available in 128-pin VTQFP Lead-free RoHS Compliant package
- Environmental
  - — Available in commercial & industrial temperature ranges

Order Numbers:

LAN9420-NU For 128-PIN, VTQFP Lead-Free, RoHS Compliant Package (0 to 70°C)

LAN9420I-NU For 128-PIN, VTQFP Lead-Free, RoHS Compliant Package (-40° to 85°C)

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000 or 1 (800) 443-SEMI

General Description

LAN9420/LAN9420i is a full-featured, Fast Ethernet controller which allows for the easy and cost-effective integration of Fast Ethernet into a PCI-based system. A system configuration diagram of LAN9420/LAN9420i in a typical embedded environment can be seen in Figure 1 on page 4, followed by an internal block diagram of LAN9420/LAN9420i in Figure 2 on page 4. LAN9420/LAN9420i consists of a PCI Local Bus Specification Revision 3.0 compliant interface, DMA Controller, Ethernet MAC, and 10/100 Ethernet PHY.

LAN9420/LAN9420i provides full IEEE 802.3 compliance and all internal components support full/half-duplex 10BASE-T, 100BASE-TX, and manual full-duplex flow control. The descriptor based scatter-gather DMA supports usage of zero-copy drivers, effectively increasing throughput while decreasing Host load. The integrated IRQ deassertion timer allows a minimum IRQ deassertion time to be set, providing reduced Host load and greater control over service routines. Automatic 32-bit CRC generation/checking, automatic payload padding, and 2K jumbo packets (2048 byte) are supported.

Big, little, and mixed endian support provides independent control over register, descriptor, and buffer endianess. This feature enables easy integration into various ARM/MIPS/PowerPC designs.

LAN9420/LAN9420i supports the PCI Bus Power Management Interface Specification Revision 1.1 and provides the optional ability to generate wake events in the D3cold state when Vaux is available. Wake on LAN, wake on link status change (energy detect), and magic packet wakeup detection are also supported, allowing for a range of power management options.

LAN9420/LAN9420i contains an EEPROM controller for connection to an optional EEPROM. This allows for the automatic loading of static configuration data upon power-up or reset. When connected, the EEPROM can be configured to load a predetermined MAC address, the PCI SSID, and the PCI SSVID of LAN9420/LAN9420i.

In addition to the primary functionality described above, LAN9420/LAN9420i provides additional features designed for extended functionality. These include a multipurpose 16-bit configurable General Purpose Timer (GPT), a Free-Run Counter, a 3-pin configurable GPIO/LED interface, and 2 GPO pins. All aspects of LAN9420/LAN9420i are managed via a set of memory mapped control and status registers.

LAN9420/LAN9420i's performance and features make it an ideal solution for many applications in the consumer electronics, enterprise, and industrial automation markets. Targeted applications include: set top boxes (cable, satellite and IP), digital televisions, digital video recorders, home gateways, digital media clients/servers, industrial automation systems, industrial single board PCs, and kiosk/POS enterprise equipment.

Block Diagrams

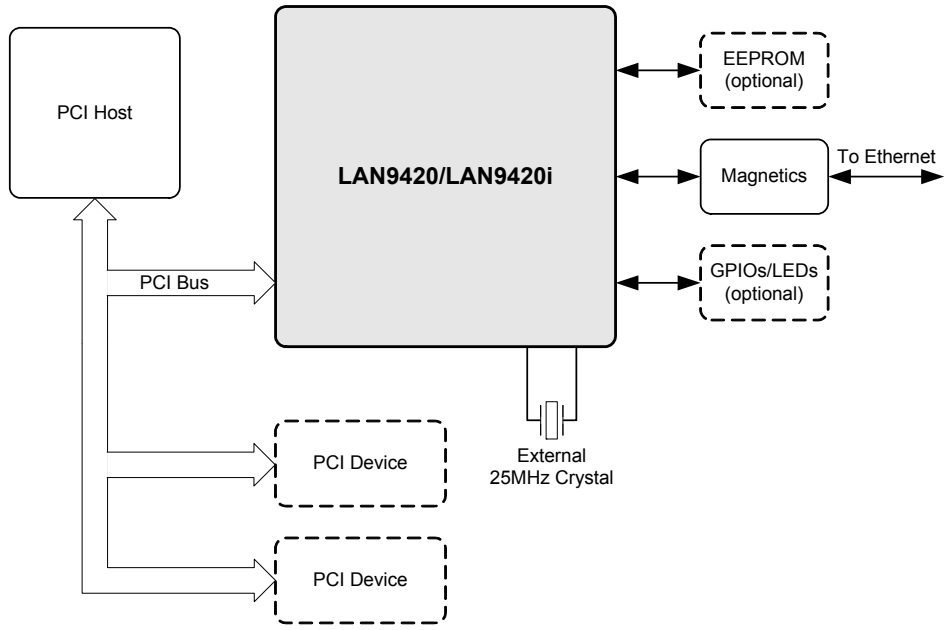

Figure 1 LAN9420/LAN9420i System Level Block Diagram

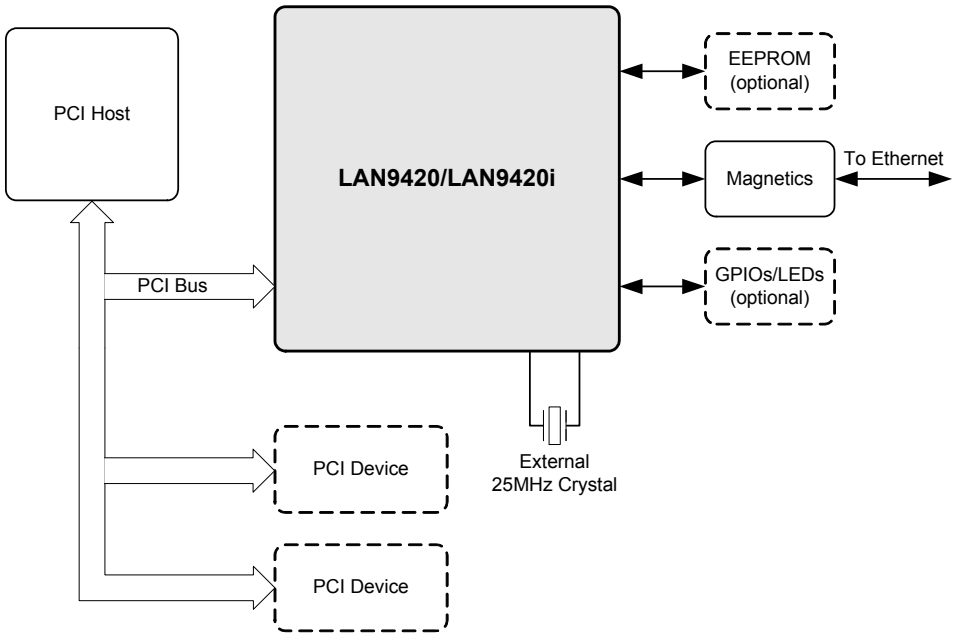

Figure 2 LAN9420/LAN9420i Internal Block Diagram

Package Outline

128-VTQFP Package

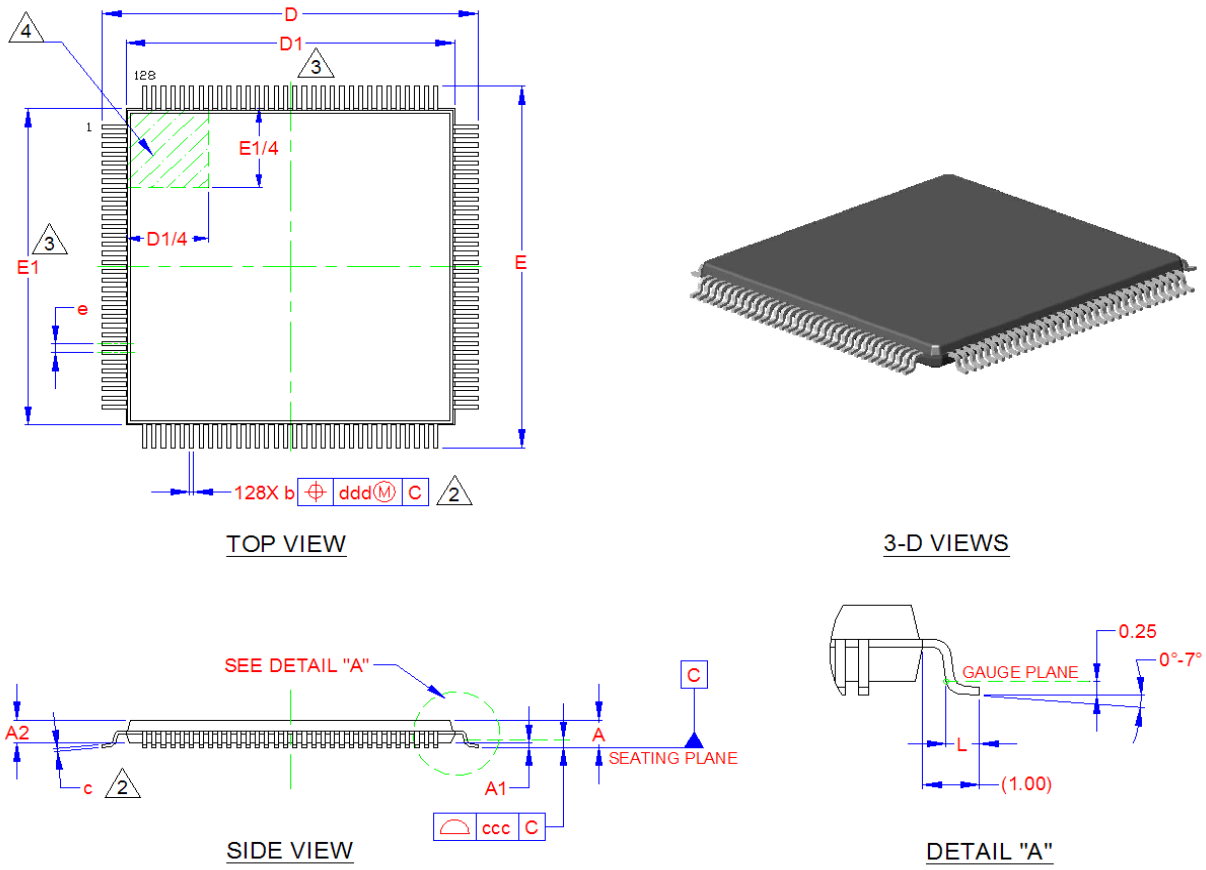

Figure 3 LAN9420/LAN9420i 128-VTQFP Package Definition

Table 1 LAN9420/LAN9420i 128-VTQFP Dimensions

	MIN	NOMINAL	MAX	REMARKS
A	-	-	1.20	Overall Package Height
A1	0.05	-	0.15	Standoff
A2	0.95	1.00	1.05	Body Thickness
D/E	15.80	16.00	16.20	X/Y Span
D1/E1	13.80	14.00	14.20	X/Y Plastic Body Size
L	0.45	0.60	0.75	Lead Foot Length
b	0.13	0.18	0.23	Lead Width
c	0.09	-	0.20	Lead Foot Thickness
e		0.40 BSC		Lead Pitch
ddd	0.00	-	0.07	True Position Spread
ccc	-	-	0.08	Coplanarity

Notes:

1. All dimensions are in millimeters unless otherwise noted.
2. Dimensions b & c apply to the flat section of the lead foot between 0.10 and 0.25mm from the lead tip. The base metal is exposed at the lead tip.
3. Dimensions D1 and E1 do not include mold protrusions. Maximum allowed protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. The pin 1 identifier may vary, but is always located within the zone indicated.

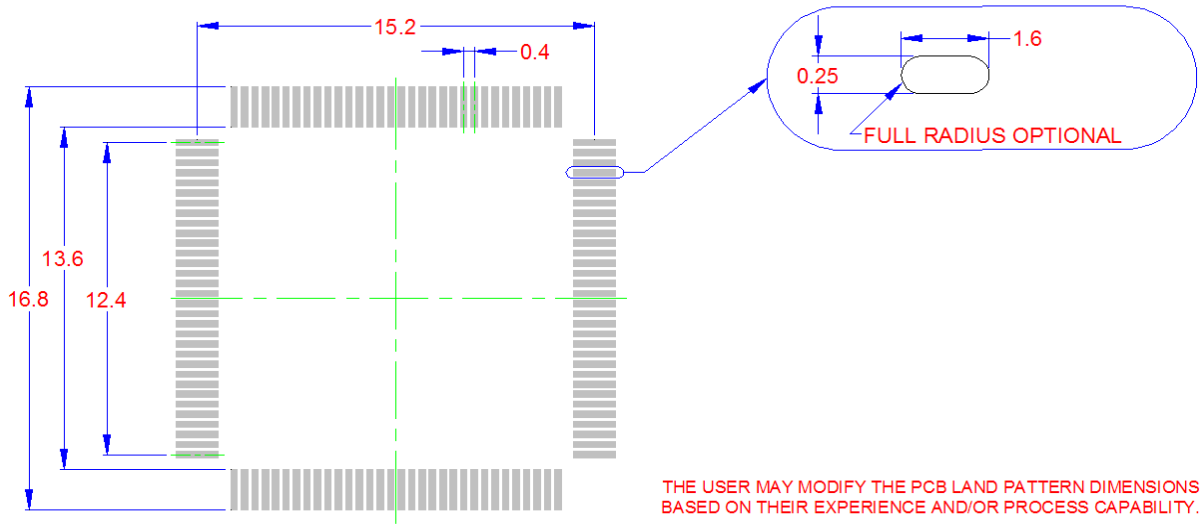

Figure 4 LAN9420/LAN9420i 128-VTQFP Recommended PCB Land Pattern