190717570 Si5383/84 Rev D Data Sheet Revision 1.1

PCN Issue Date: 7/17/2019   **Effective Date:** 10/23/2019

PCN Type: Datasheet

Description of Change

Silicon Labs is pleased to announce the release of the Si5383/84 Rev D Data Sheet from document revision 1.0 to documents revision 1.1.

A detailed description of the changes to the data sheet are summarized in the change impact section of this document.

Customers are encouraged to download the most recent version of CBPro, 2.35 or later, to take advantage of the latest software features and algorithms. A detailed description of changes for each CBPro release is available at https://www.silabs.com/documents/public/release-notes/ClockBuilder-Pro-README.pdf.

Reason for Change

Data sheet was updated to reflect device performance, changes made to specification tables, added additional application support information, and corrected some minor errors. A list of specific changes are below.

Impact on Form, Fit, Function, Quality, Reliability

There is no impact on form fit, quality and reliability. Details related to changes in function and application are below as well as a typographical correction to the package form. Note, the package dimension update does not cause a change in the actual product:

Si5383/84 Rev D Data Sheet Revision 1.1 changes
• Updated Figure 3.5 Crystal Resonator Connections on page 12.
  • Updated Crystal Resonator Connection diagram and added connection diagrams for Differential XO/Clock and Single-Ended XO.
• Updated Figure 3.6 External Reference Connections on page 13.
  • Updated diagram with additional information on input divider circuity to attenuate input to not exceed spec limit.
• Updated Figure 3.19 Supported Differential Output Terminations on page 24.
  • Updated AC-Coupled LVDS/LVPECL figure to clarify LVDS and LVPECL Vddo voltage support.
• Updated 3.10.8 LVCMOS Output Polarity.
  • Clarified language used to describe that LVCMOS output polarity is configurable, enabling either in-phase or complementary clock generation.
• Updated 5. Electrical Specifications.
  • Updated Table 5.3 Input Clock Specifications on page 31.
    • Removed LVCMOS from Standard Input Buffer with Differential or Single-Ended Configuration description to be more in line with other Silicon Labs products.
    • Input Capacitance, CIN changed to 2.4pf to match IBIS model.
    • Input Frequency parameter changes.
      • Change fIN_PULSED to fIN_CMOS.
      • Changed Standard Mode Test Condition to LVCMOS Mode.
      • Added Pulsed CMOS Mode Test Condition and spec limits.
    • Minimum Pulse Width parameter changes.
      • Changed Standard Mode to LVCMOS CMOS Mode (250 MHz @ 40% Duty Cycle).
      • Added Pulsed CMOS (1 MHz @ 5% Duty Cycle) test condition and spec limits.
    • Duty Cycle parameter added.
      • Added Duty Cycle Test Conditions and spec limits for LVCMOS and Pulsed CMOS.
  • Updated Table 5.4 Control Input Pin Specifications on page 33.
    • Input Capacitance, CIN changed to 1.5 pF to match IBIS model.
  • Updated Table 5.5 Differential Clock Output Specifications on page 34.
    • Duty Cycle (DC) – 2nd row of Test Condition table - 712.5 MHz changed to 718.5 MHz.
    • Vpp_diff = 2*Vpp_se diagram – Moved diagram under Note 1.
  • Updated Table 5.6 LVCMOS Clock Output Specifications on page 35
    • Output Voltage Low Parameter – Removed reference to Note 3, it does not apply.
  • Updated Table 5.7 Output Status Pin Specifications on page 37.
    • Removed VDDO = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5% from conditions at top of table.
  • Updated Table 5.8 Performance Characteristics on page 37.
    • Updated PLL Lock Time Parameter.
      • Added fIN = 19.44 MHz; Ramped Exit from Holdover enabled (recommended) Test Condition and 1900 s typical spec added to reflect typical lock time when recommended Ramped Exit from Holdover setting is used.
      • 1 pps Mode8 Phase error < 10 ns Test Condition and typical 25 s spec added. Note 8 added at bottom of table.
      • 1 pps Mode9 Test Condition updated with "Fully Locked", max spec removed, and typical spec of 2 min added to reflect typical lock time under conditions of Note 9 at bottom of table.
      • Added Note 10 to fIN = 19.44 MHz; Ramped Exit from Holdover enabled (recommended)10.
      • Pull-in Range6 Parameter – Standard mode test condition spec changed to 500 ppm typical to reflect spec limits of similar Silicon Labs products.
      • Input-to-Output Delay Variation8 Parameter, tIODELAY – Specification Removed - Under high device junction temperatures, it is possible that all of the output Multisynths may not start exactly at the same time. This effect may be different after each reset or power cycle at high temperatures.
Si5383/84 Rev D Data Sheet
• Updated 9. Pin Descriptions.
  • Updated Table 9.1 Si5383/84 Pin Descriptions 1 on page 46.
    • Added Note 3 to OUT2 and OUT2b Pin names.
• Updated 10. Package Outline.
  • Updated Table 10.1 Package Dimensions on page 49.
    • Dimension A Min spec changed to 0.80 and Nom. Spec changed to 0.90. Both specification changes reflect a lower overall package height than was originally on the datasheet. These dimension were incorrect when datasheet was released.
• Updated 11. PCB Land Pattern.
  • Updated Table 11.1 PCB Land Pattern Dimensions on page 52.
    • Stencil Design Note 4 changed to reflect recommendation for an LGA package. Original Note 4 applied to QFN package.

Product Identification

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Existing Part #
SI5383A-D00100-GM
SI5383A-D00100-GMR
SI5383A-D05886-GM
SI5383A-D05886-GMR
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SI5383A-D06791-GM
SI5383A-D06791-GMR
SI5383A-D07163-GM
SI5383A-D07163-GMR
SI5383A-D07165-GM
SI5383A-D07165-GMR
SI5383A-D07172-GM
SI5383A-D07172-GMR
SI5383A-D07185-GM
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SI5383B-D10003-GMR
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SI5383B-D10476-GMR
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SI5384A-D07173-GM
SI5384A-D07173-GMR
SI5384A-D07186-GM
SI5384A-D07186-GMR
SI5384A-D09306-GM
SI5384A-D09306-GMR
SI5384A-D09315-GM
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SI5384A-D-GM
SI5384A-D-GMR
SI5384B-D00100-GM
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SI5384B-D00100-GMR
SI5384B-D07686-GM
SI5384B-D07686-GMR
SI5384B-D07700-GM
SI5384B-D07700-GMR
SI5384B-D-GM
SI5384B-D-GMR
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Last Date of Unchanged Product: 10/23/2019

Qualification Samples

NA

Customer Response

Lack of acknowledgment of the PCN within 30 days constitutes acceptance of the change, Ref. JEDEC-J-STD-046.

To request further data or inquire about this notification, please contact your Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at http://www.silabs.com.
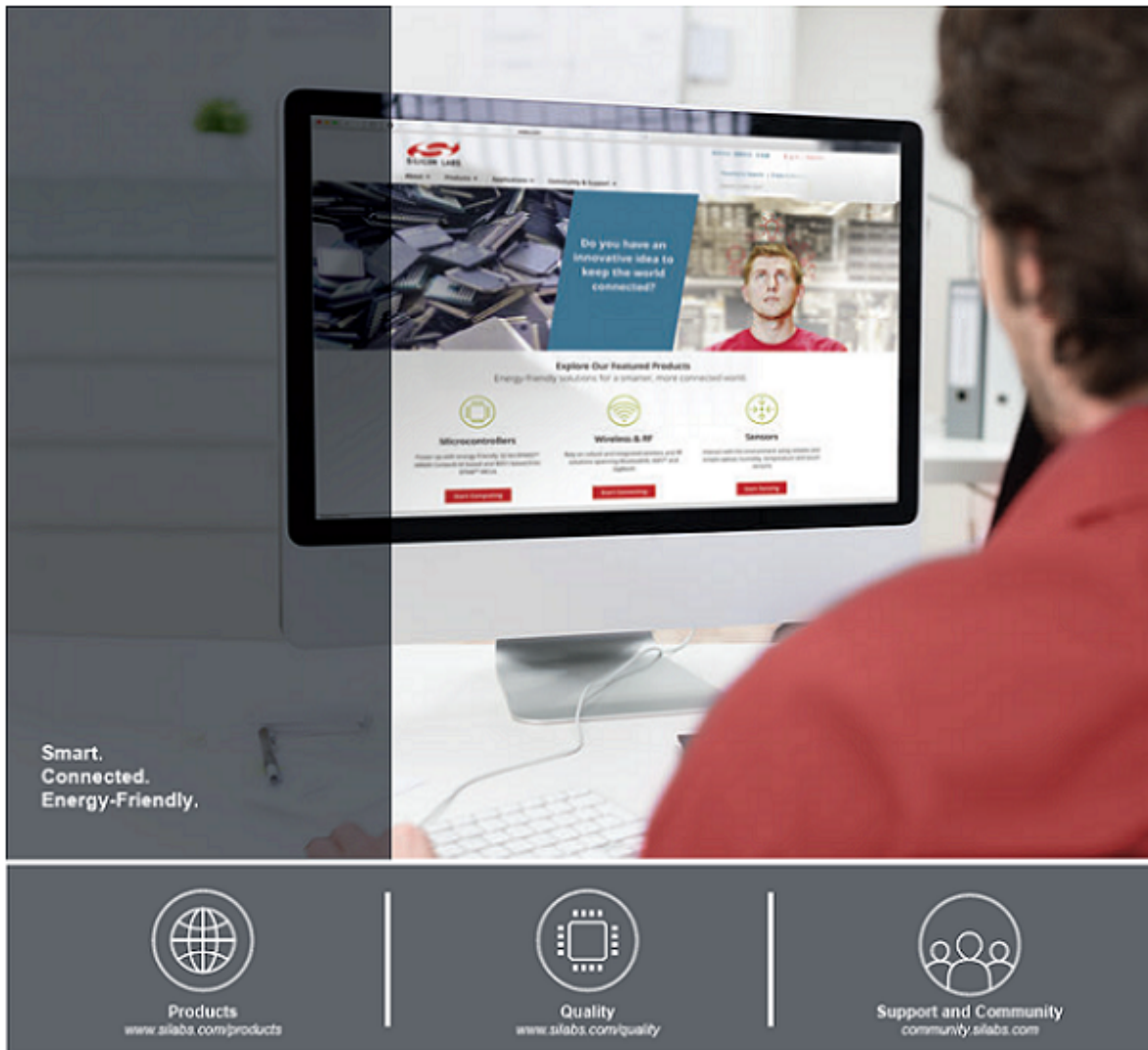
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