Cypress Semiconductor Corporation, 198 Champion Court, San Jose, CA 95134. Tel (408)943-2600

PRODUCT INFORMATION NOTIFICATION

PIN: PIN145325 **Date:** July 09, 2014

Subject: Mask Changes for CY2291/CY2292 Product Families to Fix Design Marginality Issues.

Change Type: N/A

Product Information: Cypress has fixed the design marginality issue seen on CY2291/CY2292 devices through a mask change. This change does not affect any Form, Fit or Function of the devices and all datasheet parameters remain the same.

Background: Cypress's CY2291/CY2292 is a family of EPROM based programmable clock generators that have three Phase-Locked Loops (PLLs); 1) CPU PLL (CPLL), 2) System Clock PLL (SPLL), and 3) Utility PLL (UPLL). It supports 3.3V/5V Vdd range and can operate up to a maximum frequency of 100MHz.

In May 2012, Cypress had identified a minor design marginality with the CY2291/CY2292 family of devices that caused the CPLL to not achieve phase lock within the datasheet specification of 50ms. This occurred during device startup and in an application environment with certain Temperature/Vcc/noise levels. The other two PLLs (SPLL and UPLL) were not affected by this startup issue.

No field failures were reported due to the above issue. As a proactive containment measure, Cypress implemented a test screen on May 30, 2012 which was communicated through PIN 125151.

The mask change has completely resolved this issue.

Affected Part Numbers: 28
Affected Parts: Please see attached sheet for the parts list.

Qualification Status:
The design fix has been qualified through a series of tests identified in Qualification Test Plan (QTP) Report No. 124910. The QTP report can be found in the attachment to this notification or by visiting www.cypress.com and typing the QTP number in the keyword search window.

Approximate Implementation Date:
Cypress will transition to shipments of the new parts starting August 15, 2014.

Anticipated Impact:
Products manufactured with the design fix are completely compatible with existing products from a functional, parametric, and quality performance perspective.

Cypress recommends that customers take this opportunity to review these changes against current application notes, system design considerations and customer environment conditions to assess impact (if any) to their application.

Method of Identification:
Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

Response Required:
This is an information only announcement. No response is required.

For additional information regarding this change, contact your local sales representative or contact the PCN Administrator at pcn_adm@cypress.com.

Sincerely,

Cypress PCN Administration