Switching Regulator IC for Buck Converter

w/ 40V/1A or 40V/600mA MOSFET

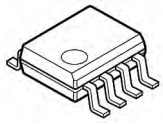
■ GENERAL DESCRIPTION

The **NJW4152** is a buck converter with **40V/1A** or **40V/600mA** MOSFET. It corresponds to high oscillating frequency, and Low ESR Output Capacitor (MLCC) within wide input range from 4.6V to 40V. Therefore, the **NJW4152** can realize downsizing of an application with a few external parts.

Also, it has a soft start function, an over current protection and a thermal shutdown circuit. Moreover there is an automotive for extended operating temperature range version.

It is suitable for logic voltage generation from high voltage that Car Accessory, Office Automation Equipment, Industrial Instrument and so on.

■ PACKAGE OUTLINE



NJW4152GM1-A
(HSOP8)

NJW4152R-B
(MSOP8 (VSP8))

■ FEATURES

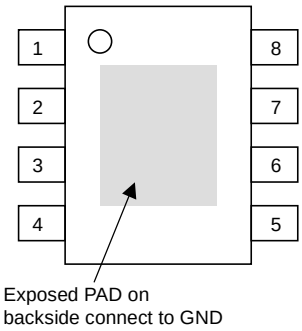
- Maximum Rating Input Voltage 45V
- Wide Operating Voltage Range 4.6V to 40V
- Switching Current 1.4A(min.) @A version
  0.8A(min.) @B version
- PWM Control
- Wide Oscillating Frequency 300kHz to 1MHz
- Soft Start Function 4ms typ.
- UVLO (Under Voltage Lockout)
- Over Current Protection / Thermal Shutdown Protection
- Standby Function
- Package Outline NJW4152GM1: HSOP8
  NJW4152R: MSOP8 (VSP8)* *MEET JEDEC MO-187-DA

■ PRODUCT CLASSIFICATION

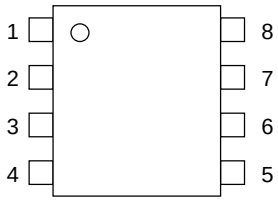
Part Number	Version	Output Current	Switching Current Limit (MIN.)	Operating Voltage	Package
NJW4152GM1-A	A	1.0A	1.4A	4.6 to 40V	HSOP8
NJW4152GM1-AB	AB	1.0A	1.4A	3.6 to 40V	HSOP8
NJW4152R-B	B	600mA	0.8A	4.6 to 40V	MSOP8 (VSP8)

This data sheet is applied to "NJW4152GM1-A, NJW4152R-B".
Please refer to each data sheet for other versions.

■ PIN CONFIGURATION



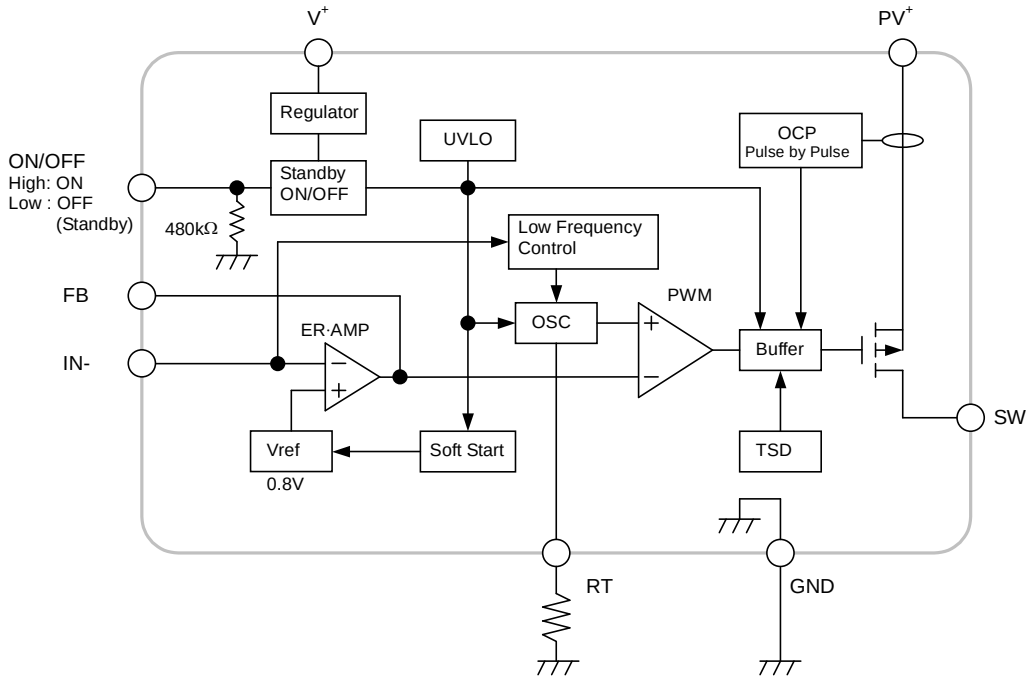
NJW4152GM1-A



NJW4152R-B

PIN FUNCTION
1. PV^+
2. V^+
3. ON/OFF
4. RT
5. IN-
6. FB
7. GND
8. SW

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT
Supply Voltage (V^+ pin, PV^+ pin)	V^+	+45	V
PV^+- SW pin Voltage	V_{PV-SW}	+45	V
IN- pin Voltage	V_{IN-}	-0.3 to +6	V
ON/OFF pin Voltage	$V_{ON/OFF}$	+45	V
Power Dissipation	P_D	HSOP8 790 (*1) 2,500 (*2) MSOP8(VSP8) 595 (*3) 805 (*4)	mW
Junction Temperature Range	Tj	-40 to +150	°C
Operating Temperature Range	T_{opr}	-40 to +85	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

(*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

(*3): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*4): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers), internal Cu area: 74.2×74.2mm

■ RECOMMENDED OPERATING CONDITIONS

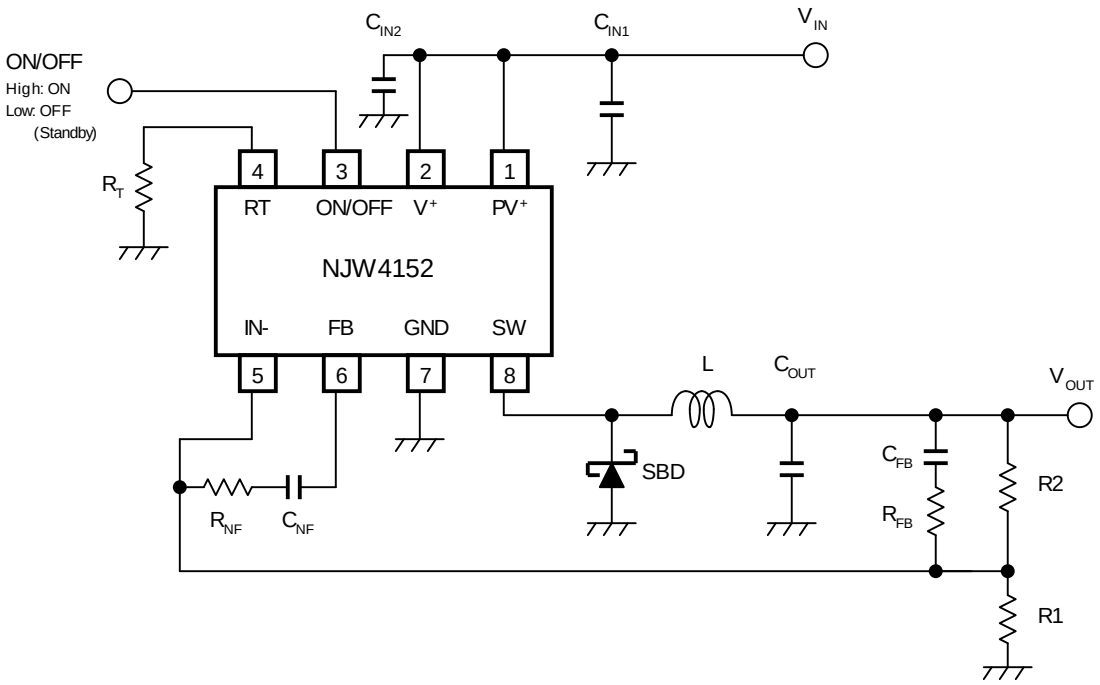
PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage		V^+	4.6	–	40	V
Output Current (*5)	A version	I_{OUT}	–	–	1.0	A
	B version		–	–	0.6	A
Timing Resistor		R_T	18	27	68	kΩ
Oscillating Frequency		fosc	300	700	1,000	kHz

(*5): At Static Status

■ ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $V^+=V_{ON/OFF}$=12V, R_T=27kΩ, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Under Voltage Lockout Block						
ON Threshold Voltage	V_{T_ON}	V^+= L → H	4.3	4.5	4.6	V
OFF Threshold Voltage	V_{T_OFF}	V^+= H → L	4.2	4.4	4.54	V
Hysteresis Voltage	V_{HYS}		60	100	–	mV
Soft Start Block						
Soft Start Time	T_{SS}	V_B=0.75V	2	4	8	ms
Oscillator Block						
Oscillation Frequency	f_{OSC}		630	700	770	kHz
Oscillation Frequency (Low Frequency Control)	f_{OSC_LOW}	V_{IN-}=0.4V, V_{FB}=0.55V	–	270	–	kHz
RT pin Voltage	V_{RT}		0.24	0.275	0.31	V
Oscillation Frequency deviation (Supply voltage)	f_{DV}	V^+=4.6 to 40V	–	1	–	%
Oscillation Frequency deviation (Temperature)	f_{DT}	Ta=-40°C to +85°C	–	2	–	%
Error Amplifier Block						
Reference Voltage	V_B		-1.0%	0.8	+1.0%	V
Input Bias Current	I_B		-0.1	–	+0.1	μA
Open Loop Gain	A_V		–	80	–	dB
Gain Bandwidth	G_B		–	0.6	–	MHz
Output Source Current	I_{OM+}	V_{FB}=1V, V_{IN-}=0.7V	8	16	24	μA
Output Sink Current	I_{OM-}	V_{FB}=1V, V_{IN-}=0.9V	1	2	4	mA
PWM Comparate Block						
Maximum Duty Cycle	$M_{AX}D_{UTY}$	V_{IN-}=0.7V	100	–	–	%
Output Block						
Output ON Resistance	R_{ON}	A version, I_{SW}=1A	–	0.3	0.5	Ω
		B version, I_{SW}=0.6A	–	0.28	0.48	Ω
Switching Current Limit	I_{LIM}	A version	1.4	1.7	2.0	A
		B version	0.8	1.0	1.3	A
Switching Leak Current	I_{LEAK}	$V_{ON/OFF}$=0V, V^+=45V, V_{SW}=0V	–	–	1	μA
ON/OFF Block						
ON Control Voltage	V_{ON}	$V_{ON/OFF}$= L → H	1.6	–	V^+	V
OFF Control Voltage	V_{OFF}	$V_{ON/OFF}$= H → L	0	–	0.5	V
Pull-down Resistance	R_{PD}		–	480	–	kΩ
General Characteristics						
Quiescent Current	I_{DD}	R_L=no load, V_{IN-}=0.7V, V_{FB}=0.55V	–	2.5	2.8	mA
Standby Current	I_{DD_STB}	$V_{ON/OFF}$=0V	–	–	1	μA

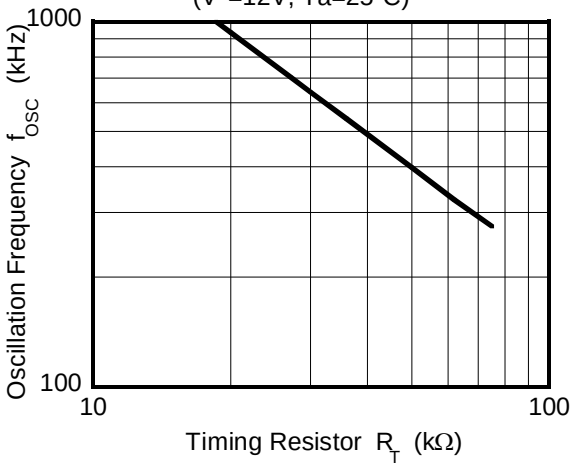
■ TYPICAL APPLICATIONS



■ CHARACTERISTICS

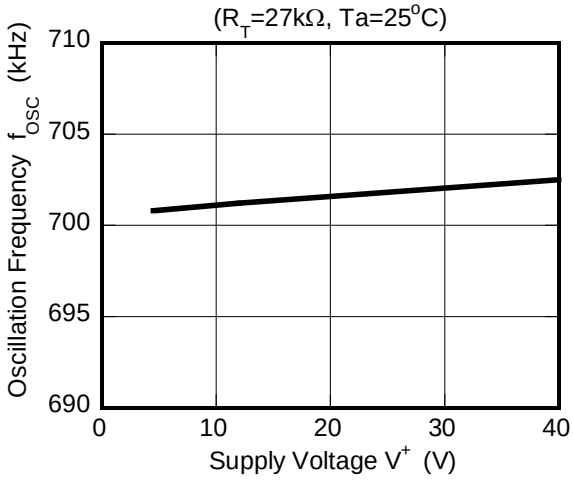
Timing Resistor vs.Oscillation Frequency

(V^+=12V, Ta=25°C)



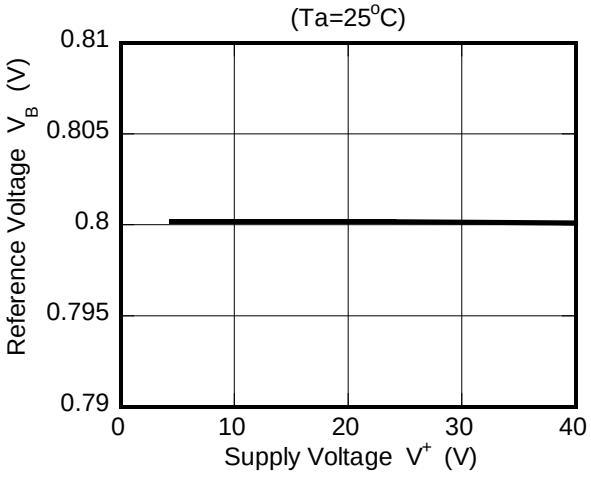
Oscillation Frequency vs. Supply Voltage

(R_T=27kΩ, Ta=25°C)



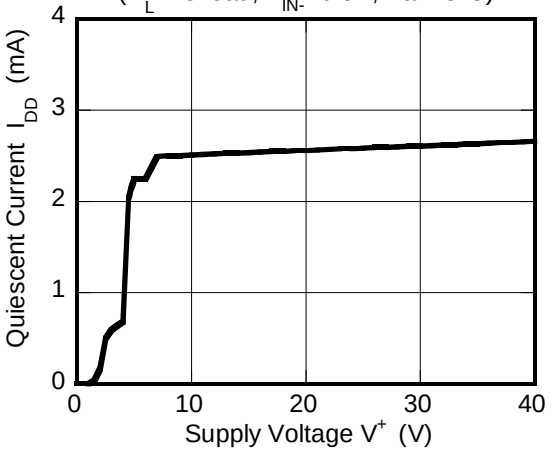
Reference Voltage vs. Supply Voltage

(Ta=25°C)



Quiescent Current vs. Supply Voltage

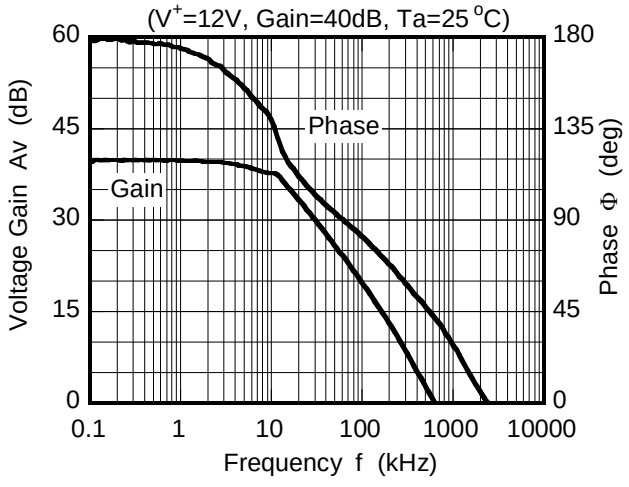
(R_L=no load, V_{IN-}=0.5V, Ta=25°C)



Error Amplifier Block

Voltage Gain, Phase vs. Frequency

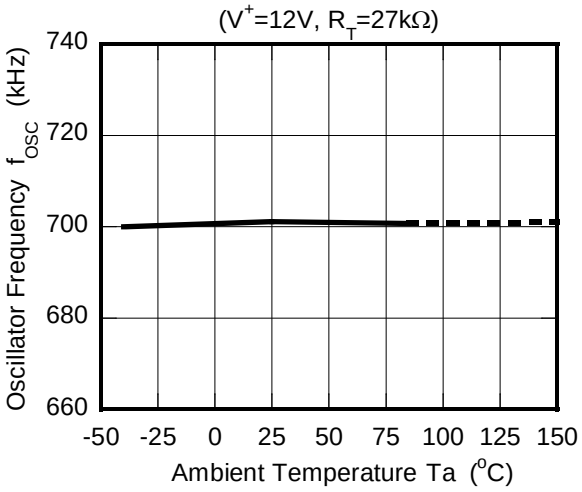
(V^+=12V, Gain=40dB, Ta=25 °C)



■ CHARACTERISTICS

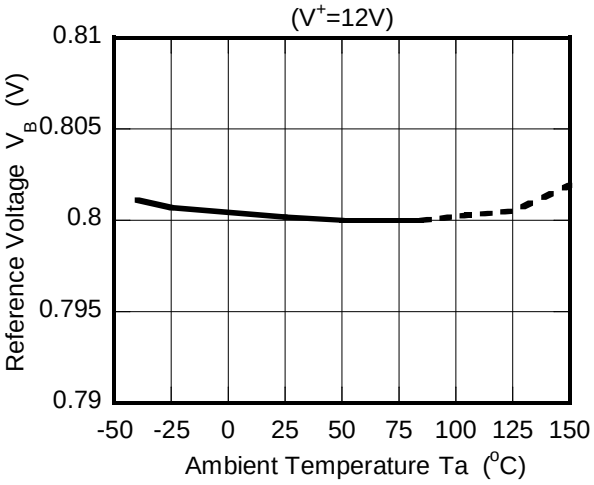
Oscillator Frequency vs. Temperature

(V^+=12V, R_T=27kΩ)



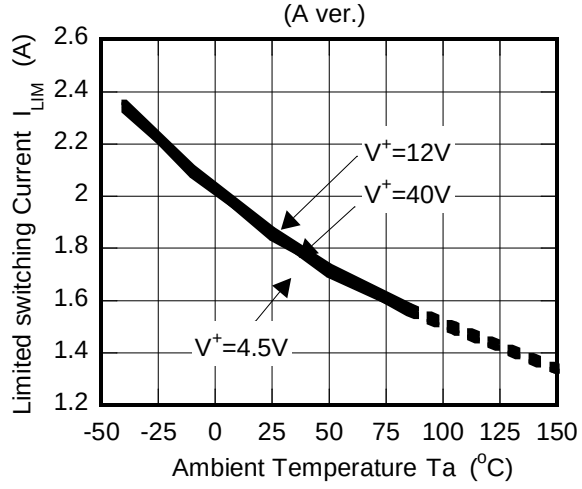
Reference Voltage vs. Temperature

(V^+=12V)



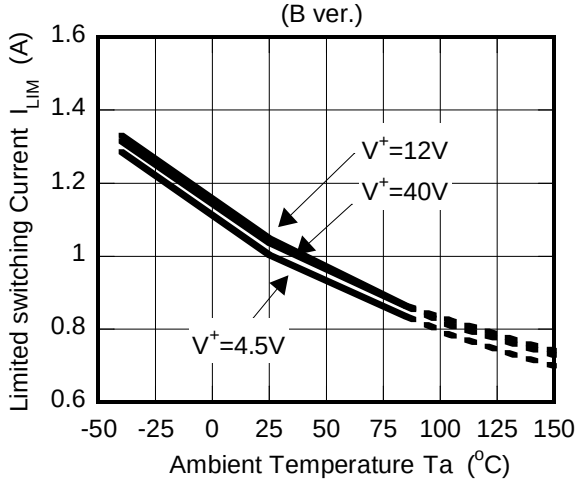
Limited Switching Current vs. Temperature

(A ver.)



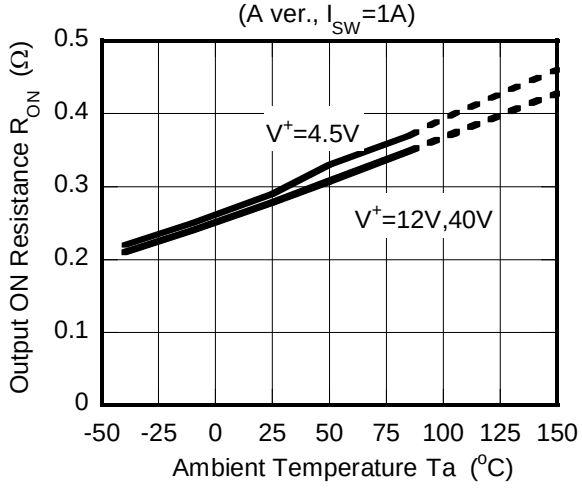
Limited Switching Current vs. Temperature

(B ver.)



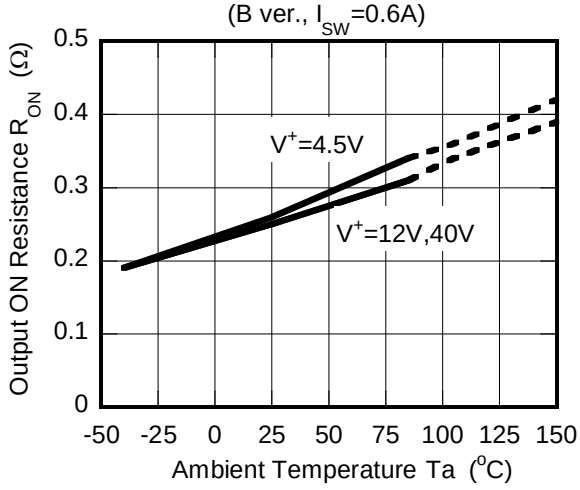
Output ON Resistance vs.Temperature

(A ver., I_{SW}=1A)



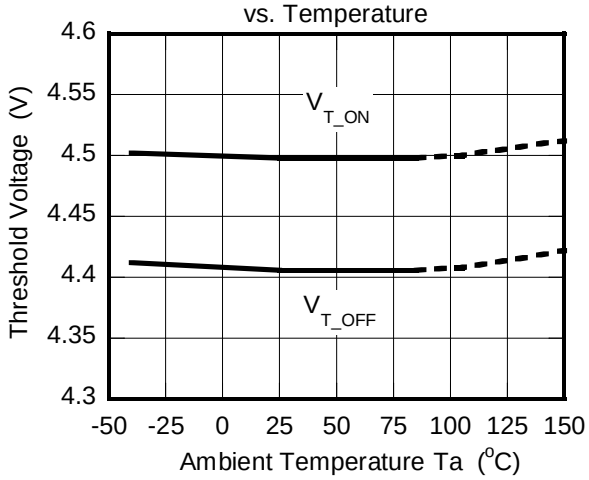
Output ON Resistance vs.Temperature

(B ver., I_{SW}=0.6A)

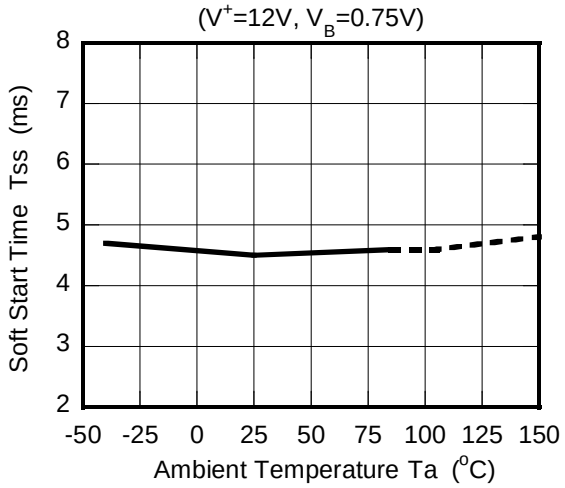


■ CHARACTERISTICS

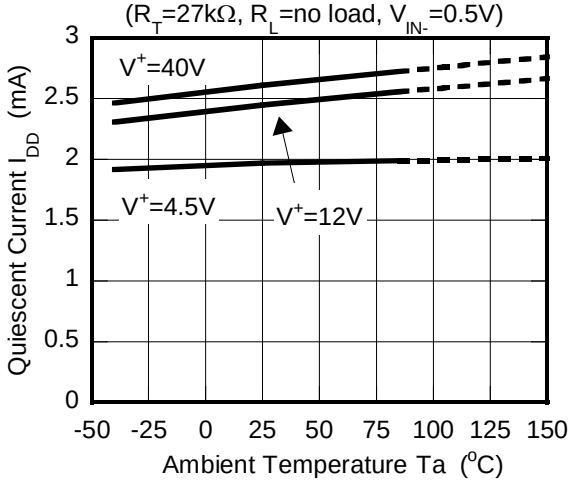
Under Voltage Lockout Voltage vs. Temperature



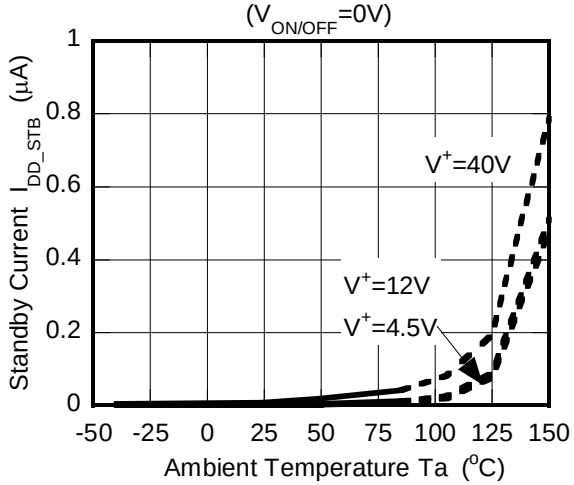
Soft Start Time vs. Temperature (V^+=12V, V_B=0.75V)



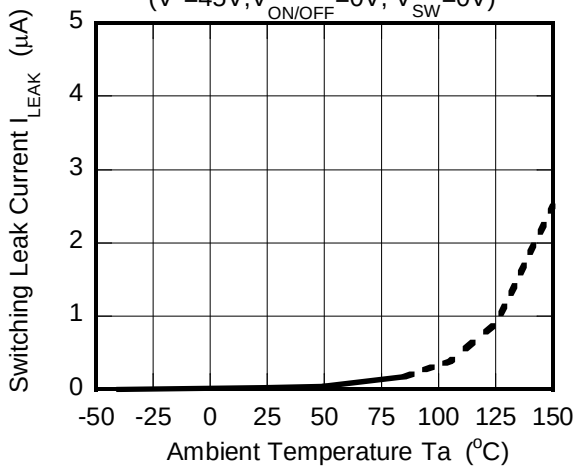
Quiescent Current vs. Temperature (R_T=27kΩ, R_L=no load, V_{IN-}=0.5V)



Standby Current vs. Temperature ($V_{ON/OFF}$=0V)



Switching Leak Current vs. Temperature (V^+=45V,$V_{ON/OFF}$=0V, V_{SW}=0V)



■ PIN DESCRIPTIONS

PIN NUMBER	PIN NAME	FUNCTION
1	PV^+	Power Supply pin for Power Line
2	V^+	Power Supply pin for IC Control
3	ON/OFF	ON/OFF Control pin The ON/OFF pin internally pulls down with 480kΩ. Normal Operation at the time of High Level. Standby Mode at the time of Low Level or OPEN.
4	RT	Oscillating Frequency Setting pin by Timing Resistor. Oscillating Frequency should set between 300kHz and 1MHz.
5	IN-	Output Voltage Detecting pin Connects output voltage through the resistor divider tap to this pin in order to voltage of the IN- pin become 0.8V.
6	FB	Feedback Setting pin The feedback resistor and capacitor are connected between the FB pin and the IN- pin.
7	GND	GND pin
8	SW	Switch Output pin of Power MOSFET
–	Exposed PAD	Connect to GND (only HSOP8 PKG)

■ Description of Block Features

1. Basic Functions / Features

● Error Amplifier Section (ER·AMP)

0.8V±1% precise reference voltage is connected to the non-inverted input of this section.

To set the output voltage, connects converter's output to inverted input of this section (IN- pin). If requires output voltage over 0.8V, inserts resistor divider.

This AMP section has high gain and external feedback pin (FB pin). It is easy to insert a feedback resistor and a capacitor between the FB pin and the IN- pin, making possible to set optimum loop compensation for each type of application.

● Oscillation Circuit Section (OSC)

Oscillation frequency can be set by inserting resistor between the RT pin and GND. Referring to the sample characteristics in "Timing Resistor and Oscillation Frequency", set oscillation between 300kHz and 1MHz.

■ Description of Block Features (Continued)

● PWM Comparator Section (PWM)

This section controls the switching duty ratio.

PWM comparator receives the signal of the error amplifier and the triangular wave, and controls the duty ratio between 0% and 100%. The timing chart is shown in Fig.1.

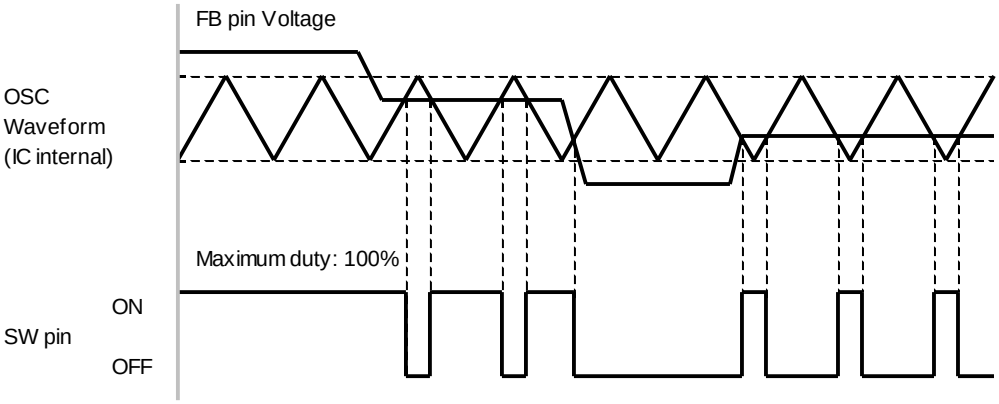


Fig. 1. Timing Chart PWM Comparator and SW pin

● Power MOSFET (SW Output Section)

The power is stored in the inductor by the switch operation of built-in power MOSFET. The output current is limited to 1.4A(min.)@A version and 0.8A(min.)@B version by the overcurrent protection function. In case of step-down converter, the forward direction bias voltage is generated with inductance current that flows into the external regenerative diode when MOSFET is turned off.

The SW pin allows voltage between the PV^+ pin and the SW pin up to +45V. However, you should use an Schottky diode that has low saturation voltage.

● Power Supply, GND pin (V^+, PV^+ and GND)

In line with switching element drive, current flows into the IC according to frequency. If the power supply impedance provided to the power supply circuit is high, it will not be possible to take advantage of IC performance due to input voltage fluctuation. Therefore insert a bypass capacitor close to the V^+ pin – the GND pin connection in order to lower high frequency impedance.

2. Additional and Protection Functions / Features

● Under Voltage Lockout (UVLO)

The UVLO circuit operating is released above V^+=4.5V(typ.) and IC operation starts. When power supply voltage is low, IC does not operate because the UVLO circuit operates. There is 100mV width hysteresis voltage at rise and decay of power supply voltage. Hysteresis prevents the malfunction at the time of UVLO operating and releasing.

● Soft Start Function (Soft Start)

The output voltage of the converter gradually rises to a set value by the soft start function. The soft start time is 4ms (typ). It is defined with the time of the error amplifier reference voltage becoming from 0V to 0.75V. The soft start circuit operates after the release UVLO and/or recovery from thermal shutdown. The operating frequency is controlled with a low frequency, approximately 40% of the set value by the timing resistor, until voltage of the IN- pin becomes approximately 0.4V.

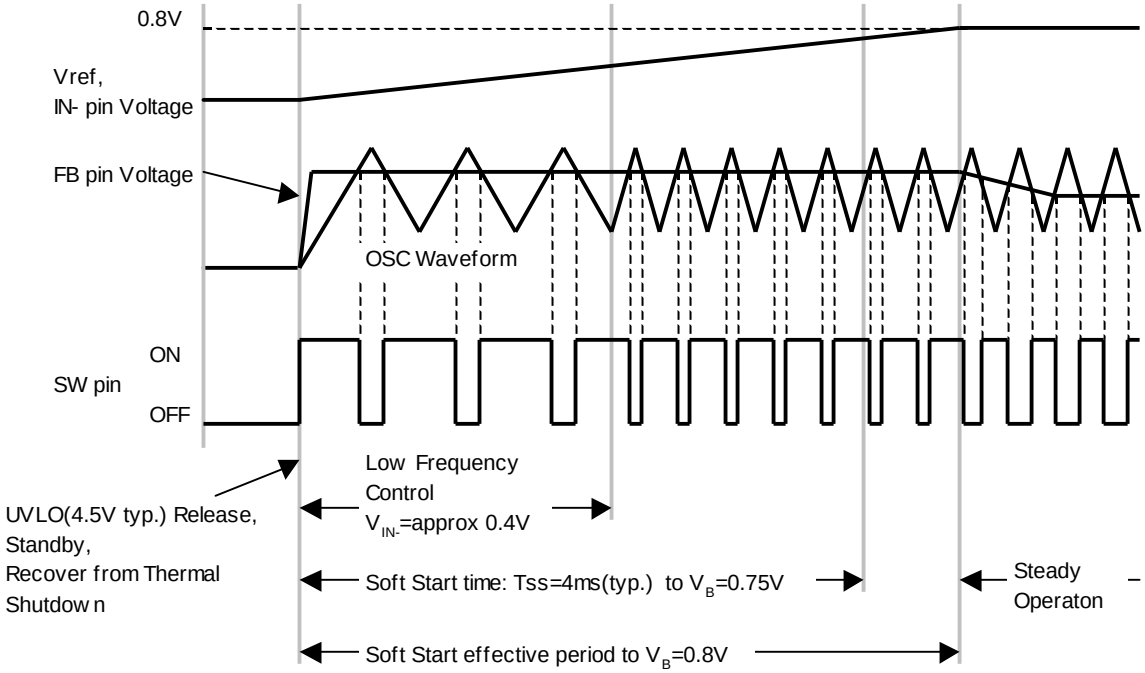


Fig. 2. Startup Timing Chart

■ Description of Block Features (Continued)

● Over Current Protection Circuit (OCP)

At when the switching current becomes I_{LIM} or more, the overcurrent protection circuit is stopped the MOSFET output. The switching output holds low level down to next pulse output at OCP operating.

The NJW4152 output returns automatically along with release from the over current condition because the OCP is pulse-by-pulse type.

Fig.3. shows the timing chart of the over current protection detection.

If voltage of the IN- pin becomes less than 0.4V, the oscillation frequency decreases to approximately 40% and the energy consumption is suppressed.

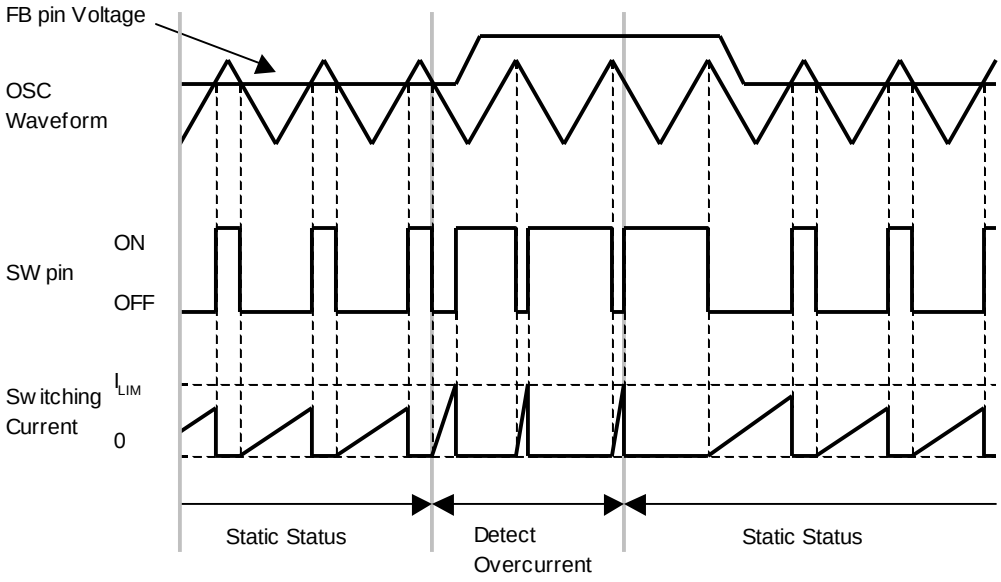


Fig. 3. Timing Chart at Over Current Detection

● Thermal Shutdown Function (TSD)

When Junction temperature of the NJW4152 exceeds the 175°C*, internal thermal shutdown circuit function stops SW function. When junction temperature decreases to 145°C* or less, SW operation returns with soft start operation.

The purpose of this function is to prevent malfunctioning of IC at the high junction temperature. Therefore it is not something that urges positive use. You should make sure to operate within the junction temperature range rated (150°C). (* Design value)

● ON/OFF Function (Standby Control)

The NJW4152 stops the operating and becomes standby status when the ON/OFF pin becomes less than 0.5V.

The ON/OFF pin internally pulls down with 480kΩ, therefore the NJW4152 becomes standby mode when the ON/OFF pin is OPEN. You should connect this pin to V^+ when you do not use ON/OFF function.

■ Application Information

● Inductors

Large currents flow into inductor, therefore you must provide current capacity that does not saturate.

Reducing L, the size of the inductor can be smaller. However, peak current increases and adversely affecting efficiency.

On the other hand, increasing L, peak current can be reduced at switching time. Therefore conversion efficiency improves, and output ripple voltage reduces. Above a certain level, increasing inductance windings increases loss (copper loss) due to the resistor element.

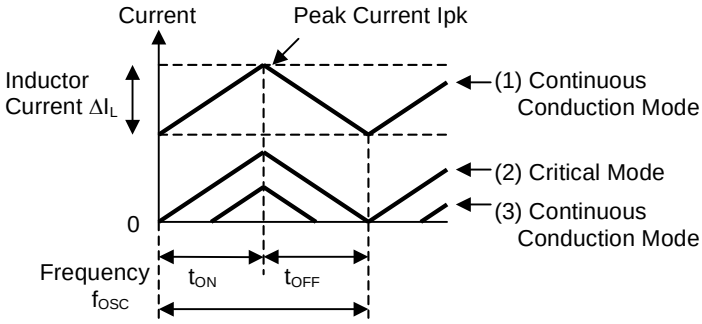


Fig. 4. Inductor Current State Transition

Ideally, the value of L is set so that inductance current is in continuous conduction mode. However, as the load current decreases, the current waveform changes from (1) CCM: Continuous Conduction Mode → (2) Critical Mode → (3) DCM: Discontinuous Conduction Mode (Fig. 4.).

In discontinuous mode, peak current increases with respect to output current, and conversion efficiency tend to decrease. Depending on the situation, increase L to widen the load current area to maintain continuous mode.

If the application needs maximum output current, the inductor ripple current should be set less than 20% to prevent operating the over current protection circuit at the minimum switching limiting current.

● Catch Diode

When the switch element is in OFF cycle, power stored in the inductor flows via the catch diode to the output capacitor. Therefore during each cycle current flows to the diode in response to load current. Because diode's forward saturation voltage and current accumulation cause power loss, a Schottky Barrier Diode (SBD), which has a low forward saturation voltage, is ideal.

An SBD also has a short reverse recovery time. If the reverse recovery time is long, through current flows when the switching transistor transitions from OFF cycle to ON cycle. This current may lower efficiency and affect such factors as noise generation.

● Input Capacitor

Transient current flows into the input section of a switching regulator responsive to frequency. If the power supply impedance provided to the power supply circuit is large, it will not be possible to take advantage of the NJW4152 performance due to input voltage fluctuation. Therefore insert an input capacitor as close to the MOSFET as possible.

● Output Capacitor

An output capacitor stores power from the inductor, and stabilizes voltage provided to the output.

When selecting an output capacitor, you must consider Equivalent Series Resistance (ESR) characteristics, ripple current, and breakdown voltage.

Also, the ambient temperature affects capacitors, decreasing capacitance and increasing ESR (at low temperature), and decreasing lifetime (at high temperature). Concerning capacitor rating, it is advisable to allow sufficient margin.

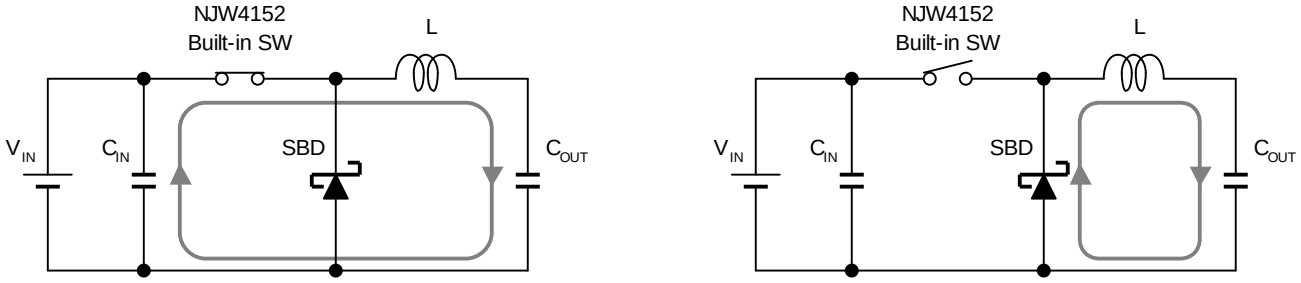
Output capacitor ESR characteristics have a major influence on output ripple noise. A capacitor with low ESR can further reduce ripple voltage. Be sure to note the following points; when ceramic capacitor is used, the capacitance value decreases with DC voltage applied to the capacitor.

■ Application Information (Continued)

● Board Layout

In the switching regulator application, because the current flow corresponds to the oscillation frequency, the substrate (PCB) layout becomes an important.

You should attempt the transition voltage decrease by making a current loop area minimize as much as possible. Therefore, you should make a current flowing line thick and short as much as possible. Fig.5. shows a current loop at step-down converter. Especially, should lay out high priority the loop of C_{IN}-SW-SBD that occurs rapid current change in the switching. It is effective in reducing noise spikes caused by parasitic inductance.



(a) Buck Converter SW ON (b) Buck Converter SW OFF

Fig. 5. Current Loop at Buck Converter

Concerning the GND line, it is preferred to separate the power system and the signal system, and use single ground point.

The voltage sensing feedback line should be as far away as possible from the inductance. Because this line has high impedance, it is laid out to avoid the influence noise caused by flux leaked from the inductance.

Fig. 6. shows example of wiring at buck converter. Fig. 7 shows the PCB layout example.

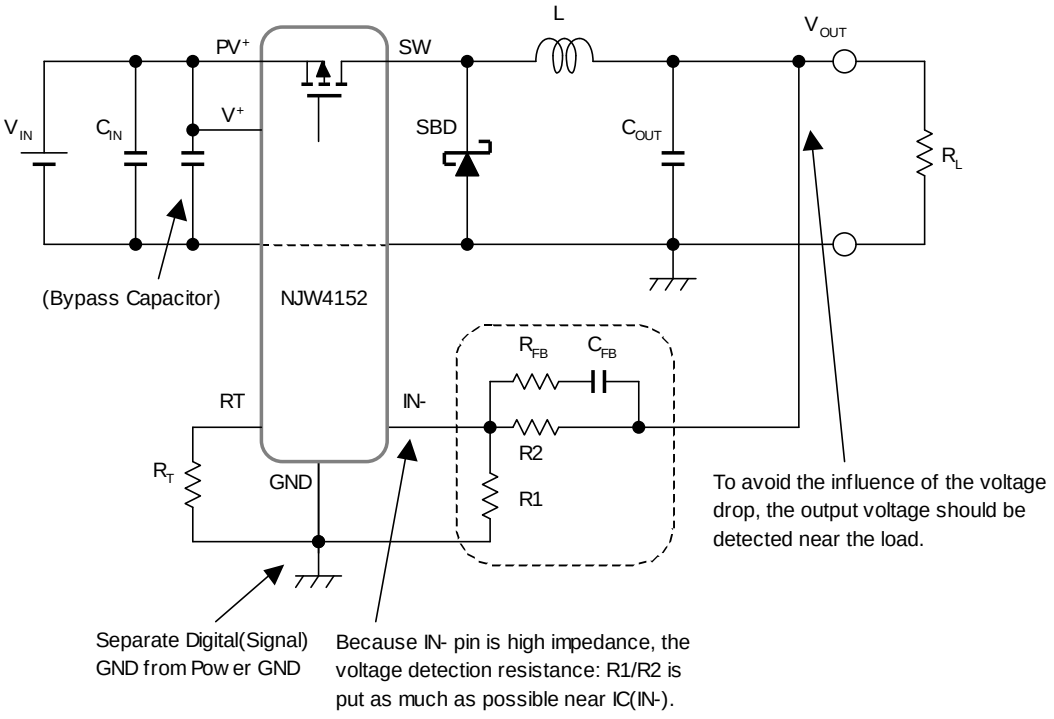
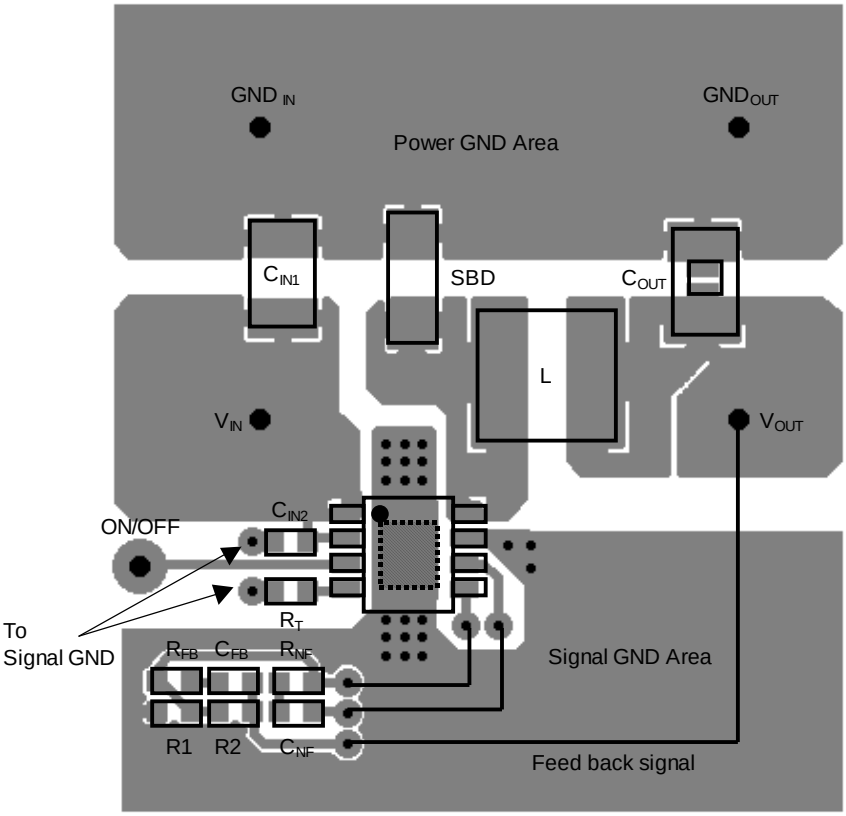


Fig. 6. Board Layout at Buck Converter

■ Application Information (Continued)



Connect Signal GND line and Power GND line on backside pattern

Fig. 7 Layout Example (upper view)

■ Calculation of Package Power

A lot of the power consumption of buck converter occurs from the internal switching element (Power MOSFET). Power consumption of NJW4152 is roughly estimated as follows.

Input Power:	$P_{IN} = V_{IN} \times I_{IN}$ [W]
Output Power:	$P_{OUT} = V_{OUT} \times I_{OUT}$ [W]
Diode Loss:	$P_{DIODE} = V_F \times I_{L(avg)} \times$ OFF duty [W]
NJW4152 Power Consumption:	$P_{LOSS} = P_{IN} - P_{OUT} - P_{DIODE}$ [W]

Where:

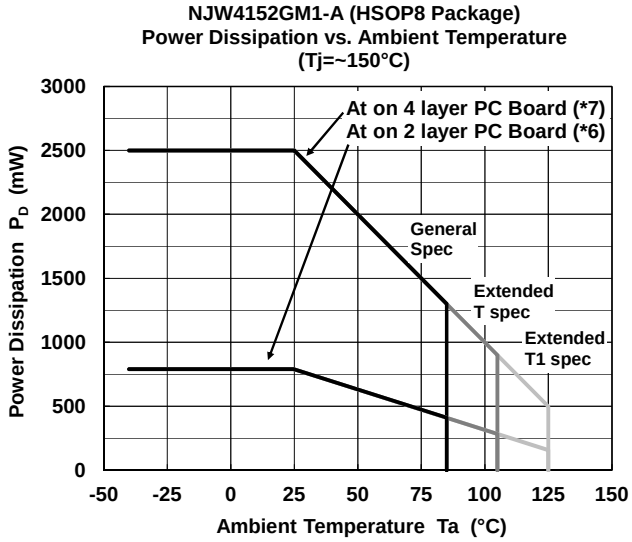
V_{IN}	: Input Voltage for Converter	I_{IN}	: Input Current for Converter
V_{OUT}	: Output Voltage of Converter	I_{OUT}	: Output Current of Converter
V_F	: Diode's Forward Saturation Voltage	$I_{L(avg)}$	: Inductor Average Current
OFF duty	: Switch OFF Duty		

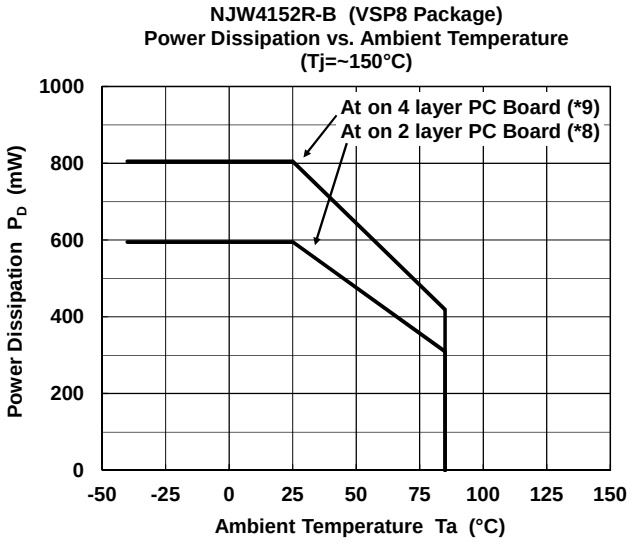
Efficiency (η) is calculated as follows.

$\eta = (P_{OUT} \div P_{IN}) \times 100$ [%]

You should consider temperature derating to the calculated power consumption: P_D.

You should design power consumption in rated range referring to the power dissipation vs. ambient temperature characteristics (Fig. 8).





(*6): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*7): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers)
(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

(*8): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

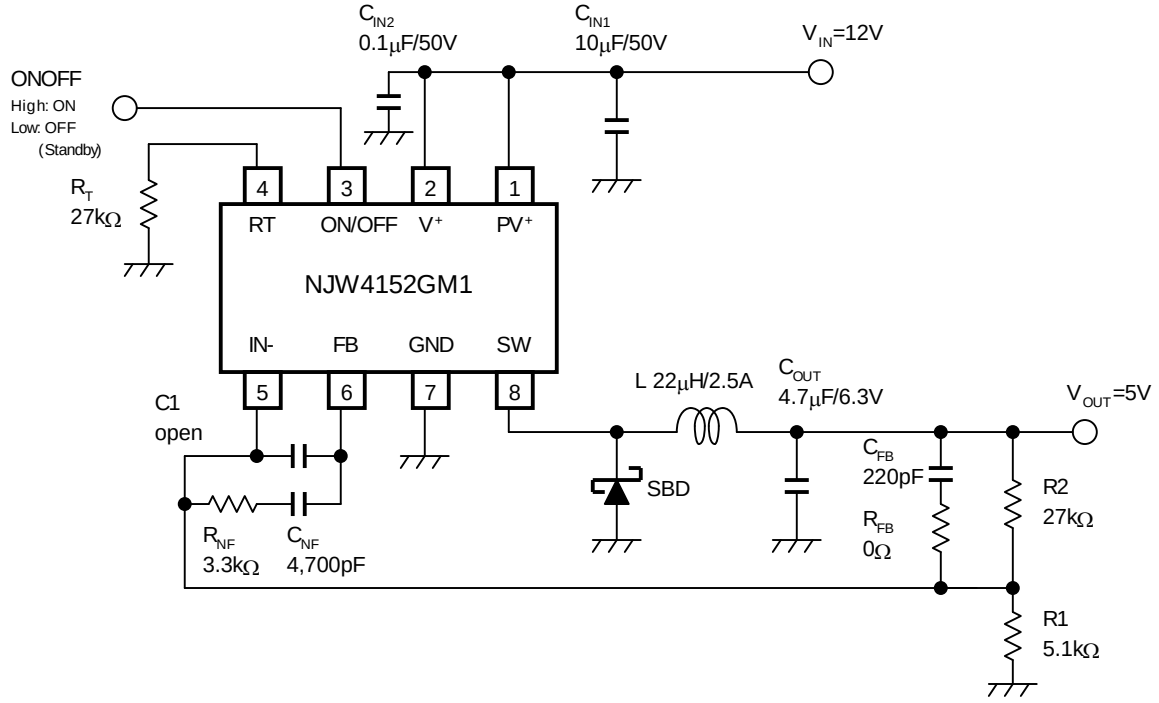
(*9): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers),
internal Cu area: 74.2×74.2mm

Fig. 8. Power Dissipation vs. Ambient Temperature Characteristics

■ Application Design Examples

● Step-Down Application Circuit

IC : NJW4152GM1
Input Voltage : V_{IN}=12V
Output Voltage : V_{OUT}=5V
Output Current : I_{OUT}=1A
Oscillation frequency : fosc=700kHz
Output Ripple Voltage : $V_{ripple(P-P)}$=less than 20mV



Reference	Qty.	Part Number	Description	Manufacturer
IC	1	NJW4152GM1	Internal 1A MOSFET SW.REG. IC	New JRC
L	1	CDRH8D28HPNP-220N	Inductor 22μH, 2.5A(Ta=20°C) / 1.9A (Ta=100°C)	Sumida
D	1	CMS11	Schottky Diode 40V, 2A	Toshiba
C_{IN1}	1	UMK325BJ106MM	Ceramic Capacitor 3225 10μF, 50V, X5R	Taiyo Yuden
C_{IN2}	1	0.1μF	Ceramic Capacitor 1608 0.1μF, 50V, B	Std.
C_{OUT}	1	JMK212ABJ475KG	Ceramic Capacitor 2012 4.7μF, 6.3V, X5R	Taiyo Yuden
C_{NF}	1	4,700pF	Ceramic Capacitor 1608 4,700pF, 50V, B	Std.
C_{FB}	1	220pF	Ceramic Capacitor 1608 220pF, 50V, CH	Std.
C1	0	— (Optional)	Optional	—
R1	1	5.1kΩ	Resistor 1608 5.1kΩ, ±1%, 0.1W	Std.
R2, R_T	2	27kΩ	Resistor 1608 27kΩ, ±1%, 0.1W	Std.
R_{NF}	1	3.3kΩ	Resistor 1608 3.3kΩ, ±5%, 0.1W	Std.
R_{FB}	1	0Ω (Short)	Resistor 1608 0Ω, 0.1W	Std.

■ Application Design Examples (Continued)

● Setting Oscillation Frequency

From the Oscillation frequency vs. Timing Resistor Characteristic, R_T=27 [kΩ], t=1.43[μs] at fosc=700kHz.

Step-down converter duty ratio is shown with the following equation.

$$Duty = \frac{V_{OUT} + V_F}{V_{IN}} \times 100 = \frac{5 + 0.4}{12} \times 100 = 45\,[\%]$$

Therefore, t_{ON}=0.64 [μs], t_{OFF}=0.79 [μs]

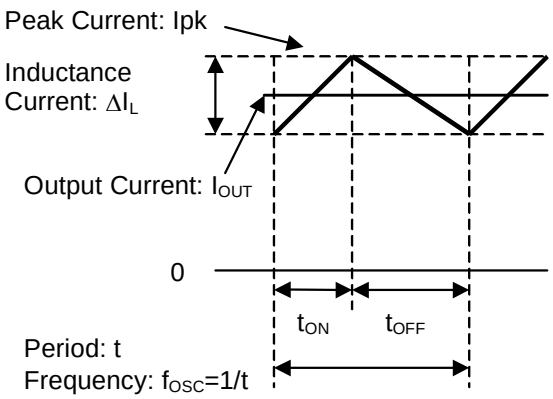


Fig. 9. Inductor Current Waveform

● Selecting Inductance

To assume maximum output current: 1A, and the inductor ripple current should be set not to exceed the minimum switching limiting current: I_{LIM}=1.4A (min.).

ΔIL is Inductance ripple current. When to ΔIL= output current 20%:

$\Delta I_L = 0.2 \times I_{OUT} = 0.2 \times 1 = 0.2$ [A]

This obtains inductance L. V_{DS_RON} is drop voltage by MOSFET on resistance.

$$L = \frac{V_{IN} - V_{DS-RON} - V_{OUT}}{\Delta I_L} \times t_{ON} = \frac{12 - 0.5 - 5}{0.2} \times 0.64\mu = 20.8\,[\mu H] \Rightarrow 22[\mu H]$$

Inductance L is a theoretical value. The optimum value varies according such factors as application specifications and components. Fine-tuning should be done on the actual device.

This obtains the peak current Ipk at switching time.

$$Ipk = I_{OUT} + \frac{\Delta I_L}{2} = 1 + \frac{0.2}{2} = 1.1\,[A]$$

The current that flows into the inductance provides sufficient margin for peak current at switching time.
In the application circuit, use L=22μH, 2.5A(Ta=20°C) / 1.9A (Ta=100°C).

■ Application Design Examples (Continued)

● Selecting the Input Capacitor

The input capacitor corresponds to the input of the power supply. It is required to adequately reduce the impedance of the power supply. The input capacitor selection should be determined by the input ripple current and the maximum input voltage of the capacitor rather than its capacitance value.

The effective input current can be expressed by the following formula.

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} [A]$$

In the above formula, the maximum current is obtained when $V_{IN} = 2 \times V_{OUT}$, and the result in this case is $I_{RMS} = I_{OUT\,(MAX)} \div 2$.

When selecting the input capacitor, carry out an evaluation based on the application, and use a capacitor that has adequate margin.

● Selecting the Output Capacitor

The output capacitor is an important component that determines output ripple noise. Equivalent Series Resistance (ESR), ripple current, and capacitor breakdown voltage are important in determining the output capacitor.

The output ripple noise can be expressed by the following formula.

$$ESR = \frac{V_{ripple(p-p)}}{\Delta I_L}$$

When selecting output capacitance, select a capacitor that allows for sufficient ripple current.

The effective ripple current that flows in a capacitor (I_{rms}) is obtained by the following equation.

$$I_{rms} = \frac{\Delta I_L}{2\sqrt{3}} = \frac{0.2}{2\sqrt{3}} = 58\,[mArms]$$

Consider sufficient margin, and use a capacitor that fulfills the above spec.

In the application circuit, use C_{OUT}=4.7μF/6.3V.

● Setting Output Voltage

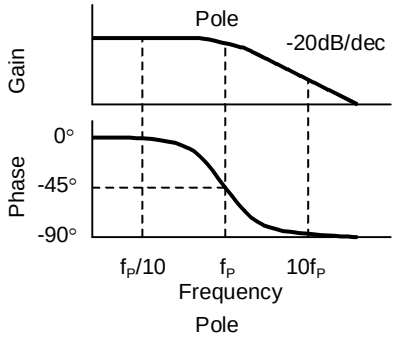
The output voltage V_{OUT} is determined by the relative resistances of R1, R2. The current that flows in R1, R2 must be a value that can ignore the bias current that flows in ER AMP.

$$V_{OUT} = \left(\frac{R2}{R1} + 1\right) \times V_B = \left(\frac{27k}{5.1k} + 1\right) \times 0.8 = 5.04\,[V]$$

■ Compensation design example

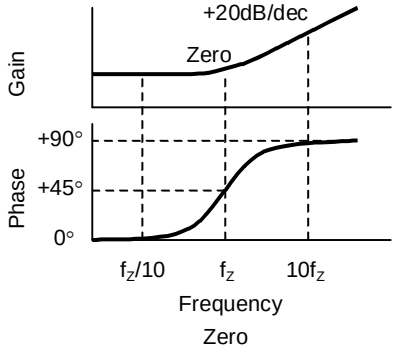
A switching regulator requires a feedback circuit for acquiring a stable output. Because the frequency characteristics of the application change according to the inductance, output capacitor, and so on, the compensation constant should ideally be determined in such a way that the maximum band is acquired while the necessary phase for stable operation is maintained.

These compensation constants play an important role in the adjustment of the NJW4152 when mounted in an actual unit. Finally, select the constants while performing measurement, in consideration of the application specifications.



● Feedback and Stability

Basically, the feedback loop should be designed in such a way that the open loop phase shift at the point where the loop gain is 0 dB is less than -180°. It is also important that the loop characteristics have margin in consideration of ringing and immunity to oscillation during load fluctuations. With the NJW4152, the feedback circuit can be freely designed, enabling the arrangement of the poles and zeros which is important for loop compensation, to be optimized.



The characteristics of the poles and zeros are shown in Fig. 10.
Poles: The gain has a slope of -20 dB/dec, and the phase shifts -90°.
Zeros: The gain has a slope of +20 dB/dec, and the phase shift +90°.

Fig. 10. Characteristics of Pole and Zero

If the number of factors constituting poles is defined as “n”, the change in the gain and phase will be “n”-fold. This also applies to zeros as well. The poles and zeros are in a reciprocal relationship, so if there is one factor for each pole and zero, they will cancel each other.

● Configuration of the compensation circuit

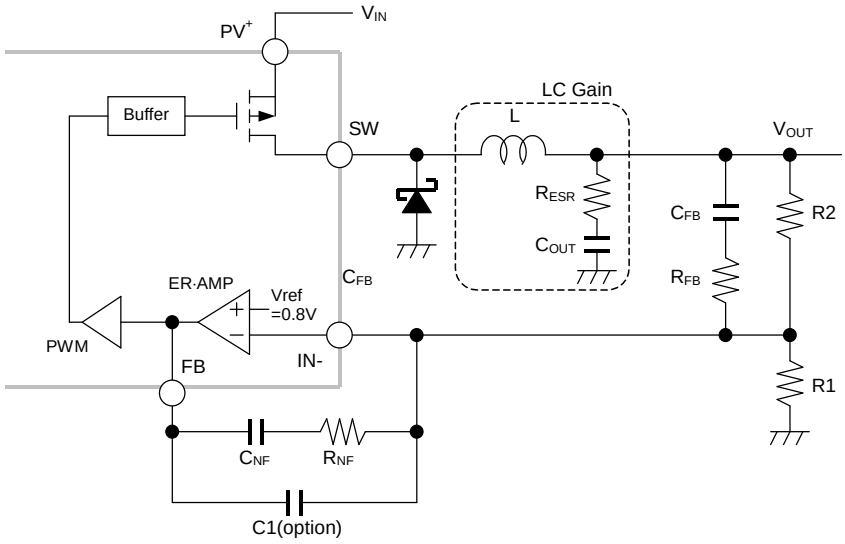


Fig. 11. Compensation Circuit Configuration

■ Compensation Design (Continued)

● Poles and zeros due to the inductance and output capacitor

Double poles $f_{P(LC)}$ are generated by the inductance and output capacitor. Simultaneously, single zeros $f_{Z(ESR)}$ are generated by the output capacitor and ESR. Each pole and zero is expressed by the following formula.

$$f_{Z(ESR)} = \frac{1}{2\pi C_{OUT} R_{ESR}} \qquad f_{P(LC)} = \frac{1}{2\pi\sqrt{LC_{OUT}}}$$

If the ESR of the output capacitor is high, $f_{Z(ESR)}$ will be located in the vicinity of $f_{P(LC)}$. In an application such as this, the zero $f_{Z(ESR)}$ compensates the double poles $f_{P(LC)}$, resulting in a tendency for stability to be readily maintained.

However, if the ESR of the output capacitor is low, $f_{Z(ESR)}$ shifts to the high region, and the phase is shifted -180° by $f_{P(LC)}$.The NJW4152 compensation circuit enables compensation to be realized by using zeros f_{Z1} and f_{Z2}.

● Poles and zeros due to error amplifier

The single poles and zeros generated by the error amplifier are obtained using the following formula.

Zero	Pole
$f_{Z1} = \frac{1}{2\pi C_{NF} R_{NF}}$	$f_{P1} = \frac{1}{2\pi C_{NF} A_V \left(\frac{R1 R2}{R1 + R2} \right)}$ (Av: Amplifier Open Loop Gain=80dB)
$f_{Z2} = \frac{1}{2\pi C_{FB} R2}$	$f_{P2} = \frac{1}{2\pi C_{FB} \left(R_{FB} + \frac{R1 R2}{R1 + R2} \right)}$
	$f_{P3} = \frac{1}{2\pi C1 R_{NF}}$ (Option)

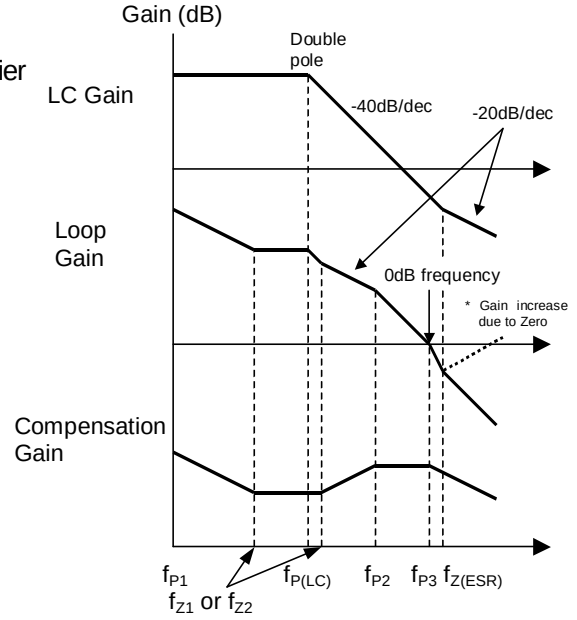


Fig12. Loop Gain examples

f_{Z1} and f_{Z2} are located on both sides of $f_{P(LC)}$.

Because the inductance and output capacitor vary, they are each set using the following as a rough guide.

$f_{P(LC)} \times$ 0.5-fold – 0.9-fold

$f_{P(LC)} \times$ 1.1-fold – 2.0-fold

There is also a method in which f_{Z1} and f_{Z2} are located at positions lower than even $f_{P(LC)}$. Because there is a tendency for the phase shift to increase and the gain to rise, it can be expected that the response will improve.

However, there is a tendency for the phase margin to become insufficient, so care is necessary.

f_{P1} creates poles in the low frequency region due to the Miller effect of the error amplifier. The stability becomes better as f_{P1} becomes lower. On the other hand, the frequency characteristics do not improve, so the response is adversely affected. f_{P1} is set using a frequency gain of 20 dB for $f_{P(LC)}$ as a rough guide.

If the open loop gain of the error amplifier is made 80 dB, design is carried out using $f_{P1} < f_{P(LC)} \div 10^3$ (= 60 dB) as a rough guide.

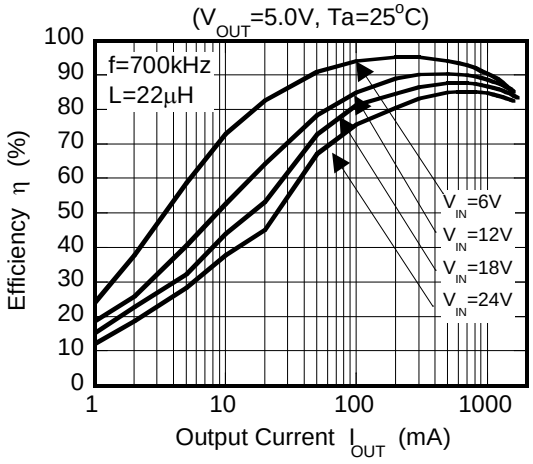
Above several 100 kHz, various poles are generated, so the upper limit of the frequency range where the loop gain is 0 dB is set to fifth (1/5) to tenth (1/10) of oscillation frequency. The $f_{Z(ESR)}$ in the high frequency region sometimes causes a loop gain to be generated (See Fig.12 Loop Gain “). Using f_{P2} and f_{P3}, perform adjustment with the NJW4152 mounted in an actual unit, so as to adequately reduce the loop gain in the high frequency region.

■Application Characteristics :NJW4152GM1-A

● At V_{OUT}=5.0V setting (R1=5.1kΩ, R2=27kΩ, C_{FB}=220pF, R_{FB}=0Ω)

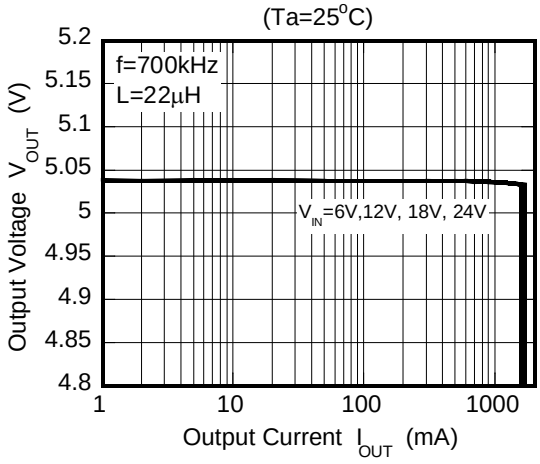
Efficiency vs. Output Current

(V_{OUT}=5.0V, Ta=25°C)



Output Voltage vs. Output Current

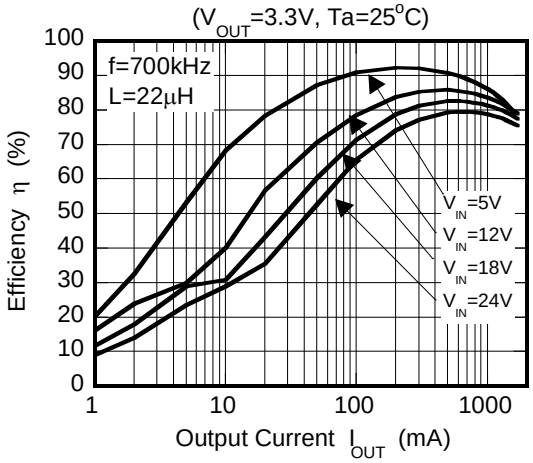
(Ta=25°C)



● At V_{OUT}=3.3V setting (R1=5.1kΩ, R2=16kΩ, C_{FB}=220pF, R_{FB}=0Ω)

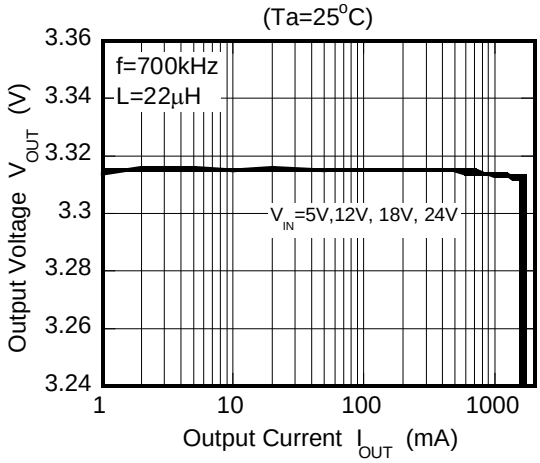
Efficiency vs. Output Current

(V_{OUT}=3.3V, Ta=25°C)



Output Voltage vs. Output Current

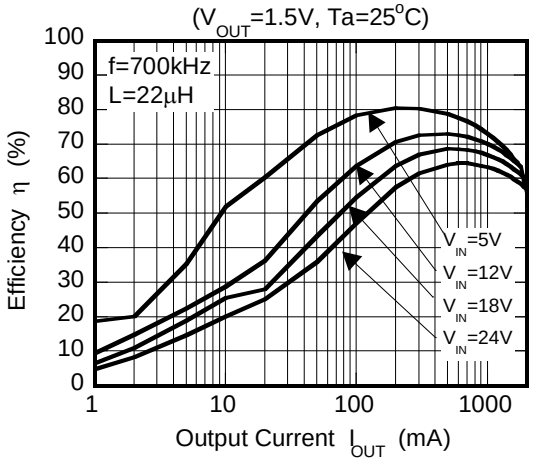
(Ta=25°C)



● At V_{OUT}=1.5V setting (R1=30kΩ, R2=27kΩ, C_{FB}=220pF, R_{FB}=10kΩ)

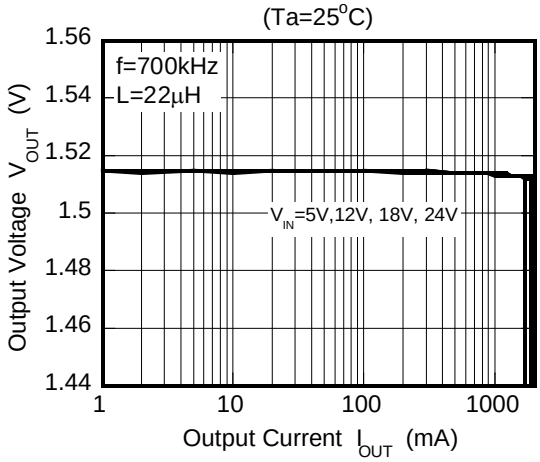
Efficiency vs. Output Current

(V_{OUT}=1.5V, Ta=25°C)



Output Voltage vs. Output Current

(Ta=25°C)



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