FAIRCHILD SEMICONDUCTOR®

March 2000
Revised June 2005

FST162861
20-Bit Bus Switch with 25Ω Series Resistors in Outputs

General Description

The Fairchild Switch FST162861 provides 20-bits of high-speed CMOS TTL-compatible bus switching. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as a 10-bit or 20-bit bus switch. When $\overline{OE}_1$ is LOW, the switch is ON and Port 1A is connected to Port 1B. When $\overline{OE}_2$ is LOW, Port 2A is connected to Port 2B. When $\overline{OE}_X$ is HIGH, a high impedance state exists between the A and B ports. The FST162861 has an equivalent 25Ω series resistors to reduce signal-reflection noise, eliminating the need for external terminating resistors.

Features

- 25Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

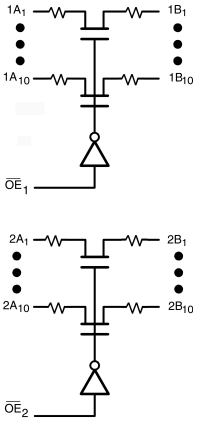
Ordering Code:

Order Number	Package Number	Package Description
FST162861MTD (Note 1)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
FST162861MTDX_NL (Note 2)	MTD48	Pb-Free 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

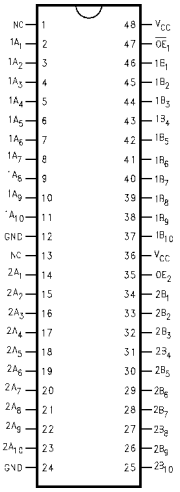
Note 1: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Note 2: "_NL" indicates Pb-Free product (per JEDEC J-STD-020B). Device is available in Tape and Reel only.

Logic Diagram



Connection Diagram



Truth Table

Inputs		Inputs/Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

Pin Descriptions

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B

Absolute Maximum Ratings(Note 3)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S) (Note 4)	−0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 5)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN} < 0V	−50mA
DC Output (I_{OUT}) Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	±100mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 6)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	-40 °C to +85 °C

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: V_S is the voltage observed/applied at either the A or B Port across the switch.

Note 5: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 6: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 7)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0 ≤ V_{IN} ≤ 5.5V
		0			±1.0	µA	V_{IN} = 5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ A, B ≤ V_{CC}
R_{ON}	Switch ON Resistance (Note 8)	4.5	20	26	38	Ω	V_{IN} = 0V, I_{IN} = 64mA
		4.5	20	27	40	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5	20	28	48	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0	20	30	48	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 7: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 8: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\,^\circ C$ to $+85\,^\circ C$, $C_L = 50$ pF, RU = RD = 500Ω				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 9)		1.25		1.25	ns	V_I = OPEN	Figures 1, 2
t_{PZH}, t_{PZL}	Output Enable Time	1.0	5.3		5.5	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figures 1, 2
t_{PHZ}, t_{PLZ}	Output Disable Time	1.0	6.0		6.3	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figures 1, 2

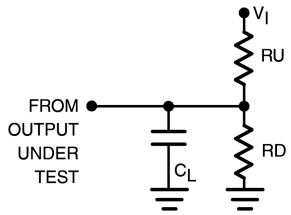
Note 9: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 10)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3.5		pF	V_{CC} = 5.0V, V_{IN} = 0V
$C_{I/O}$	Input/Output Capacitance "OFF State"	6.0		pF	V_{CC}, $\overline{OE}$ = 5.0V, V_{IN} = 0V

Note 10: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

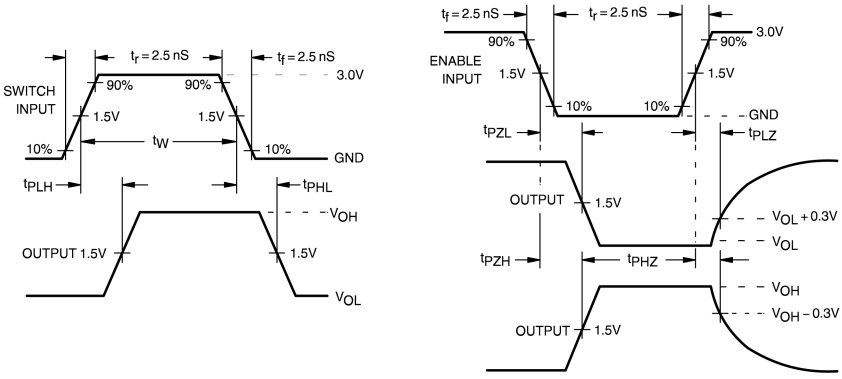
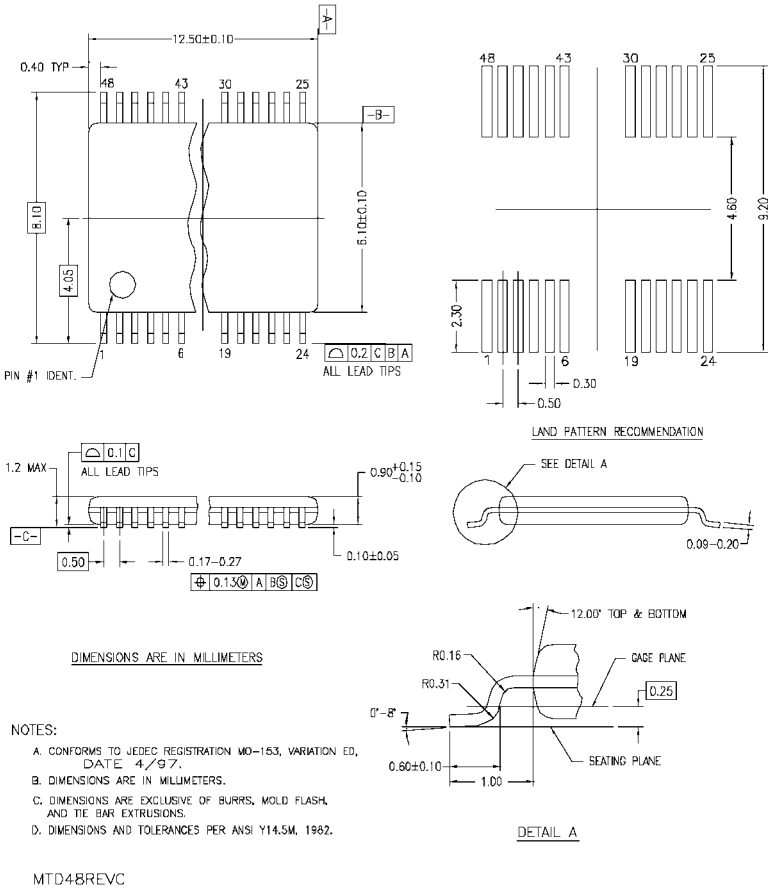


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384(FST3384) bus switch product.

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com