PCA9306-Q1 Dual Bidirectional I^2C Bus and SMBus Voltage-Level Translator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 2: –40°C to 105°C
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- 2-Bit Bidirectional Translator for SDA and SCL Lines in Mixed-Mode I^2C Applications
- Compatible With I^2C and SMBus
- Less Than 1.5-ns Maximum Propagation Delay to Accommodate Standard-Mode and Fast-Mode I^2C Devices and Multiple Masters
- Allows Voltage-Level Translation Between
  - 1.2-V V_{REF1} and 1.8-V, 2.5-V, 3.3-V, or 5-V V_{REF2}
  - 1.8-V V_{REF1} and 2.5-V, 3.3-V, or 5-V V_{REF2}
  - 2.5-V V_{REF1} and 3.3-V, or 5-V V_{REF2}
  - 3.3-V V_{REF1} and 5-V V_{REF2}
- Provides Bidirectional Voltage Translation With No Direction Pin
- Low 3.5-Ω ON-State Connection Between Input and Output Ports Provides Less Signal Distortion
- Open-Drain I^2C I/O Ports (SCL1, SDA1, SCL2, and SDA2)
- 5-V Tolerant I^2C I/O Ports to Support Mixed-Mode Signal Operation
- High-Impedance SCL1, SDA1, SCL2, and SDA2 Pins for EN = Low
- Lock-Up-Free Operation for Isolation When EN = Low
- Flow-Through Pinout for Ease of Printed-Circuit Board Trace Routing
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- I^2C, SMBus, PMBus, MDIO, UART, Low-Speed SDIO, GPIO, and Other Two-Signal Interfaces
- Automotive Head Units
- Automotive Instrument Clusters
- Automotive Driver Assistance Cameras

3 Description

This dual bidirectional I^2C and SMBus voltage-level translator, with an enable (EN) input, is operational from 1.2-V to 3.3-V V_{REF1} and 1.8-V to 5.5-V V_{REF2}.

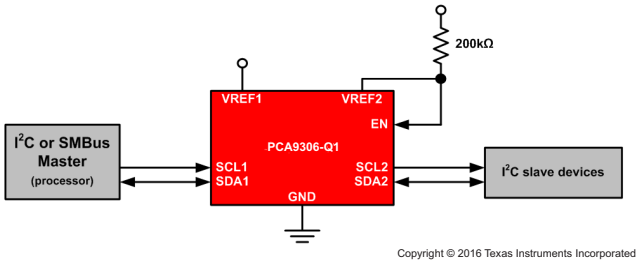
The PCA9306-Q1 allows bidirectional voltage translations between 1.2 V and 5 V, without the use of a direction pin. The low ON-state resistance (r_{on}) of the switch allows connections to be made with minimal propagation delay. When EN is high, the translator switch is ON, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is low, the translator switch is off, and a high-impedance state exists between ports.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCA9306-Q1	VSSOP (8)	2.30 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2013) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Description (continued)

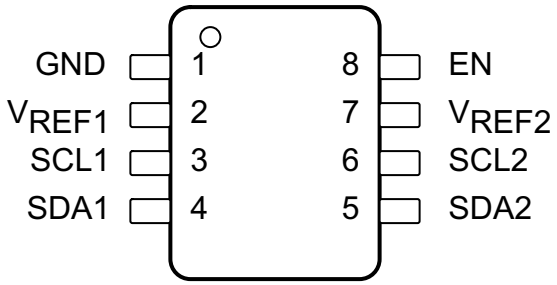
In I^2C applications, the bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9306-Q1 enables the system designer to isolate two halves of a bus; thus, more I^2C devices or longer trace length can be accommodated.

The PCA9306-Q1 also can be used to run two buses, one at 400-kHz operating frequency and the other at 100-kHz operating frequency. If the two buses are operating at different frequencies, the 100-kHz bus must be isolated when the 400-kHz operation of the other bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater.

All channels have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, because the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower-voltage devices and at the same time protects less ESD-resistant devices.

6 Pin Configuration and Functions

DCU Package
8-Pin VSSOP
Top View



Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	GND	Ground, 0 V
2	V_{REF1}	Low-voltage-side reference supply voltage for SCL1 and SDA1
3	SCL1	Serial clock, low-voltage side. Connect to V_{REF1} through a pullup resistor.
4	SDA1	Serial data, low-voltage side. Connect to V_{REF1} through a pullup resistor.
5	SDA2	Serial data, high-voltage side. Connect to V_{REF2} through a pullup resistor.
6	SCL2	Serial clock, high-voltage side. Connect to V_{REF2} through a pullup resistor.
7	V_{REF2}	High-voltage-side reference supply voltage for SCL2 and SDA2
8	EN	Switch enable input. Connected to V_{REF2} and pulled up through a high resistor.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{REF1}	DC reference voltage		–0.5	7	V
V_{REF2}	DC reference bias voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
$V_{I/O}$	Input/output voltage(2)		–0.5	7	V
	Continuous channel current			128	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
θ_{JA}	Package thermal impedance			227	°C/W
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and input/output negative voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	SCL1, SDA1, SCL2, SDA2	0	5	V
V_{REF1}	Reference voltage		0	5	V
V_{REF2}	Reference voltage		0	5	V
EN	Enable input voltage		0	5	V
I_{PASS}	Pass switch current			64	mA
T_A	Operating free-air temperature		–40	105	°C

7.4 Thermal Information

THERMAL METRIC(1)		PCA9306-Q1 DCU (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$(2)	Junction-to-ambient thermal resistance	227	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA,	EN = 0 V				–1.2	V
I_{IH}	Input leakage current		V_I = 5 V,	EN = 0 V				5	µA
C_i(EN)	Input capacitance		V_I = 3 V or 0 V				11		pF
$C_{io(off)}$	Off capacitance	SCLn, SDAn	V_O = 3 V or 0 V,	EN = 0 V			4	6	pF
$C_{io(on)}$	On capacitance	SCLn, SDAn	V_O = 3 V or 0 V,	EN = 3 V			10.5	12.5	pF
r_{on} (2)	ON-state resistance	SCLn, SDAn	V_I = 0 V,	I_O = 64 mA	EN = 4.5 V		3.5	5.5	Ω
					EN = 3 V		4.7	7	
					EN = 2.3 V		6.3	9.5	
					EN = 1.5 V		25.5	32	
			V_I = 2.4 V,	I_O = 15 mA	EN = 4.5 V	1	6	15	
					EN = 3 V	20	60	140	
			V_I = 1.7 V,	I_O = 15 mA	EN = 2.3 V	20	60	140	

(1) All typical values are at T_A = 25°C.
(2) Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals, at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

7.6 Switching Characteristics: Translating Down, V_{IH} = 3.3 V

over recommended operating free-air temperature range, EN = 3.3 V, V_{IH} = 3.3 V, V_{IL} = 0, and V_M = 1.15 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	C_L = 50 pF		0.8	ns
			C_L = 30 pF		0.6	
			C_L = 15 pF		0.3	
t_{PHL}	SCL2 or SDA2	SCL1 or SDA1	C_L = 50 pF		1.2	ns
			C_L = 30 pF		1	
			C_L = 15 pF		0.5	

7.7 Switching Characteristics: Translating Down, V_{IH} = 2.5 V

over recommended operating free-air temperature range, EN = 2.5 V, V_{IH} = 2.5 V, V_{IL} = 0, and V_M = 0.75 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	C_L = 50 pF		1	ns
			C_L = 30 pF		0.7	
			C_L = 15 pF		0.4	
t_{PHL}	SCL2 or SDA2	SCL1 or SDA1	C_L = 50 pF		1.3	ns
			C_L = 30 pF		1	
			C_L = 15 pF		0.6	

7.8 Switching Characteristics: Translating Up, V_{IH} = 2.3 V

over recommended operating free-air temperature range, EN = 3.3 V, V_{IH} = 2.3 V, V_{IL} = 0, V_T = 3.3 V, V_M = 1.15 V, and R_L = 300 Ω (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	SCL1 or SDA1	SCL2 or SDA2	C_L = 50 pF		0.9	ns
			C_L = 30 pF		0.6	
			C_L = 15 pF		0.4	
t_{PHL}	SCL1 or SDA1	SCL2 or SDA2	C_L = 50 pF		1.4	ns
			C_L = 30 pF		1.1	
			C_L = 15 pF		0.7	

7.9 Switching Characteristics: Translating Up, V_{IH} = 1.5 V

over recommended operating free-air temperature range, EN = 2.5 V, V_{IH} = 1.5 V, V_{IL} = 0, V_T = 2.5 V, V_M = 0.75 V, and R_L = 300 Ω (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	SCL1 or SDA1	SCL2 or SDA2	C_L = 50 pF		1	ns
			C_L = 30 pF		0.6	
			C_L = 15 pF		0.4	
t_{PHL}	SCL1 or SDA1	SCL2 or SDA2	C_L = 50 pF		1.3	
			C_L = 30 pF		1.3	
			C_L = 15 pF		0.8	

7.10 Typical Characteristics

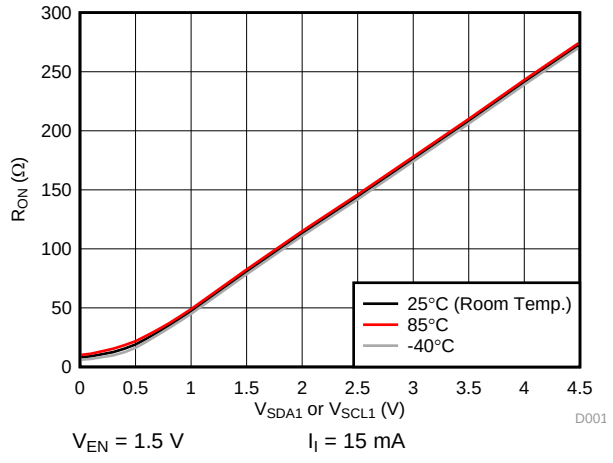


Figure 1. ON-Resistance (R_{ON}) vs Input Voltage (V_{SDA1} or V_{SCL1})

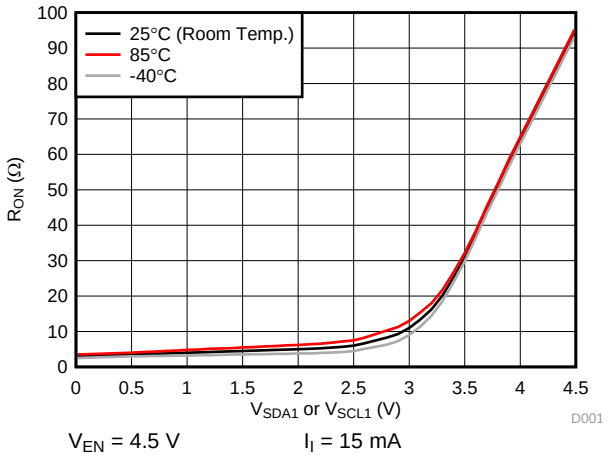
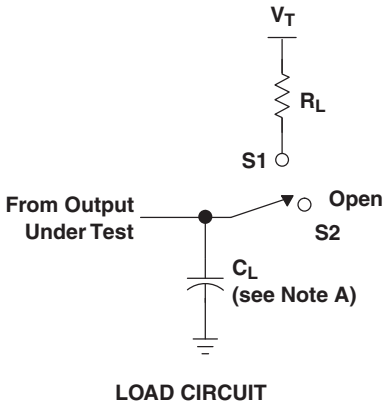
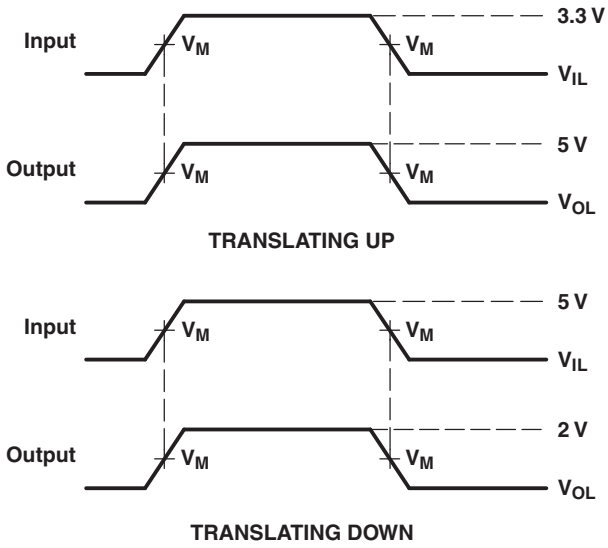


Figure 2. ON-Resistance (R_{ON}) vs Input Voltage (V_{SDA1} or V_{SCL1})

8 Parameter Measurement Information



USAGE	SWITCH
Translating up	S1
Translating down	S2



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 3. Load Circuit for Outputs

9 Detailed Description

9.1 Overview

The PCA9306-Q1 is a dual bidirectional I^2C and SMBus voltage-level translator with an enable (EN) input that operates without the use of a direction pin. The voltage supply range for VREF1 is 1.2 V to 3.3 V and the supply range for VREF2 is 1.8 V to 5.5 V.

The PCA9306-Q1 can also be used to run two buses, one at a 400-kHz operating frequency and the other at a 100-kHz operating frequency. If the two buses are operating at different frequencies, the 100-kHz bus must be isolated by using the EN pin when the 400-kHz operation of the main bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater.

In I^2C applications, the bus capacitance limit of 400 pF restricts the number of devices and bus length. The capacitive load on both sides of the PCA9306-Q1 must be considered when approximating the total load of the system, ensuring the sum of both sides is under 400 pF.

Both the SDA and SCL channels of the PCA9306-Q1 have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This characteristic is a benefit over discrete transistor voltage translation solutions, because the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower-voltage devices and at the same time protects less ESD-resistant devices.

9.2 Functional Block Diagram

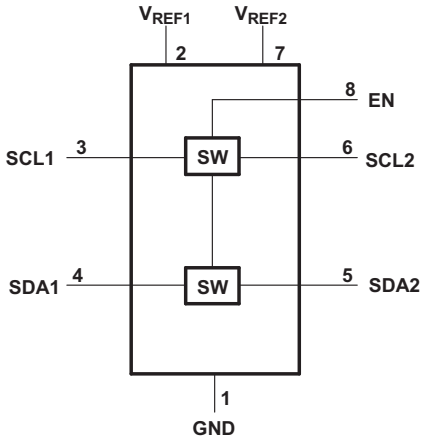


Figure 4. Logic Diagram (Positive Logic)

9.3 Feature Description

9.3.1 Enable (EN) Pin

The PCA9306-Q1 is a double-pole, single-throw switch in which the gate of the transistors is controlled by the voltage on the EN pin. In Figure 5, the PCA9306-Q1 always remains enabled when power is applied to VREF2. Figure 5, the device becomes enabled when a control signal from a processor is in a logic high state. In another variation, the EN pin can be controlled by the output of a processor, but VREF2 can be connected to a power supply through a 200-kΩ resistor. In this case, VREF2 and EN are not to be tied together and the SCL and SDA switches are in a high impedance state when EN is in a logic-low state, as shown in the *Device Functional Modes* section.

9.3.2 Voltage Translation

The primary feature of the PCA9306-Q1 is translating voltage from an I^2C bus referenced to VREF1 up to an I^2C bus referenced to VDPU, to which VREF2 is connected through a 200-kΩ pullup resistor. When translating a standard, open-drain I^2C bus, this is achieved by simply connecting pullup resistors from SCL1 and SDA1 to VREF1 and connecting pullup resistors from SCL2 and SDA2 to VDPU. Find more information on sizing the pullup resistors in the *Sizing Pullup Resistor* section.

9.4 Device Functional Modes

Table 1 describes the two functions of the translation device.

Table 1. Function Table

INPUT EN(1)	TRANSLATOR FUNCTION
H	SCL1 = SCL2, SDA1 = SDA2
L	Disconnect

(1) EN is controlled by the V_{REF2} logic levels and must be at least 1 V higher than V_{REF1} for best translator operation.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 General Applications of I^2C

As with the standard I^2C system, pullup resistors are required to provide the logic-high levels on the translator bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode I^2C devices, in addition to SMBus devices. Standard-mode I^2C devices only specify 3 mA in a generic I^2C system where standard-mode devices and multiple masters are possible. Under certain conditions, high termination currents can be used. When the SDA1 or SDA2 port is low, the clamp is in the ON state, and a low-resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by V_{REF1}. When the SDA1 port is high, the SDA2 port is pulled to the pullup supply voltage of the drain (V_{DPU}) by the pullup resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1-SCL2 channel also functions in the same way as the SDA1-SDA2 channel.

10.2 Typical Application

Figure 5 and Figure 6 show how these pullup resistors are connected in a typical application, as well as two options for connecting the EN pin.

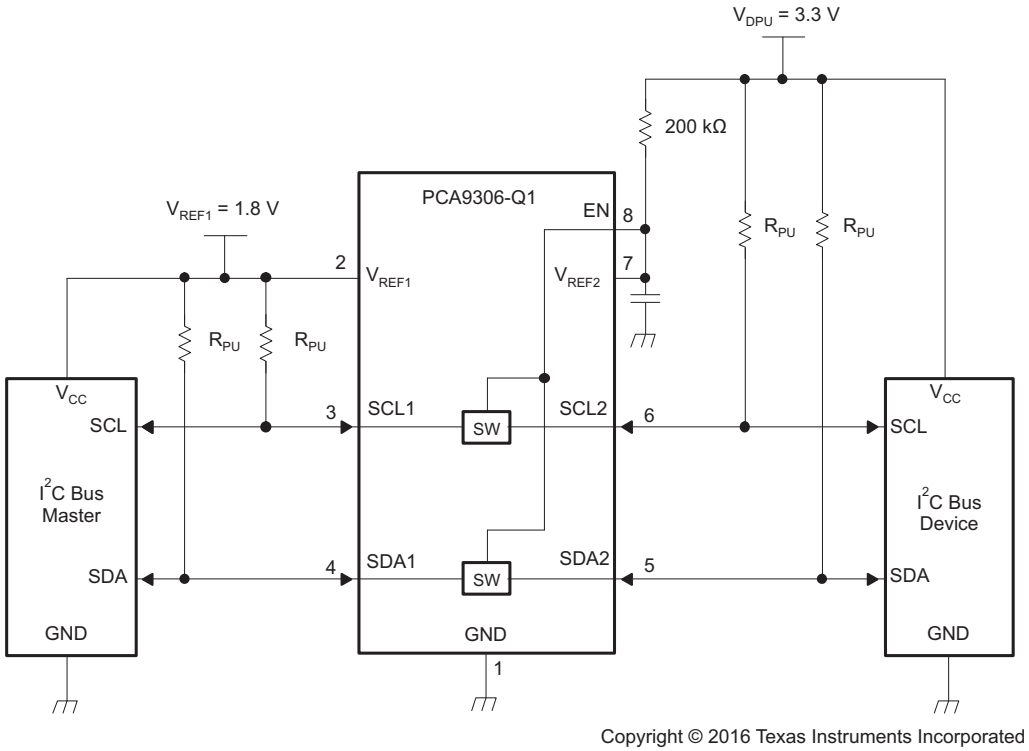


Figure 5. Typical Application Circuit (Switch Always Enabled) Diagram

Typical Application (continued)

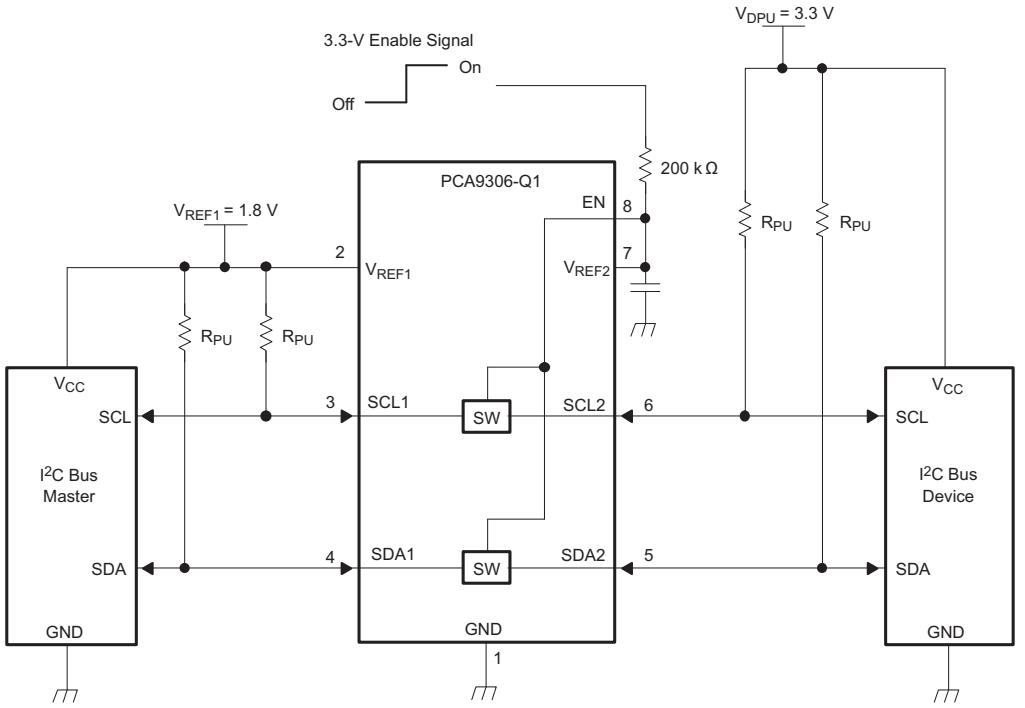


Figure 6. Typical Application Circuit (Switch Enable Control) Diagram

10.2.1 Design Requirements

Table 2 lists the design parameters for this example.

Table 2. Design Parameters

		MIN	TYP(1)	MAX	UNIT
V_{REF2}	Reference voltage	V_{REF1} + 0.6	2.1	5	V
EN	Enable input voltage	V_{REF1} + 0.6	2.1	5	V
V_{REF1}	Reference voltage	0	1.5	4.4	V
I_{PASS}	Pass switch current		14		mA
I_{REF}	Reference-transistor current		5		µA
T_A	Operating free-air temperature	–40		85	°C

(1) All typical values are at T_A = 25°C.

10.2.2 Detailed Design Procedure

10.2.2.1 Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{REF2} and both pins pulled to high-side V_{DPU} through a pullup resistor (typically 200 kΩ). This allows V_{REF2} to regulate the EN input. A filter capacitor on V_{REF2} is recommended. The I^2C bus master output can be totem-pole or open-drain (pullup resistors may be required) and the I^2C bus device output can be totem-pole or open-drain (pullup resistors are required to pull the SCL2 and SDA2 outputs to V_{DPU}). However, if either output is totem-pole, data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction. If both outputs are open-drain, no direction control is needed.

The reference supply voltage (V_{REF1}) is connected to the processor core power-supply voltage.

10.2.2.2 Sizing Pullup Resistor

The pullup resistor value must limit the current through the pass transistor, when it is in the ON state, to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15 mA, the pullup resistor value is calculated as:

$$R_{PU} = \frac{V_{DPU} - 0.35\ V}{0.015\ A} \quad (1)$$

Table 3 summarizes resistor values, reference voltages, and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) must be used to ensure that the pass voltage of the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the PCA9306-Q1 device at 0.175 V, although the 15 mA applies only to current flowing through the PCA9306-Q1 device.

Table 3. Pullup Resistor Values (1) (2)

PULLUP RESISTOR VALUE (Ω)						
V_{DPU}	15 mA		10 mA		3 mA	
	NOMINAL	+10% (3)	NOMINAL	+10% (3)	NOMINAL	+10% (3)
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) Calculated for V_{OL} = 0.35 V
(2) Assumes output driver V_{OL} = 0.175 V at stated current
(3) +10% to compensate for V_{DD} range and resistor tolerance

10.2.2.3 PCA9306-Q1 Bandwidth

The maximum frequency of the PCA9306-Q1 device depends on the application. The device can operate at speeds of > 100 MHz given the correct conditions. The maximum frequency is dependent upon the loading of the application. The PCA9306-Q1 device behaves like a standard switch where the bandwidth of the device is dictated by the ON-resistance and ON-capacitance of the device.

Figure 9 shows a bandwidth measurement of the PCA9306-Q1 device using a two-port network analyzer.

The 3-dB point of the PCA9306-Q1 device is approximately 600 MHz. However, this is an analog type of measurement. For digital applications, the signal must not degrade up to the fifth harmonic of the digital signal. As a rule of thumb, the frequency bandwidth must be at least five times the maximum digital clock rate. This component of the signal is very important in determining the overall shape of the digital signal. In the case of the PCA9306-Q1 device, digital clock frequency of > 100 MHz can be achieved.

The PCA9306-Q1 device does not provide any drive capability like the PCA9515 or PCA9517 series of devices. Therefore, higher-frequency applications require higher drive strength from the host side. No pullup resistor is needed on the host side (3.3 V) if the PCA9306-Q1 device is being driven by standard CMOS push-pull output driver. Ideally, it is best to minimize the trace length from the PCA9306-Q1 device on the sink side (1.8 V) to minimize signal degradation.

You can then use a simple formula to compute the maximum *practical* frequency component or the *knee* frequency (f_{knee}). All fast edges have an infinite spectrum of frequency components. However, there is an inflection (or *knee*) in the frequency spectrum of fast edges where frequency components higher than f_{knee} are insignificant in determining the shape of the signal.

To calculate f_{knee}:

f_{knee}= 0.5 / RT (10–90%)

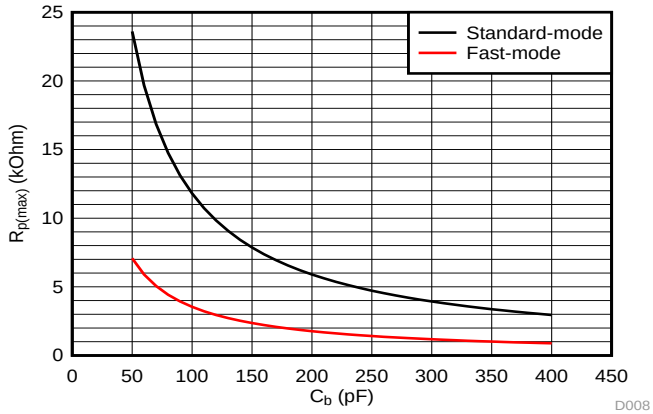
f_{knee} = 0.4 / RT (20–80%)

For signals with rise-time characteristics based on 10- to 90-percent thresholds, f_{knee} is equal to 0.5 divided by the rise time of the signal. For signals with rise-time characteristics based on 20- to 80-percent thresholds, which is very common in many current device specifications, f_{knee} is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that help maximize the performance of the device:

- Keep trace length to a minimum by placing the PCA9306-Q1 device close to the I^2C output of the processor.
- The trace length must be less than half the time of flight to reduce ringing and line reflections or non-monotonic behavior in the switching region.
- To reduce overshoots, a pullup resistor can be added on the 1.8-V side; be aware that a slower fall time is to be expected.

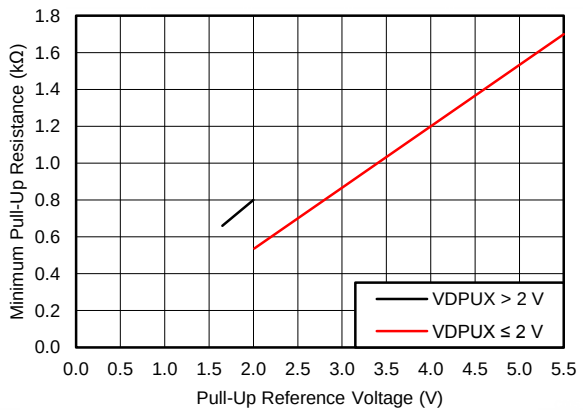
10.2.3 Application Curves



Standard mode (f_{SCL} = 100 kHz, t_r = 1 µs)

Fast mode (f_{SCL} = 400 kHz, t_r = 300 ns)

Figure 7. Maximum Pullup Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2 × V_{DPUX} , I_{OL} = 2 mA when V_{DPUX} ≤ 2 V

V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{DPUX} > 2 V

Figure 8. Minimum Pullup Resistance ($R_{p(min)}$) vs Pullup Reference Voltage (V_{DPUX})

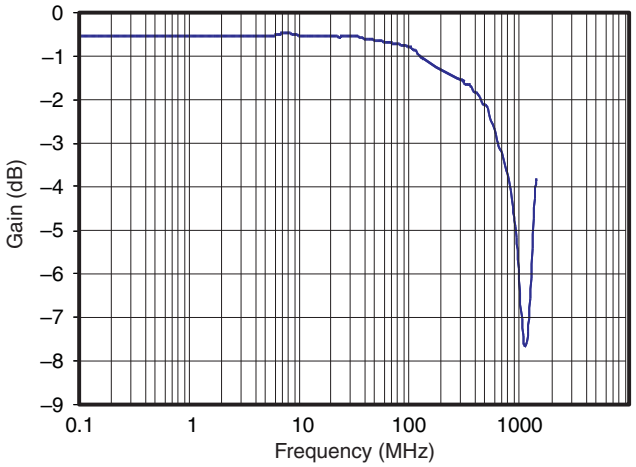


Figure 9. Bandwidth

11 Power Supply Recommendations

For supplying power to the PCA9306-Q1, the VREF1 pin can be connected directly to a power supply. The VREF2 pin must be connected to the VDPU power supply through a 200-kΩ resistor. Failure to have a high impedance resistor between VREF2 and VDPU results in excessive current draw and unreliable device operation.

12 Layout

12.1 Layout Guidelines

For printed-circuit board (PCB) layout of the PCA9306-Q1, common PCB layout practices must be followed; however, additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. The 100-pF filter capacitor must be placed as close to V_{REF2} as possible. A larger decoupling capacitor can also be used, but a longer time constant of two capacitors and the 200-kΩ resistor results in longer turnon and turnoff times for the PCA9306-Q1 device. These best practices are shown in Figure 10.

For the layout example provided in Figure 10, it would be possible to fabricate a PCB with only two layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a four-layer board is preferable for boards with higher-density signal routing. On a four-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface-mount component pad, which must attach to V_{CC} or GND, and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace must be routed to the opposite side of the board, but this technique is not demonstrated in Figure 10.

12.2 Layout Example

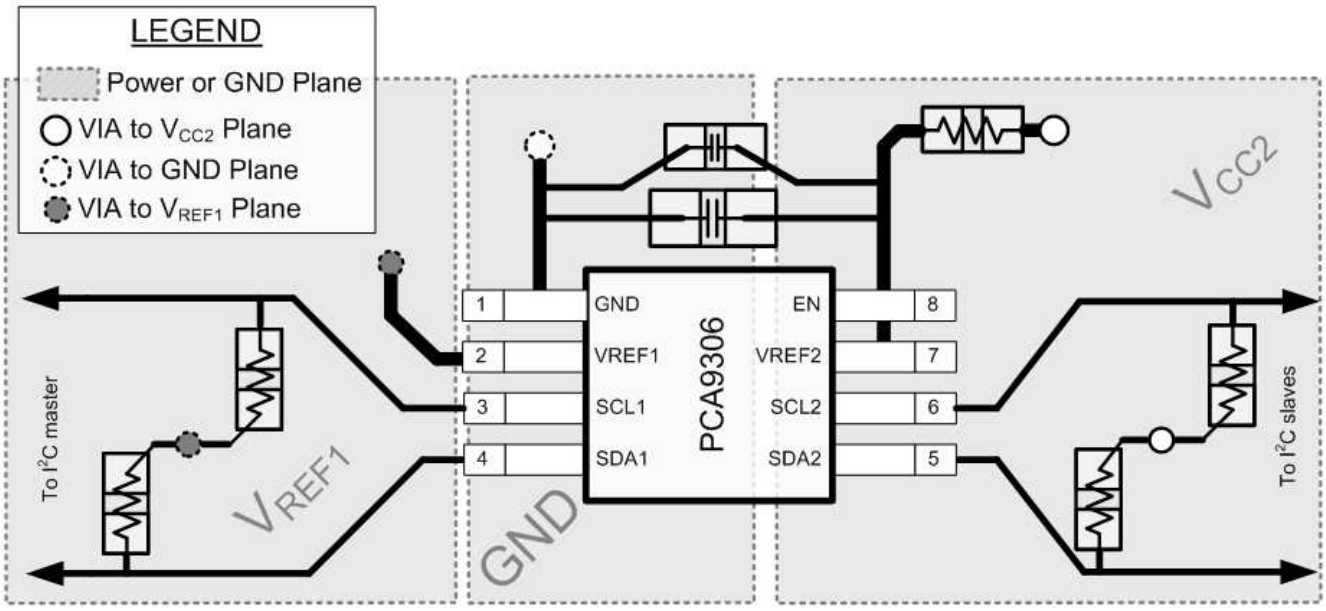


Figure 10. PCA9306-Q1 Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

Technical Documents – http://www.ti.com/product/PCA9306-Q1/technicaldocuments

13.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9306IDCURQ1	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	CCUS	Samples
PCA9306TDCURQ1	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	YAAS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF PCA9306-Q1 :

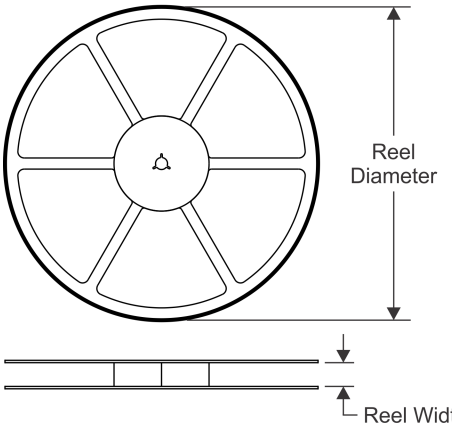
- Catalog: PCA9306

NOTE: Qualified Version Definitions:

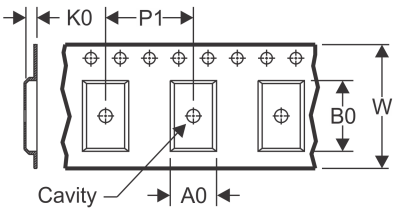
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

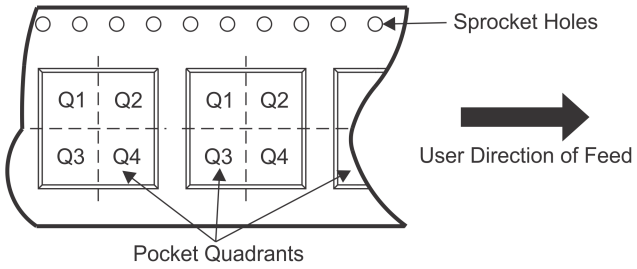


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

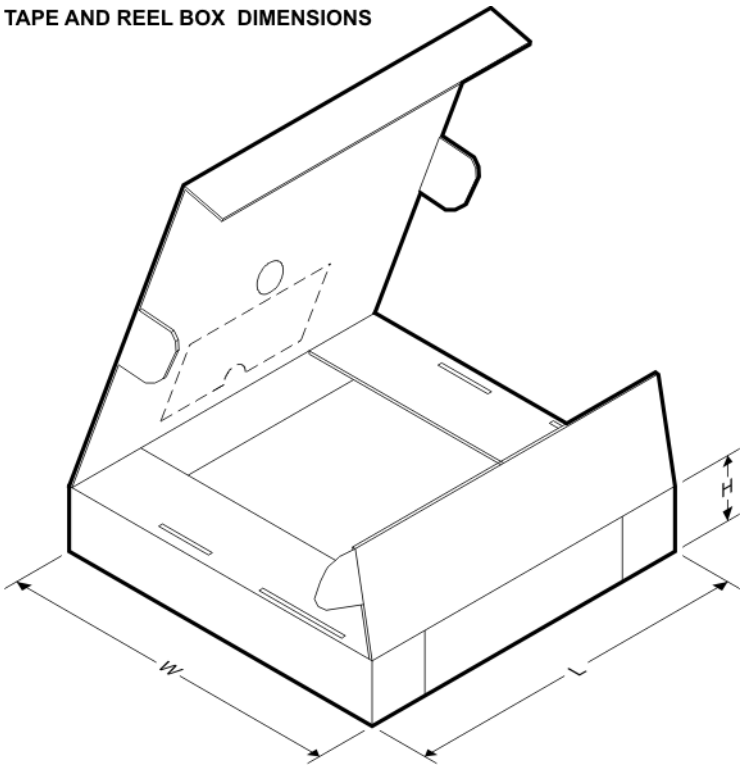
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9306IDCURQ1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
PCA9306TDCURQ1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

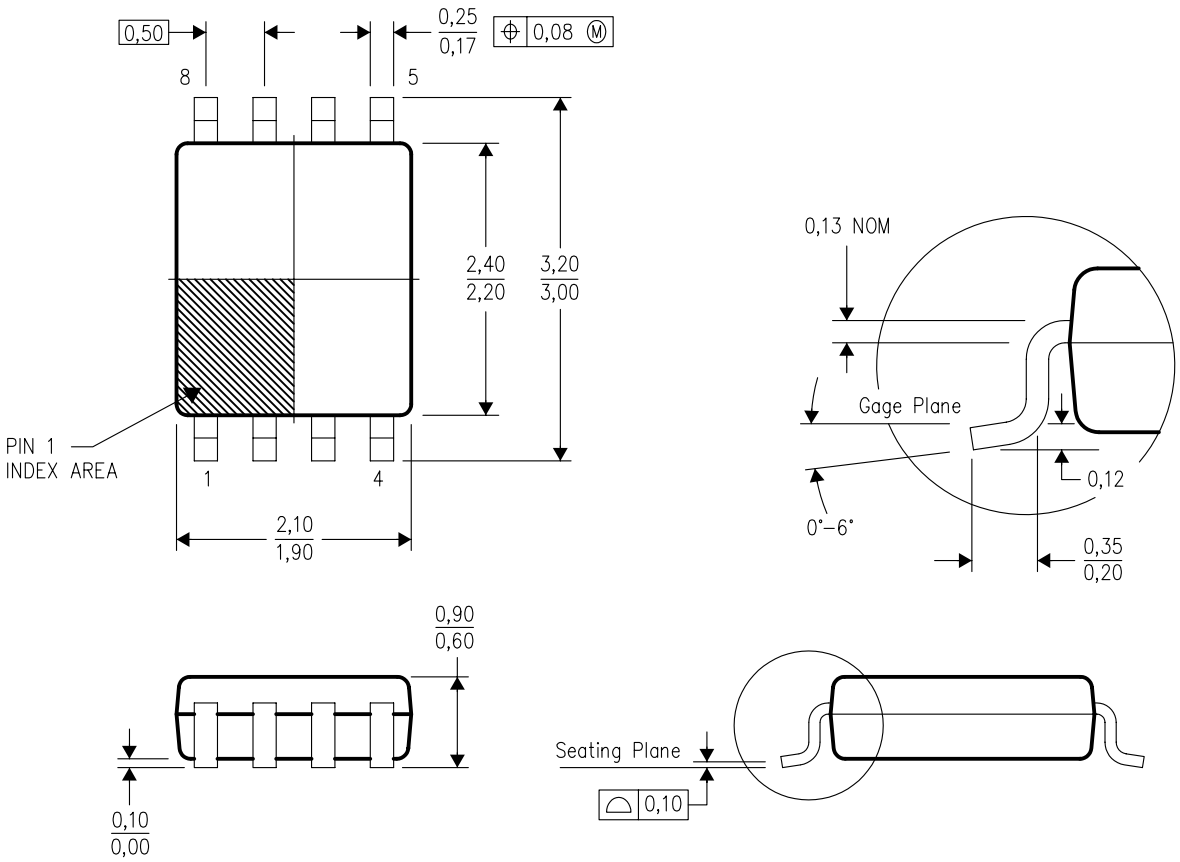
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9306IDCURQ1	VSSOP	DCU	8	3000	202.0	201.0	28.0
PCA9306TDCURQ1	VSSOP	DCU	8	3000	202.0	201.0	28.0

DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

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