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Kind regards,

Team Nexperia



# PMPB40SNA

60 V N-channel Trench MOSFET

29 October 2013

Product data sheet

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction
- Tin-plated 100 % solderable side pads for optical solder inspection
- AEC-Q101 qualified

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$	-	-	60	V
$V_{GS}$	gate-source voltage		-20	-	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{sp} = 25\text{ }^\circ\text{C}$	-	-	12.9	A
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 4.8\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	34	43	m $\Omega$

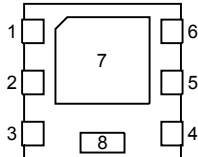
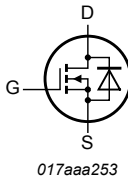


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## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view DFN2020MD-6 (SOT1220)</p>	 <p>017aaa253</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMPB40SNA	DFN2020MD-6	DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1220

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PMPB40SNA	1E

## 8. Limiting values

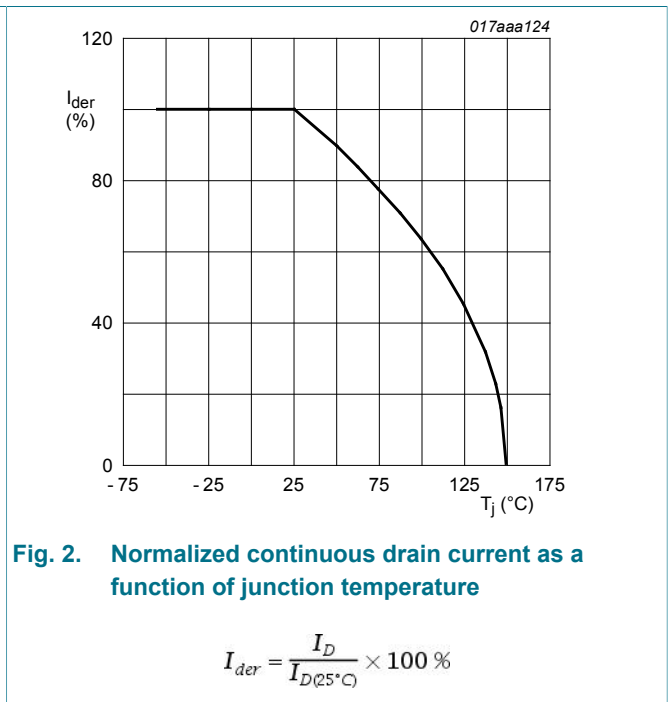
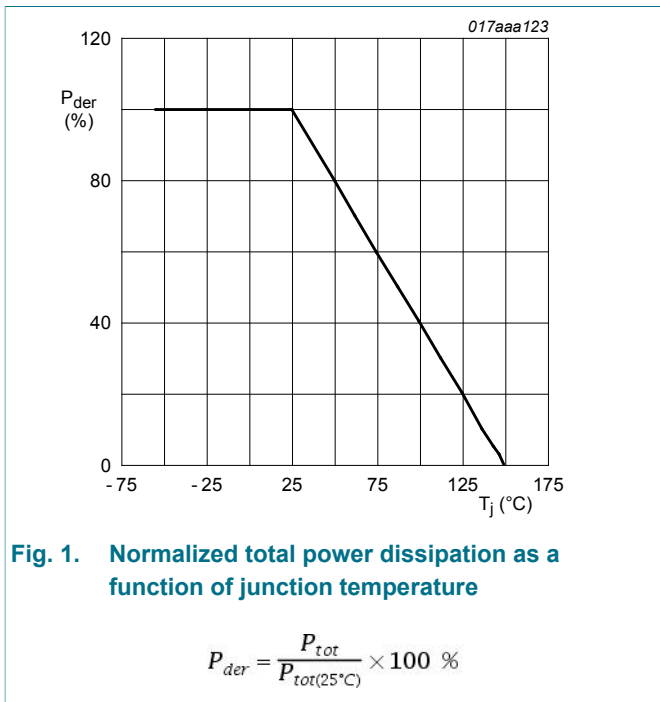
Table 5. Limiting values

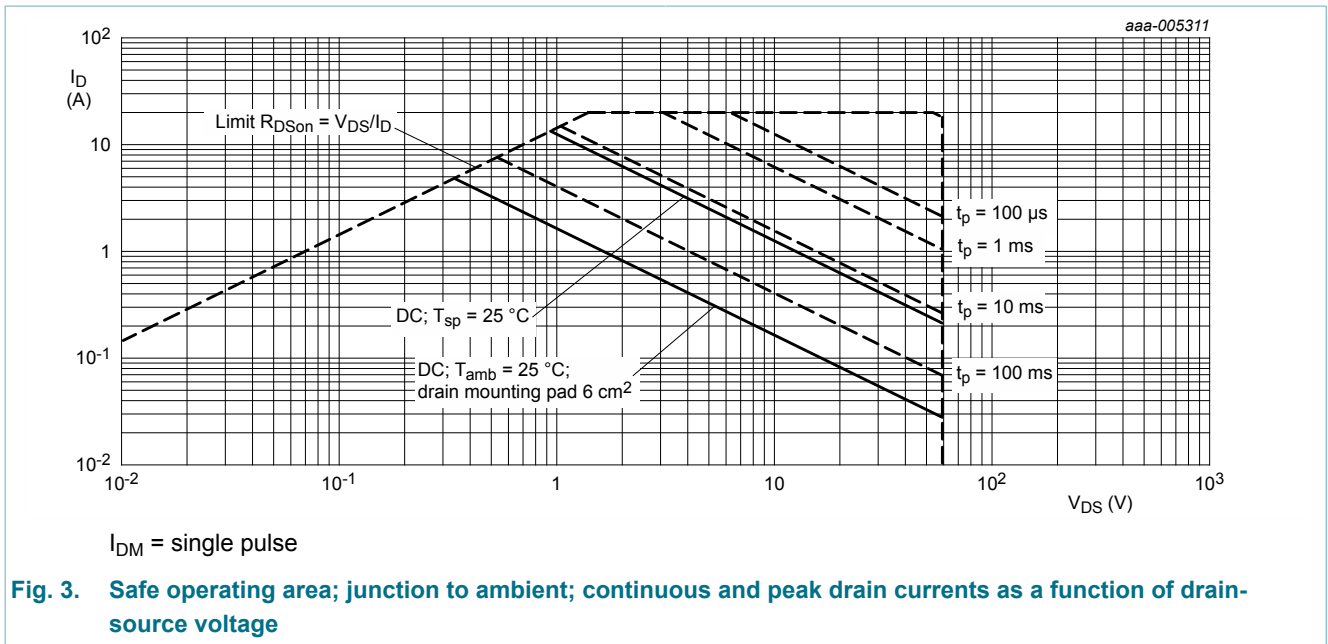
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	60	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{sp} = 25\text{ °C}$	-	12.9	A
		$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	6.8	A
		$V_{GS} = 10\text{ V}; T_{amb} = 100\text{ °C}$	[1]	3	A
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$	-	23	A

Symbol	Parameter	Conditions		Min	Max	Unit
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $I_D = 0.6\text{ A}$ ; DUT in avalanche (unclamped)		-	19	mJ
$P_{\text{tot}}$	total power dissipation	$T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$	[1]	-	1.7	W
		$T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$ ; $t \leq 5\text{ s}$	[1]	-	3.5	W
		$T_{\text{sp}} = 25\text{ }^{\circ}\text{C}$		-	12.5	W
$T_j$	junction temperature			-55	150	$^{\circ}\text{C}$
$T_{\text{amb}}$	ambient temperature			-55	150	$^{\circ}\text{C}$
$T_{\text{stg}}$	storage temperature			-65	150	$^{\circ}\text{C}$
<b>Source-drain diode</b>						
$I_S$	source current	$T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$	[1]	-	1.7	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ .





## 9. Thermal characteristics

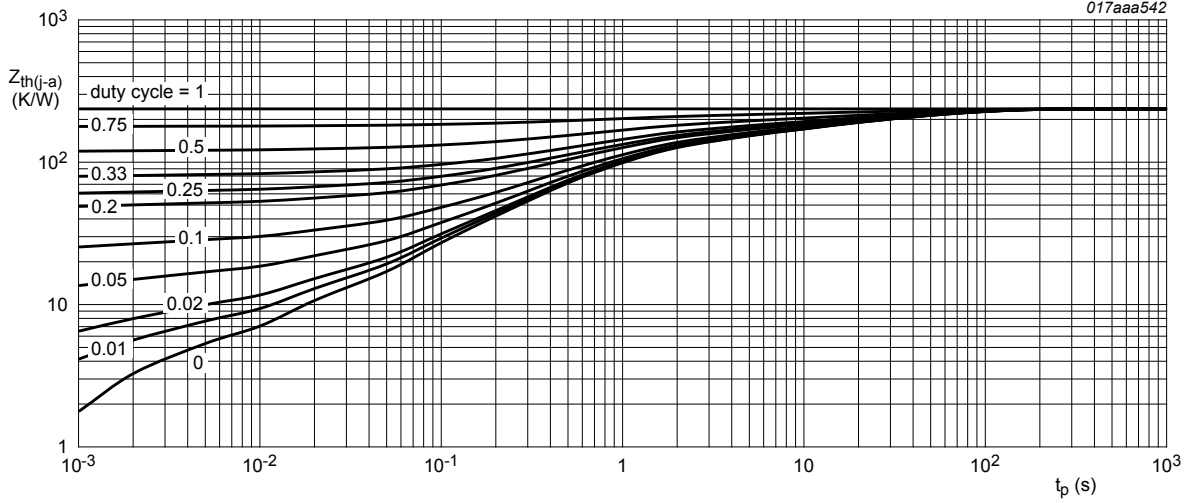
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	235	270	K/W
			[2]	-	67	74	K/W
			[3]	-	33	36	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	5	10	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

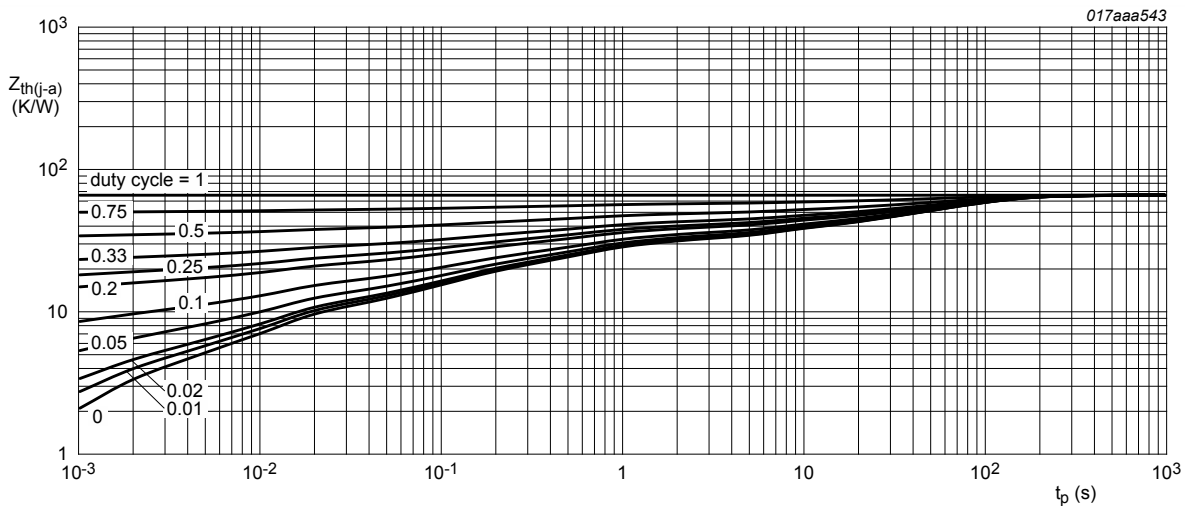
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ .

[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ ,  $t \leq 5\text{ s}$



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm<sup>2</sup>

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1	1.7	3	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	20	$\mu A$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	100	nA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	-100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 4.8 A; T <sub>j</sub> = 25 °C	-	34	43	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 4.8 A; T <sub>j</sub> = 150 °C	-	60	75	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 3.2 A; T <sub>j</sub> = 25 °C	-	40	50	mΩ
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 5 V; I <sub>D</sub> = 4.8 A; T <sub>j</sub> = 25 °C	-	19	-	S
R <sub>G</sub>	gate resistance	f = 1 MHz	-	1.1	-	Ω
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	V <sub>DS</sub> = 30 V; I <sub>D</sub> = 4.8 A; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C	-	12.1	24	nC
Q <sub>GS</sub>	gate-source charge		-	1.4	-	nC
Q <sub>GD</sub>	gate-drain charge		-	2.1	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 30 V; f = 1 MHz; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	612	-	pF
C <sub>oss</sub>	output capacitance		-	78	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	52	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 30 V; I <sub>D</sub> = 4.8 A; V <sub>GS</sub> = 4.5 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C	-	9	-	ns
t <sub>r</sub>	rise time		-	23	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	12	-	ns
t <sub>f</sub>	fall time		-	12	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 1.7 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.9	1.2	V

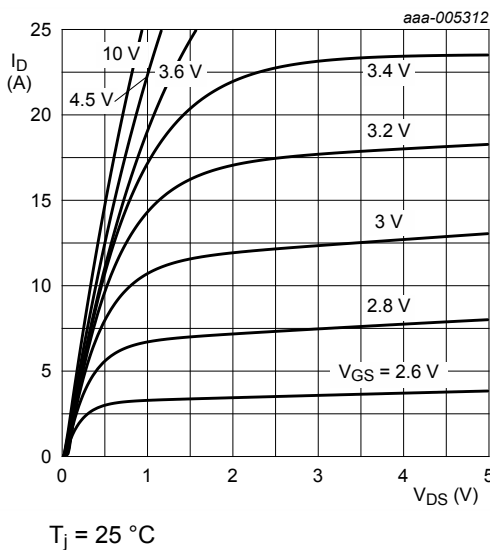


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

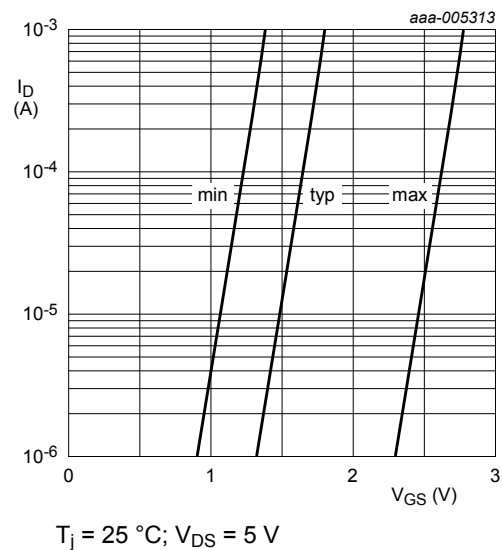
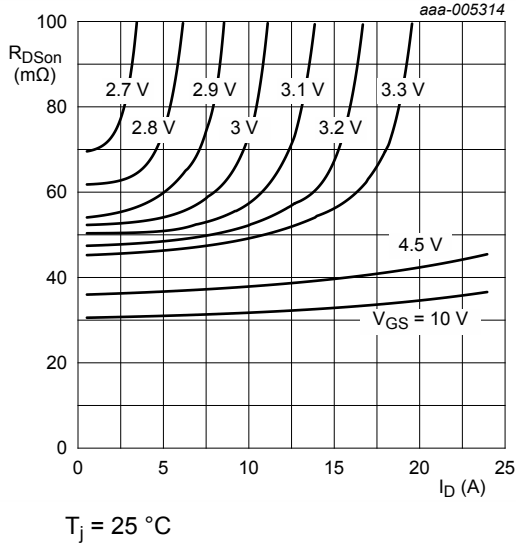
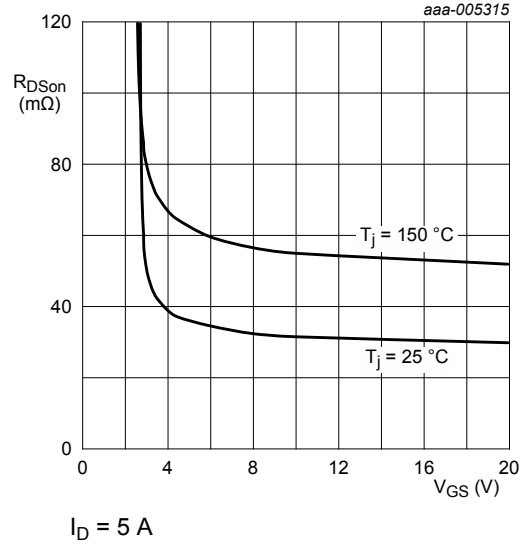


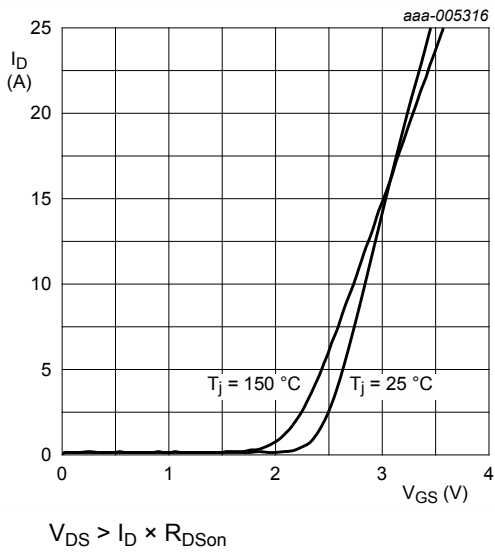
Fig. 7. Subthreshold drain current as a function of gate-source voltage



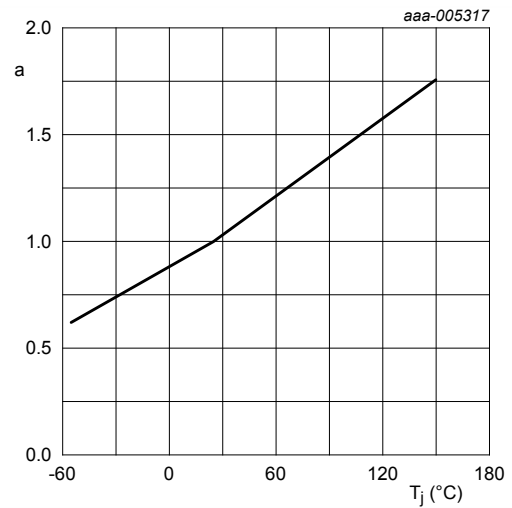
**Fig. 8. Drain-source on-state resistance as a function of drain current; typical values**



**Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



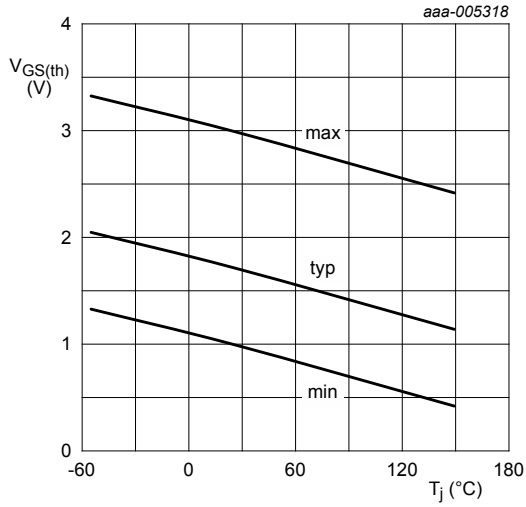
**Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



**Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**

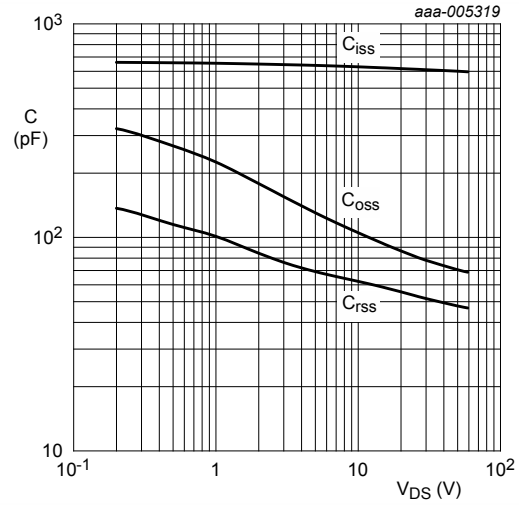
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$





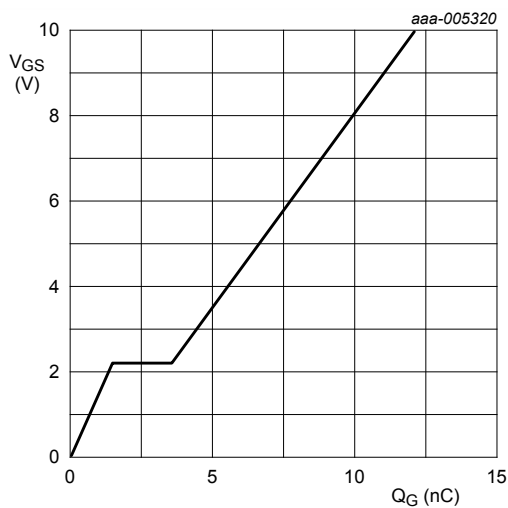
$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$

**Fig. 12. Gate-source threshold voltage as a function of junction temperature**



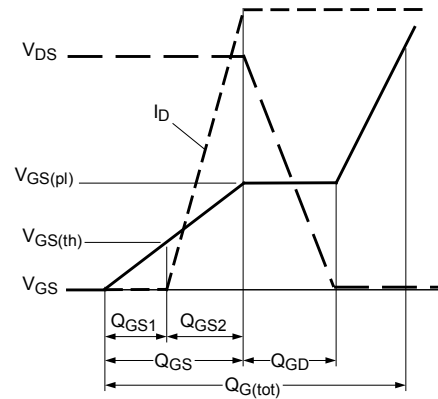
$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

**Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

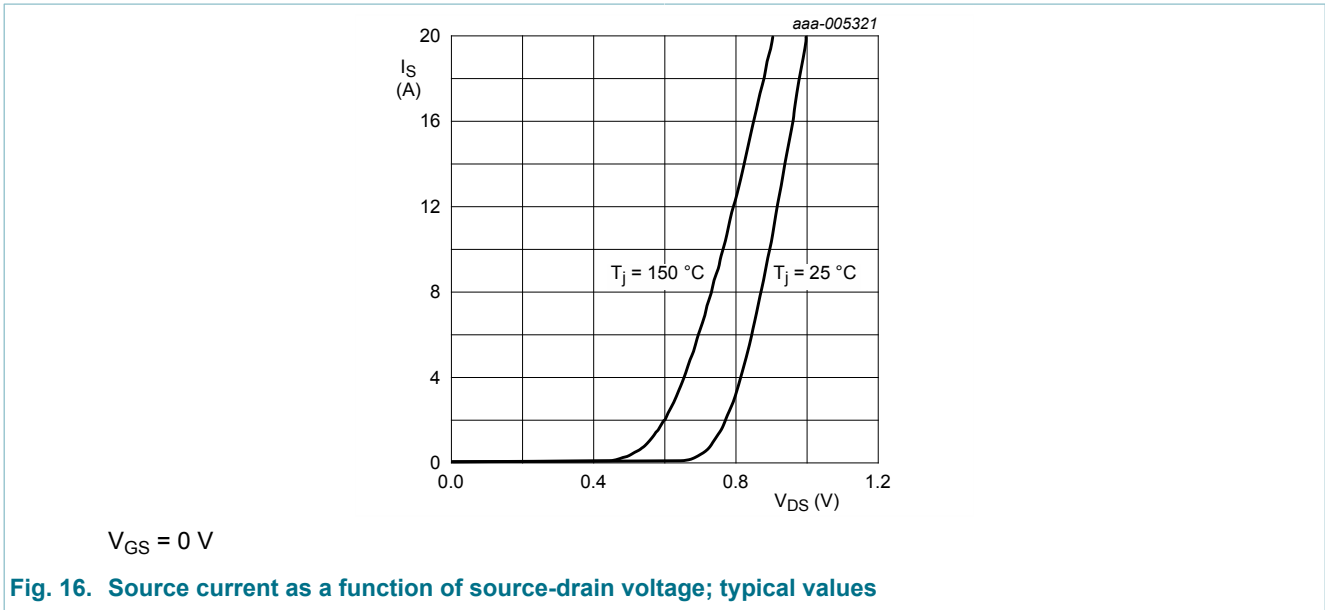


$I_D = 5 \text{ A}; V_{DS} = 30 \text{ V}; T_{amb} = 25 \text{ °C}$

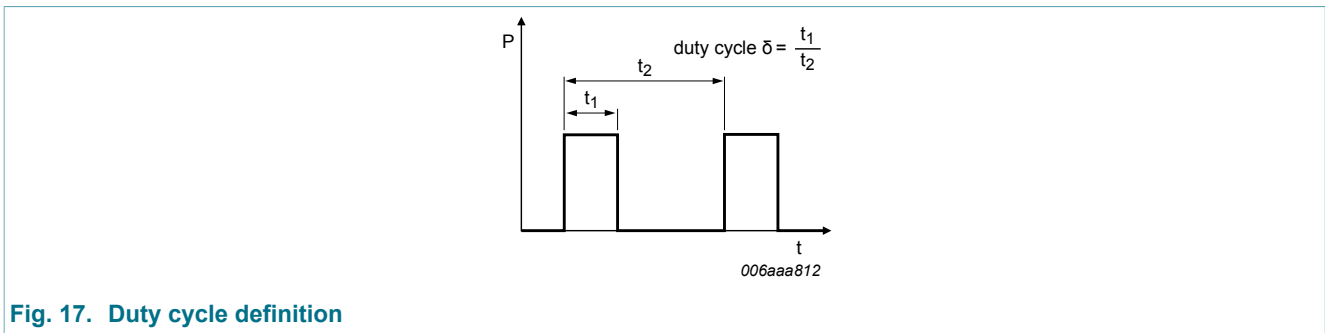
**Fig. 14. Gate-source voltage as a function of gate charge; typical values**



**Fig. 15. Gate charge waveform definitions**



## 11. Test information



### 11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

## 12. Package outline

DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads;  
6 terminals; body 2 x 2 x 0.65 mm

SOT1220

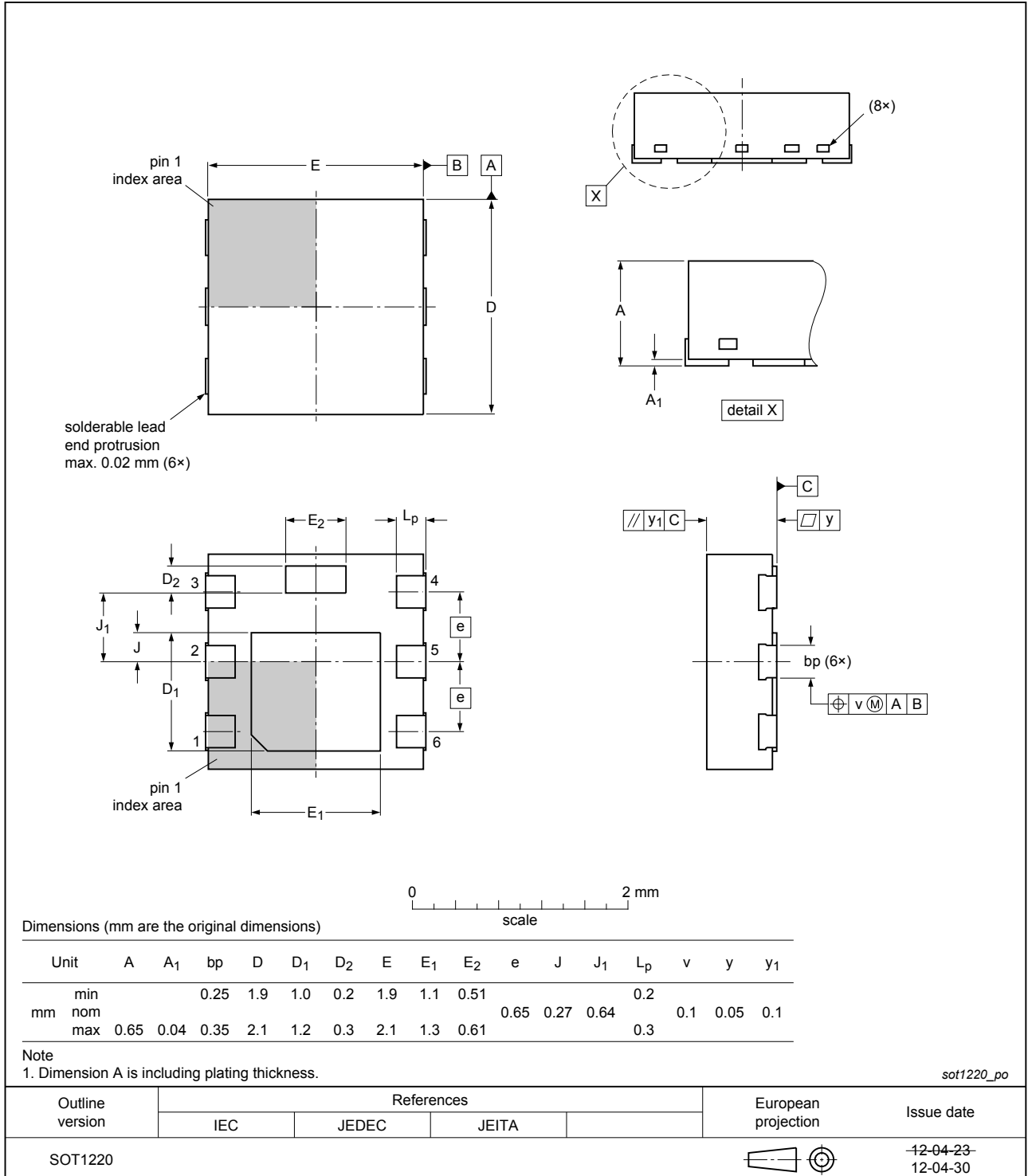


Fig. 18. Package outline DFN2020MD-6 (SOT1220)

### 13. Soldering

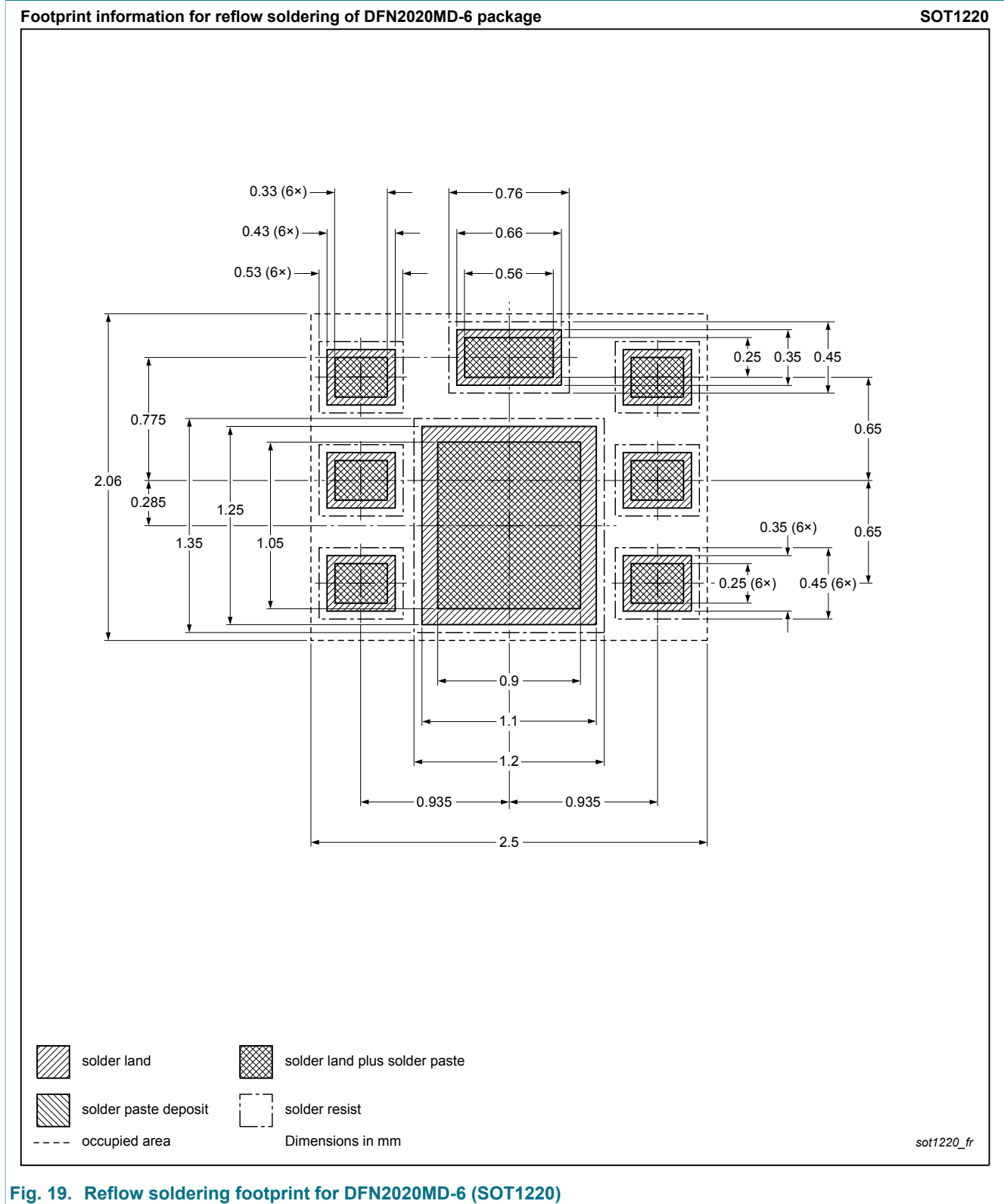


Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB40SNA v.3	20131029	Product data sheet	-	PMPB40SNA v.2
Modifications:	<ul style="list-style-type: none"><li>• Figure 8 corrected</li></ul>			
PMPB40SNA v.2	20130702	Product data sheet	-	PMPB40SNA v.1
PMPB40SNA v.1	20120928	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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