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NLX1G99

Configurable Multifunction Gate

The NLX1G99 MiniGate™ is an advanced high−speed CMOS multifunction gate with a 3−state output. With the output enable input ($\overline{OE}$) at High, the output is disabled and is kept at high impedance. With the output enable input ($\overline{OE}$) at Low, the device can be configured for logic functions such as MUX, AND, OR, NAND, NOR, XOR, XNOR, INVERT and BUFFER, depending on the combination of the 4−bit input. The device has Schmitt−trigger inputs, thereby enhancing noise immunity.

The NLX1G99 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

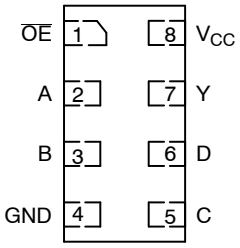
Features

- High Speed: t_{PD} = 6.7 ns (Max) @ V_{CC} = 3.3 V
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra−Small Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

PIN ASSIGNMENT

1	$\overline{OE}$
2	A
3	B
4	GND
5	C
6	D
7	Y
8	V_{CC}

PIN ASSIGNMENTS



(Top View)

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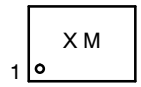
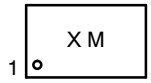
MARKING DIAGRAMS

UDFN8
1.45 x 1.0
CASE 517BZ



UDFN8
1.6 x 1.0
CASE 517BY



UDFN8
1.95 x 1.0
CASE 517CA

AA or E = Specific Device Code
M = Date Code
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

FUNCTION DIAGRAM

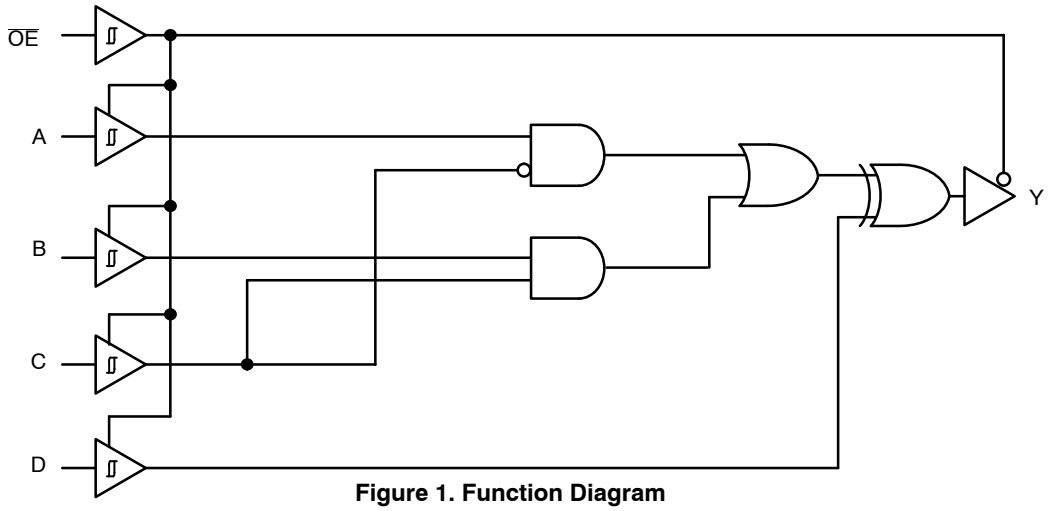


Figure 1. Function Diagram

FUNCTION TABLE*

INPUT					OUTPUT
$\overline{OE}$	D	C	B	A	Y
L	L	L	L	L	L
L	L	L	L	H	H
L	L	L	H	L	L
L	L	L	H	H	H
L	L	H	L	L	L
L	L	H	L	H	L
L	L	H	H	L	H
L	L	H	H	H	H
L	H	L	L	L	H
L	H	L	L	H	L
L	H	L	H	L	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	L	H	H
L	H	H	H	L	L
L	H	H	H	H	L
H	H or L	H or L	H or L	H or L	Z

*To select a logic function, please refer to “Logic Configurations” section.

FUNCTION SELECTION	LOGIC CONFIGURATION PAGE
3−State Buffers	3
3−State Inverters	3
3−State MUXes	3
3−State AND / OR / NOR	4
3−State NAND / OR	5
3−State XOR/XNOR	6

LOGIC CONFIGURATIONS

3−State Buffer Functions Available

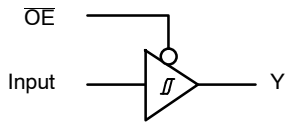


Figure 2.

Function	$\overline{OE}$	A	B	C	D
3−State Buffer	L	Input H or L L H H H or L L	H or L Input H L H or L L L	L H Input Input L H H or L	L L L H Input Input Input

3−State Inverter Functions Available

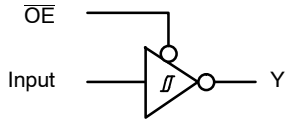


Figure 3.

Function	$\overline{OE}$	A	B	C	D
3−State Buffer	L	Input X L H H H or L H	H or L Input H L H or L H H	L H Input Input L H H or L	H H H L Input Input Input

3−State MUX Functions Available

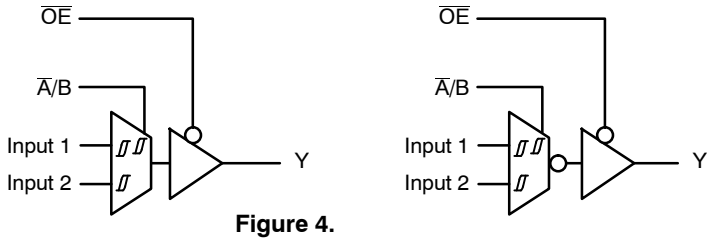


Figure 4.

Function	$\overline{OE}$	A	B	C	D
3−State 2−to−1 3−State 2−to−1 3−State 2−to−1, Inverted Out 3−State 2−to−1, Inverted Out	L	Input 1 Input 2 Input 1 Input 2	Input 2 Input 1 Input 2 Input 1	$\overline{\text{Input 1}}$ or Input 2 $\overline{\text{Input 2}}$ or Input 1 $\overline{\text{Input 1}}$ or Input 2 $\overline{\text{Input 2}}$ or Input 1	L L H H

3−State AND/NOR/OR Function Available

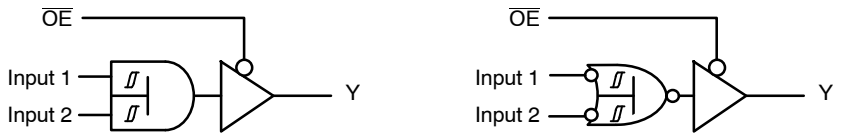


Figure 5.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2 2	3−State AND 3−State AND	3−State NOR 3−State NOR	L	L L	Input 1 Input 2	Input 2 Input 1	L L

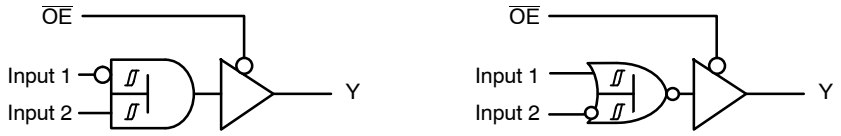


Figure 6.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2 2	3−State AND 3−State AND	3−State NOR 3−State NOR	L	Input 2 H	L Input 1	Input 1 Input 2	L H

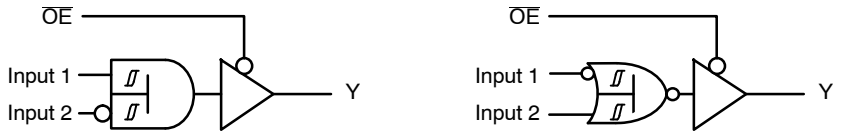


Figure 7.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2 2	3−State AND 3−State AND	3−State NOR 3−State NOR	L	Input 1 H	L Input 2	Input 2 Input 1	L H

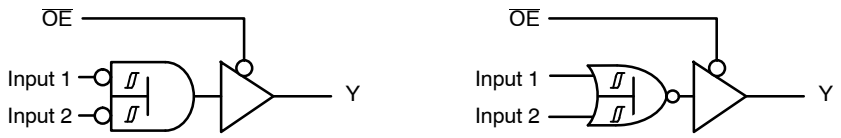


Figure 8.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2 2	3−State AND 3−State AND	3−State NOR 3−State NOR	L	Input 1 Input 2	H H	Input 2 Input 1	H H

3−State NAND/OR Function Available

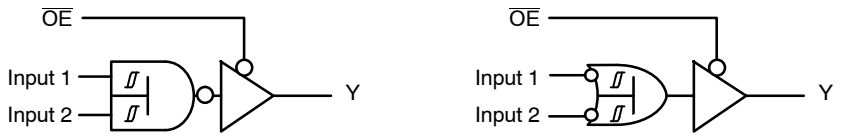


Figure 9.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2 2	3−State NAND 3−State NAND	3−State OR 3−State OR	L	L L	Input 1 Input 2	Input 2 Input 1	H H

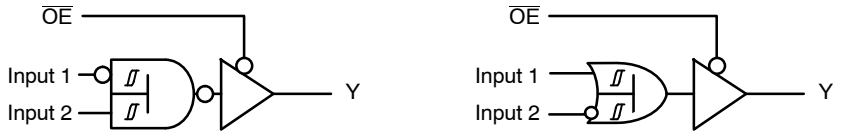


Figure 10.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2 2	3−State NAND 3−State NAND	3−State OR 3−State OR	L	Input 2 H	L Input 1	Input 1 Input 2	H L

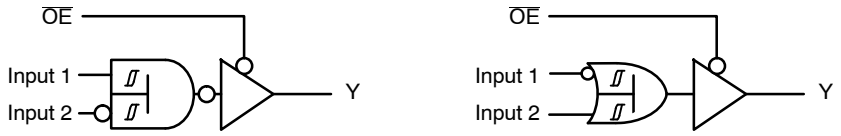


Figure 11.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2 2	3−State NAND 3−State NAND	3−State OR 3−State OR	L	Input 1 H	L Input 2	Input 2 Input 1	H L

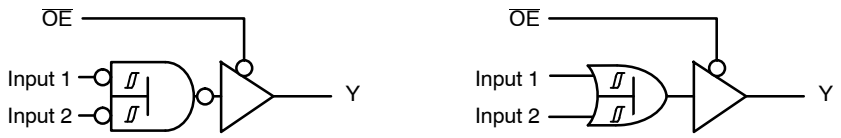


Figure 12.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2 2	3−State AND 3−State AND	3−State OR 3−State OR	L	Input 1 Input 2	H H	Input 2 Input 1	L L

3−State XOR/XNOR Function Available

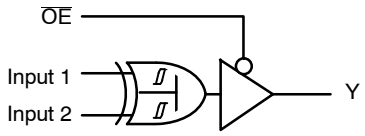


Figure 13.

Function	$\overline{OE}$	A	B	C	D
3−State XOR	L	Input 1 Input 2 H or L H or L L L	H or L H or L Input 1 Input 2 H H	L L H H Input 1 Input 2	Input 2 Input 1 Input 2 Input 1 Input 2 Input 1

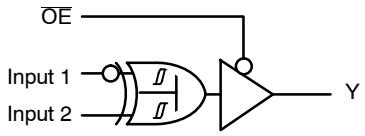


Figure 14.

Function	$\overline{OE}$	A	B	C	D
3−State XOR	L	H	L	Input 1	Input 2

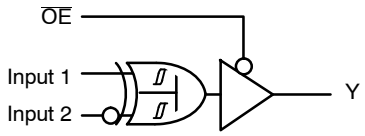


Figure 15.

Function	$\overline{OE}$	A	B	C	D
3−State XOR	L	H	L	Input 1	Input 2

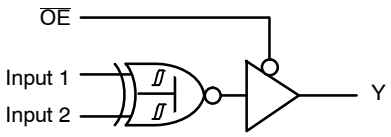


Figure 16.

Function	$\overline{OE}$	A	B	C	D
3−State XNOR 3−State XNOR	L	H H	L L	Input 1 Input 2	Input 2 Input 1

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	DC Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage	Active Mode (High or Low State) Tristate Mode (Output at Hi−Z) Power Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +7.0 −0.5 to +7.0	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	−50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC}	DC Supply Current Per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		150	°C
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34		UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 5)		±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD22−A114−A.
3. Tested to EIA / JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		1.65	5.5	V
V_{IN}	Digital Input Voltage		0	5.5	V
V_{OUT}	Output Voltage	Active Mode (High or Low State) Tristate Mode (Output at Hi−Z) Power Down Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 5.5 5.5	V
T_A	Operating Free−Air Temperature		−55	+125	°C
$\Delta t / \Delta V$	Input Transition Rise or Fall Rate	V_{CC} = 2.5 V ± 0.2 V V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0 0	No Limit No Limit No Limit	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C		$T_A \leq$ +85°C		T_A = −55°C to +125°C		Unit
				Min	Max	Min	Max	Min	Max	
V_{T+}	Positive Threshold Voltage		1.65 1.8 2.3 3.0 4.5 5.5	0.79 0.87 1.11 1.5 2.16 2.61	1.16 1.28 1.56 1.87 2.74 3.33		1.16 1.28 1.56 1.87 2.74 3.33		1.16 1.28 1.56 1.87 2.74 3.33	V
V_{T-}	Negative Threshold Voltage		1.65 1.8 2.3 3.0 4.5 5.5	0.35 0.38 0.58 0.84 1.41 1.78	0.62 0.68 0.87 1.19 1.9 2.29	0.35 0.38 0.58 0.84 1.41 1.78		0.35 0.38 0.58 0.84 1.41 1.78		V
V_H	Hysteresis Voltage		1.65 1.8 2.3 3.0 4.5 5.5	0.30 0.33 0.40 0.53 0.71 0.8	0.62 0.68 0.8 0.87 1.04 1.2	0.30 0.33 0.40 0.53 0.71 0.8	0.62 0.68 0.8 0.87 1.04 1.2	0.30 0.33 0.40 0.53 0.71 0.8	0.62 0.68 0.8 0.87 1.04 1.2	V
V_{OH}	Minimum High−Level Output Voltage	$V_{IN} = V_{T-MIN}$ or V_{T+MAX} I_{OH} = −50 μA I_{OH} = −100 μA	 1.65−5.5 1.65−5.5	 V_{CC}−0.1 V_{CC}−0.1		 V_{CC}−0.1 V_{CC}−0.1		 V_{CC}−0.1 V_{CC}−0.1		V
		$V_{IN} = V_{T-MIN}$ or V_{T+MAX} I_{OH} = −4 mA I_{OH} = −8 mA I_{OH} = −12 mA I_{OH} = −16 mA I_{OH} = −24 mA I_{OH} = −32 mA	 1.65 2.3 2.7 3.0 3.0 4.5	 1.2 1.9 2.2 2.4 2.3 3.8		 1.2 1.9 2.2 2.4 2.3 3.8		 1.2 1.9 2.2 2.4 2.3 3.8		V
V_{OL}	Maximum Low−Level Output Voltage	$V_{IN} = V_{T-MIN}$ or V_{T+MAX} I_{OL} = 50 μA I_{OL} = 100 μA	 1.65−5.5 1.65−5.5		 0.1 0.1		 0.1 0.1		 0.1 0.1	V
		$V_{IN} = V_{T-MIN}$ or V_{T+MAX} I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 12 mA I_{OL} = 16 mA I_{OL} = 24 mA I_{OL} = 32 mA	 1.65 2.3 2.7 3.0 3.0 4.5		 0.45 0.3 0.4 0.4 0.55 0.55		 0.45 0.3 0.4 0.4 0.55 0.55		 0.45 0.3 0.4 0.4 0.55 0.55	
I_{IN}	Input Leakage Current	$0 \leq V_{IN} \leq$ 5.5 V	0 − 5.5		±0.1		±1.0		±1.0	μA
I_{off}	Power off Leakage Current	V_{IN} or V_O = 5.5 V	0		±1.0		±10		±10	μA
I_{OZ}	Tri−state Output Leakage Current	$V_O = V_{CC}$ or GND	1.65−5.5		±1.0		±10		±10	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, I_O = 0	1.65−5.5		1.0		10		10	μA
ΔI_{CC}	Increase in I_{CC} Per Input	One input at (V_{CC}−0.6) V, other inputs at V_{CC} or GND	2.3 − 5.5		10		100		100	μA

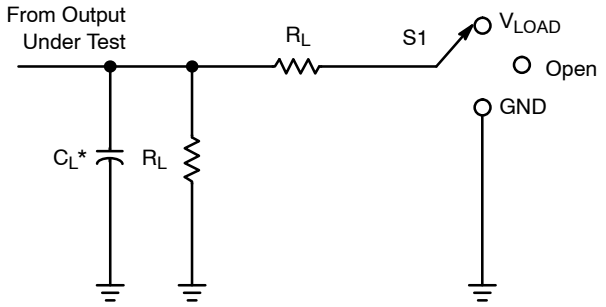
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	V_{CC} (V)	Test Condition	T_A = 25°C			$T_A \leq$ +85°C		T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, Any Input to Output Y (See Test Circuit)	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch positions and loading conditions in Figure 17 to 21.	4.3 2.4 1.7 1.3	12.8 7.1 5.2 4.0	25.1 10.2 6.7 4.5	4.3 2.4 1.7 1.3	25.1 10.2 6.9 4.9	4.3 2.4 1.7 1.3	25.1 10.2 7.0 5.0	ns
t_{EN}	Output Enable Time, $\overline{OE}$ to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch positions and loading conditions in Figure 17 to 21.	3.4 2.1 1.3 1.0		24.7 11 7.5 5.7	3.4 2.1 1.3 1.0	24.7 12 8.0 6.2	3.4 2.1 1.3 1.0	24.7 12.2 8.3 6.5	ns
t_{DIS}	Output Disable Time, $\overline{OE}$ to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch positions and loading conditions in Figure 17 to 21.	4.0 2.7 3.5 2.0		15.5 7.5 7.0 5.5	4.0 2.7 3.5 2.0	15.5 7.5 7.0 5.5	4.0 2.7 3.5 2.0	15.5 7.5 7.0 5.5	ns
t_{PLH}, t_{PHL}	Propagation Delay, Any Input to Output Y (See Test Circuit)	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch Positions and loading conditions in Figure 22 to 26.	4.3 2.5 2.3 1.6	13.6 7.8 5.6 4.4	25.7 10.7 7.6 5.2	4.3 2.5 2.3 1.6	25.7 10.7 7.6 5.2	4.3 2.5 2.3 1.6	25.7 10.7 7.6 5.2	ns
t_{EN}	Output Enable Time, $\overline{OE}$ to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch Positions and loading conditions in Figure 22 to 26.	4.2 2.4 2.0 1.7		25.2 11.3 8.0 6.0	4.2 2.4 2.0 1.7	25.2 12.2 8.5 6.5	4.2 2.4 2.0 1.7	25.2 13 8.7 6.7	ns
t_{DIS}	Output Disable Time, $\overline{OE}$ to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch Positions and loading conditions in Figure 22 to 26.	3.7 2.0 2.1 1.0		15 6.5 5.6 4.5	3.7 2.0 2.1 1.0	15 6.7 5.8 4.7	3.7 2.0 2.1 1.0	15 6.9 5.9 4.9	ns
C_{IN}	Input Capacitance	3.3			3.5						pF
C_O	Output Capacitance	3.3			6.0						pF
C_{PD}	Power Dissipation Capacitance (Note 6)	3.3	f = 10 MHz		22						pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

TEST CIRCUIT AND VOLTAGE WAVEFORMS



*C_L includes probes and jig capacitance.

Figure 17. Load Circuit

Test	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	2 x V_{CC}	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	2 x V_{CC}	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5.5 V ± 0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	2 x V_{CC}	15 pF	1 MΩ	0.3 V

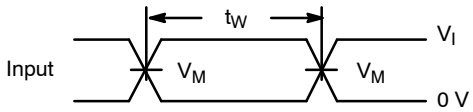


Figure 18. Voltage Waveforms Pulse Duration

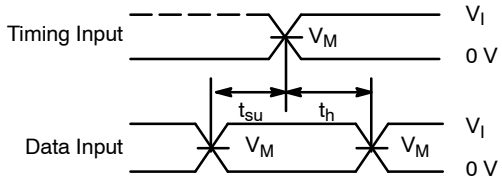


Figure 19. Voltage Waveforms Setup and Hold Times

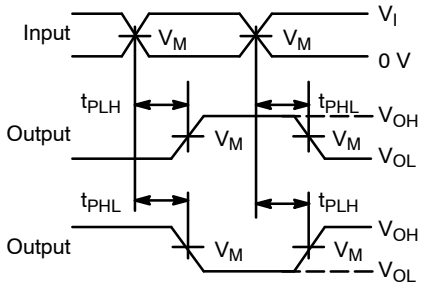


Figure 20. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs

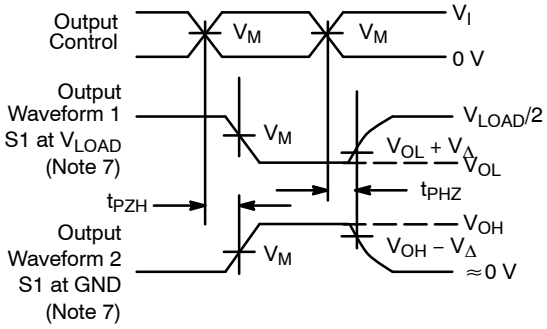
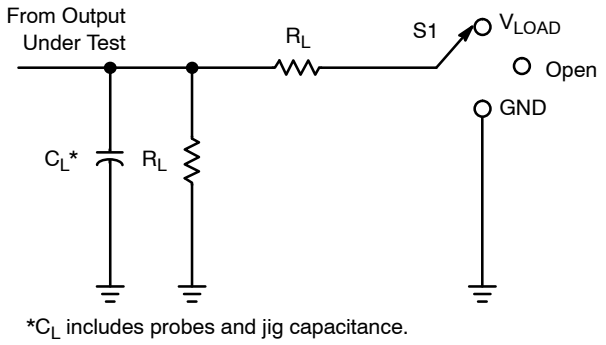


Figure 21. Voltage Waveforms Enable and Disable Times Low– and High–Level Enabling

7. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control
8. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
9. The outputs are measured one at a time, with one transition per measurement.
10. All parameters are waveforms are not applicable to all devices.



*C_L includes probes and jig capacitance.

Test	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

Figure 22. Load Circuit

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	2 x V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	2 x V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5.5 V ± 0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	2 x V_{CC}	50 pF	500 Ω	0.3 V

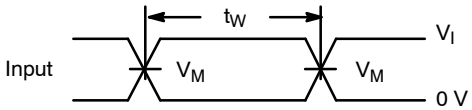


Figure 23. Voltage Waveforms Pulse Duration

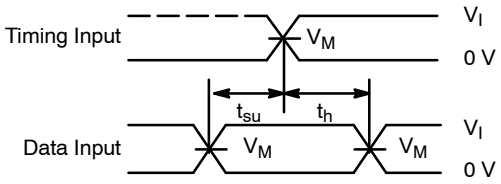


Figure 24. Voltage Waveforms Setup and Hold Times

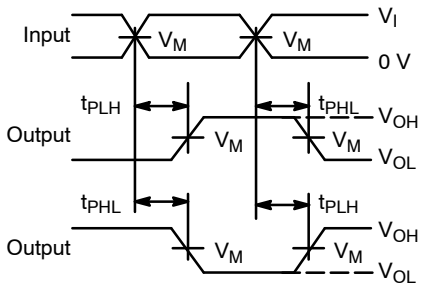


Figure 25. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs

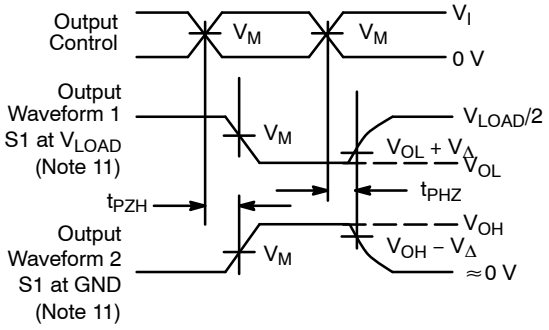


Figure 26. Voltage Waveforms Enable and Disable Times Low− and High−Level Enabling

11. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control
12. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
13. The outputs are measured one at a time, with one transition per measurement.
14. All parameters are waveforms are not applicable to all devices.

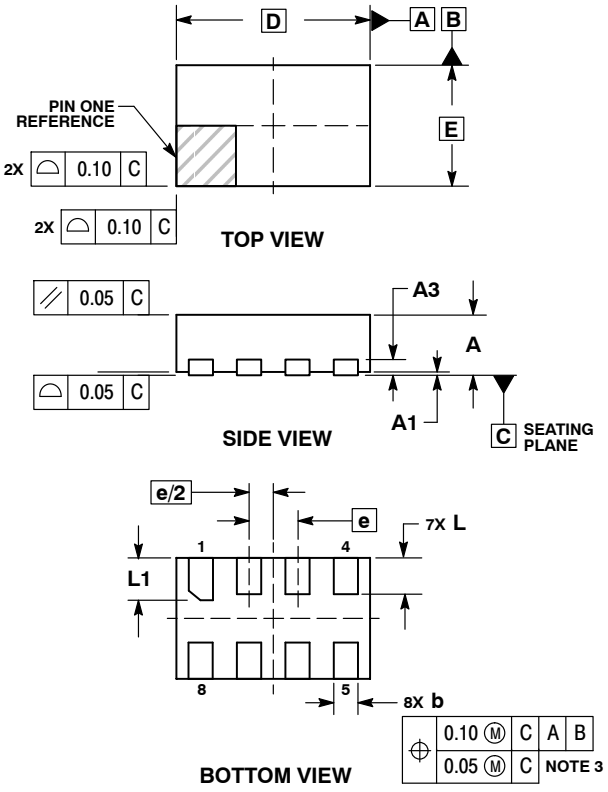
ORDERING INFORMATION

Device	Package	Shipping†
NLX1G99DMUTCG	UDFN8, 1.95 x 1.0, 0.5P (Pb−Free)	3000 / Tape & Reel
NLX1G99DMUTWG	UDFN8, 1.95 x 1.0, 0.5P (Pb−Free)	3000 / Tape & Reel
NLX1G99EMUTCG (In Development)	UDFN8, 1.6 x 1.0, 0.4P (Pb−Free)	3000 / Tape & Reel
NLX1G99FMUTCG (In Development)	UDFN8, 1.45 x 1.0, 0.35P (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

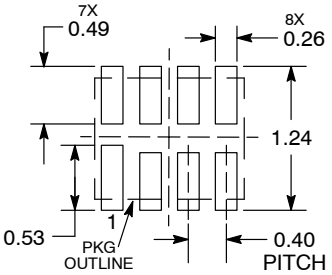
UDFN8 1.6x1.0, 0.4P
CASE 517BY
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

DIM	MILLIMETERS MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.60 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*

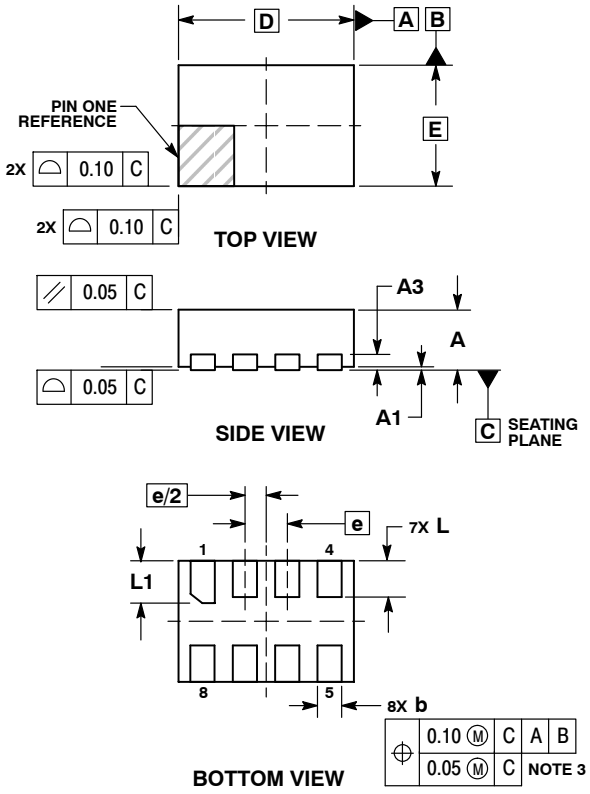


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

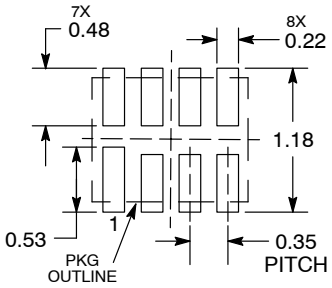
UDFN8 1.45x1.0, 0.35P
CASE 517BZ
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*

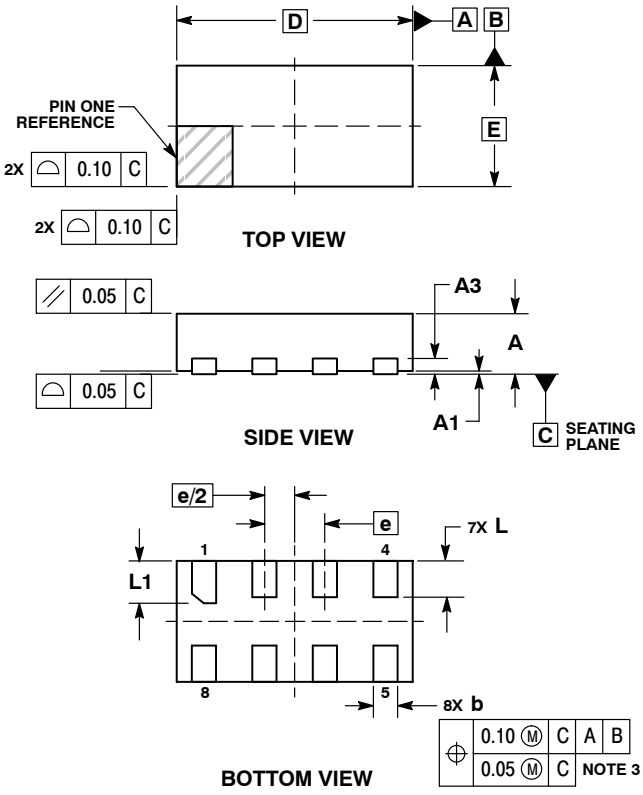


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

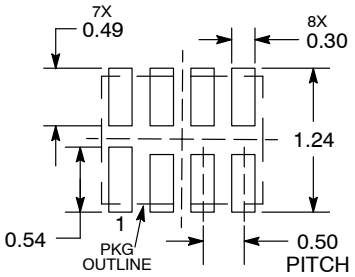
UDFN8 1.95x1.0, 0.5P
CASE 517CA
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.95 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

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