Product Change Notice (PCN)

Subject: Datasheet change for the Listed ISL80111*, ISL80112* and ISL80113* Intersil Products
Publication Date: 9/30/2016
Effective Date: 9/30/2016

Revision Description:
Initial Release

Description of Change:
This notice is to inform you that Intersil has updated the electrical specifications on the "Recommended Operating Conditions", DC Input and Bias Line Regulation and DC Output Load Regulation limits for the products listed below:

ISL80111IRAJZ	ISL80112IRAJZ	ISL80113IRAJZ
ISL80111IRAJZ-T	ISL80112IRAJZ-T	ISL80113IRAJZ-T
ISL80111IRAJZ-T7A	ISL80112IRAJZ-T7A	ISL80113IRAJZ-T7A

Reason for Change:
The change aligns the data sheet with the product characteristics and is necessary to maintain product manufacturability in support of customer delivery requirements. Details regarding the change are contained on the following page. The updated data sheet is available on the Intersil web site at:
http://www.intersil.com/content/dam/Intersil/documents/isl8/isl80111-12-13.pdf

Impact on fit, form, function, quality & reliability:
The change will have no impact on the form, fit, function, quality, reliability and environmental compliance of the devices.

Product Identification:
There have been no changes to the die/silicon or product itself. There will be no change in the external marking of the packaged parts. Product affected by this change is identifiable via Intersil's internal traceability system.

Qualification status: Not applicable
Sample availability: 9/30/2016
Device material declaration: Available upon request

Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Intersil within 30 days of the publication date.

For additional information regarding this notice, please contact your regional change coordinator (below)			
Americas: PCN-US@INTERSIL.COM	Europe: PCN-EU@INTERSIL.COM	Japan: PCN-JP@INTERSIL.COM	Asia Pac: PCN-APAC@INTERSIL.COM

From:

Recommended Operating Conditions (Notes 4, 6)

Junction Temperature Range . . . . . -40°C to +125°C
V_{IN} Relative to GND (ISL80113) (Note 9) . . . . . V_{OUT} + 0.4V to 5V
V_{IN} Relative to GND (ISL80112) (Note 9) . . . . . V_{OUT} + 0.3V to 5V
V_{IN} Relative to GND (ISL80111) (Note 9) . . . . . V_{OUT} + 0.2V to 5V
Nominal V_{OUT} Range . . . . . 800mV to 3.3V
PG, ENABLE, SENSE/ADJ, SS Relative to GND . . . . . 0V to 5.5V
V_{BIAS} Relative to GND . . . . . 0V to 5.5V
V_{BIAS} Relative to V_{OUT} . . . . . +0.8V minimum

To:

Recommended Operating Conditions (Notes 4)

Junction Temperature Range . . . . . -40°C to +125°C
VIN Relative to GND (ISL80113) (Note 8) . . . . . V_{OUT} + 0.30V to 3.6V
VIN Relative to GND (ISL80112) (Note 8) . . . . . V_{OUT} + 0.25V to 3.6V
VIN Relative to GND (ISL80111) (Note 8) . . . . . V_{OUT} + 0.20V to 3.6V
Nominal V_{OUT} Range . . . . . 800mV to 3.3V
PG, ENABLE, ADJ, SS Relative to GND . . . . . 0V to 5.5V
VBIAS Relative to GND . . . . . 0V to 5.5V

From:

Electrical Specifications Unless otherwise specified, $V_{IN} = V_{OUT} + 0.4V$, $V_{BIAS} = 2.9V$, $V_{OUT} = 1.2V$, $C_{BIAS} = 1\mu F$, $C_{IN} = 10\mu F$, $C_{OUT} = 2.2\mu F$, $T_J = +25°C$, $I_L = 0mA$. Applications must follow thermal guidelines of the package to determine worst-case junction temperature. Please refer to "Power Dissipation" on page 13 and Tech Brief TB379.
Boldface limits apply over junction temperature (T_J) range, -40°C to +125°C. Pulse load techniques used by ATE to ensure $T_J = T_A$ where datasheet limits are defined.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNITS
DC CHARACTERISTICS						
V_{BIAS} UVLO	UVLO_BIAS_r	V_{BIAS} Rising		2.3	**2.9**	V
	UVLO_BIAS_f	V_{BIAS} Falling	**1.55**	2.1	**2.8**	V
V_{BIAS} UVLO Hysteresis	$UVLO_{B\_HYS}$			0.2		V
DC ADJ Pin Voltage Accuracy	V_{ADJ}	$1.0V \le V_{IN} \le 3.6V$, $I_{LOAD} = 0A$, $2.9V \le V_{BIAS} \le 5.5V$, $V_{OUT} = V_{ADJ}$	**494**	502	**510**	mV
DC Input Line Regulation	ΔV_{OUT}	$V_{OUT} + 0.4V \le V_{IN} \le 3.6V$		0.01	**0.9**	mV
DC Bias Line Regulation	ΔV_{OUT}	$2.9V < V_{BIAS} < 5.5V$ with respect to ADJ pin		0.3	**1.4**	mV
DC Output Load Regulation	ΔV_{OUT}	$0A \le I_{LOAD} \le 3A$	**-2**	-0.2	**2**	mV
Feedback Input Current		$V_{ADJ} = 0.5V$		10	**80**	nA
V_{IN} Quiescent Current	$I_Q (V_{IN})$	VOUT = 2.5V		8	**10**	mA
V_{IN} Quiescent Current	$I_Q (V_{IN})$	VOUT = 3.3.		10.6		mA

To:

Electrical Specifications Unless otherwise specified, $V_{IN} = 3V$, $V_{BIAS} = 5.5V$, $V_{OUT} = 0.5V$, $T_J = +25°C$, $I_L = 0mA$. Applications must follow thermal guidelines of the package to determine worst-case junction temperature. Please refer to "Power Dissipation" on page 13 and Tech Brief TB379.
Boldface limits apply across junction temperature (T_J) range, -40°C to +125°C. Pulse load techniques used by ATE to ensure $T_J = T_A$ where datasheet limits are defined.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
DC CHARACTERISTICS						
V_{BIAS} UVLO	UVLO_BIAS_r	V_{BIAS} Rising		2.3	**2.9**	V
	UVLO_BIAS_f	V_{BIAS} Falling	**1.55**	2.1	**2.8**	V
V_{BIAS} UVLO Hysteresis	$UVLO_{B\_HYS}$			0.2		V
DC ADJ Pin Voltage Accuracy	V_{ADJ}	$1.0V \le V_{IN} \le 3.6V$, $I_{LOAD} = 0A$, $2.9V \le V_{BIAS} \le 5.5V$, $V_{OUT} = V_{ADJ}$	**494**	502	**510**	mV
DC Input Line Regulation	(V_{OUT} low line-V_{OUT} high line)/V_{OUT} low line	$2.9V \le V_{IN} \le 3.6V$, $V_{OUT} = 2.5V$	**-0.18**	0.02	**0.18**	%
DC Bias Line Regulation	(V_{OUT} low line-V_{OUT} high line)/V_{OUT} low line	$4.5V < V_{BIAS} < 5.5V$, $V_{OUT} = 2.5V$	**-0.28**	0.06	**0.28**	%
DC Output Load Regulation	(V_{OUT} no load-V_{OUT} high load)/V_{OUT} no load	$0A < I_{LOAD} <$ Full Load, $V_{OUT} = 2.5V$	**-0.40**	-0.04	**0.40**	%
Feedback Input Current		$V_{ADJ} = 0.5V$		10	**80**	nA
V_{IN} Quiescent Current	$I_Q (V_{IN})$	$V_{OUT} = 2.5V$		8	**10**	mA
V_{IN} Quiescent Current	$I_Q (V_{IN})$	$V_{OUT} = 3.3V$, $V_{IN} = 3.6V$, $V_{BIAS} = 5V$		10.6		mA