**FAIRCHILD**

SEMICONDUCTOR®

May 2009

# FDMS8670

## N-Channel Power Trench® MOSFET

### 30V, 42A, 2.6mΩ

### Features

- Max $r_{DS(on)}$ = 2.6mΩ at $V_{GS}$ = 10V, $I_D$ = 24A
- Max $r_{DS(on)}$ = 3.8mΩ at $V_{GS}$ = 4.5V, $I_D$ = 18A
- 100% UIL Tested
- RoHS Compliant

### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's latest proprietary Power Trench® process that has been especially tailored to minimize on-resistance. This part exhibits industry leading switching FOM (RDS*Qgd) to enhance DC-DC synchronous rectifier efficiency.

### Application

- DC - DC Conversion



**Top**    **Bottom**    Pin 1

**Power 56**
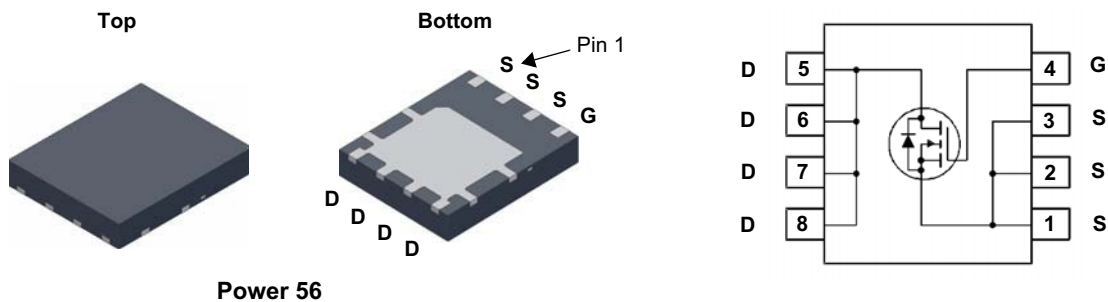
## MOSFET Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | 30 | V |
| $V_{GS}$ | Gate to Source Voltage | | ±20 | V |
| $I_D$ | Drain Current   -Continuous (Package limited)    $T_C$ = 25°C | | 42 | A |
| | -Continuous (Silicon limited)    $T_C$ = 25°C | | 135 | |
| | -Continuous    $T_A$ = 25°C    (Note 1a) | | 24 | |
| | -Pulsed | | 150 | |
| $E_{AS}$ | Single Pulse Avalanche Energy    (Note 3) | | 288 | mJ |
| $P_D$ | Power Dissipation    $T_C$ = 25°C | | 78 | W |
| | Power Dissipation    $T_A$ = 25°C    (Note 1a) | | 2.5 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | -55 to +150 | °C |

### Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | | 1.6 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient    (Note 1a) | | 50 | |

### Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDMS8670 | FDMS8670 | Power 56 | 13" | 12 mm | 3000 units |

## Electrical Characteristics $T_J$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250μA, $V_{GS}$ = 0V | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250μA, referenced to 25°C | | 19.5 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{GS}$ = 0V, $V_{DS}$ = 24V, | | | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20V, $V_{DS}$ = 0V | | | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA | 1.0 | 1.7 | 3.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250μA, referenced to 25°C | | -5.9 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10V, $I_D$ = 24A | | 2.1 | 2.6 | mΩ |
| | | $V_{GS}$ = 4.5V, $I_D$ = 18A | | 3.0 | 3.8 | |
| | | $V_{GS}$ = 10V, $I_D$ = 24A, $T_J$ = 125°C | | 3.0 | 3.8 | |
| $g_{FS}$ | Forward Transconductance | $V_{DD}$ = 5V, $I_D$ = 24A | | 117 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15V, $V_{GS}$ = 0V, f = 1MHz | | 2965 | 3940 | pF |
| $C_{oss}$ | Output Capacitance | | | 1395 | 1855 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 180 | 265 | pF |
| $R_g$ | Gate Resistance | f = 1MHz | | 1.3 | | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 15V, $I_D$ = 24A, $V_{GS}$ = 10V, $R_{GEN}$ = 6Ω | | 14 | 24 | ns |
| $t_r$ | Rise Time | | | 5 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 33 | 53 | ns |
| $t_f$ | Fall Time | | | 4 | 10 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0V to 10V | | 45 | 63 | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0V to 5V | $V_{DD}$ = 15V, $I_D$ = 24A | 23 | 33 | nC |
| $Q_{gs}$ | Gate to Source Charge | | | 8.3 | | nC |
| $Q_{gd}$ | Gate to Drain "Miller" Charge | | | 5.7 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0V, $I_S$ = 24A (Note 2) | | 0.8 | 1.3 | V |
| | | $V_{GS}$ = 0V, $I_S$ = 2.1A (Note 2) | | 0.7 | 1.2 | |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 24A, di/dt = 100A/μs | | 44 | 71 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 27 | 43 | nC |

NOTES:

1. $R_{θJA}$ is determined with the device mounted on a 1in$^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{θJC}$ is guaranteed by design while $R_{θCA}$ is determined by the user's board design.
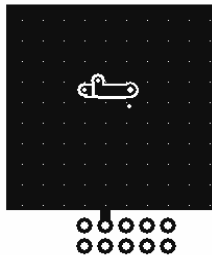


a. 50°C/W when mounted on a 1 in$^2$ pad of 2 oz copper.

b. 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3. Starting $T_J$ = 25°C, L = 1mH, $I_{AS}$ = 24A, $V_{DD}$ = 27V, $V_{GS}$ = 10V.

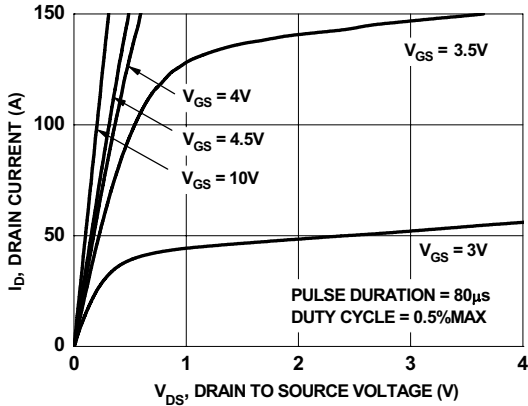## Typical Characteristics $T_J$ = 25°C unless otherwise noted



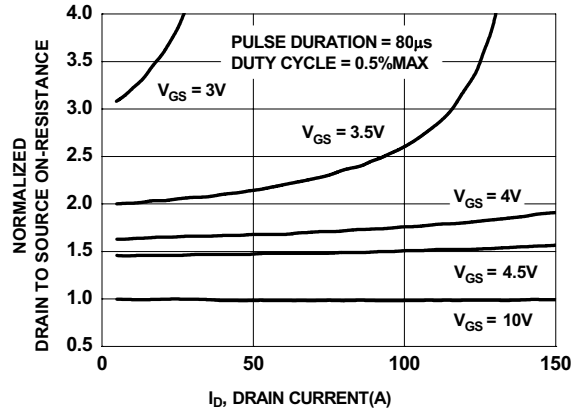Figure 1.  On-Region Characteristics



Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage
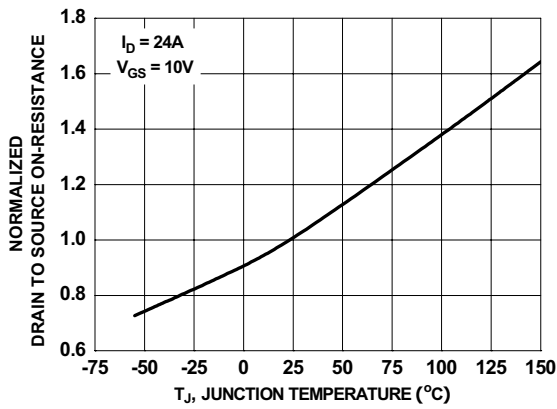


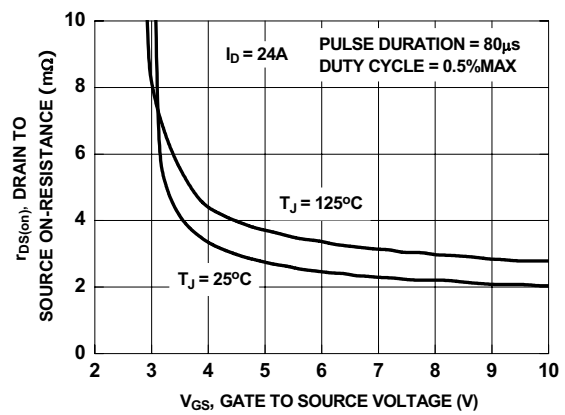Figure 3. Normalized On-Resistance vs Junction Temperature
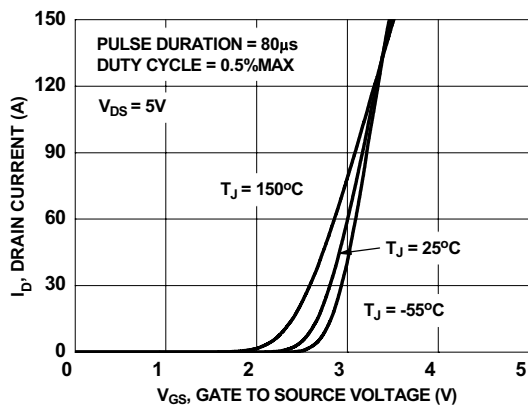


Figure 4.  On-Resistance vs Gate to Source Voltage



Figure 5.  Transfer Characteristics
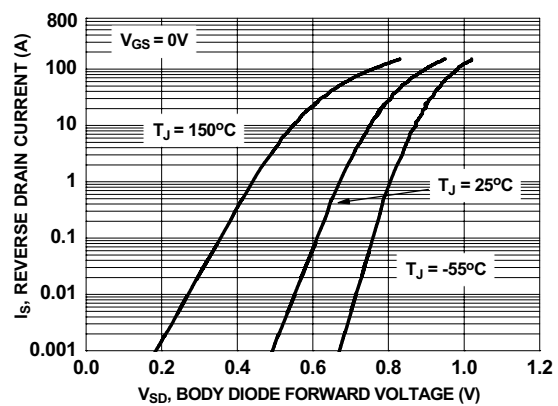


Figure 6.  Source to Drain Diode Forward Voltage vs Source Current

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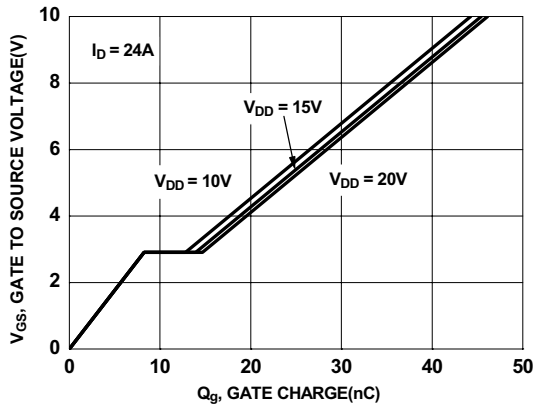## Typical Characteristics $T_J$ = 25°C unless otherwise noted



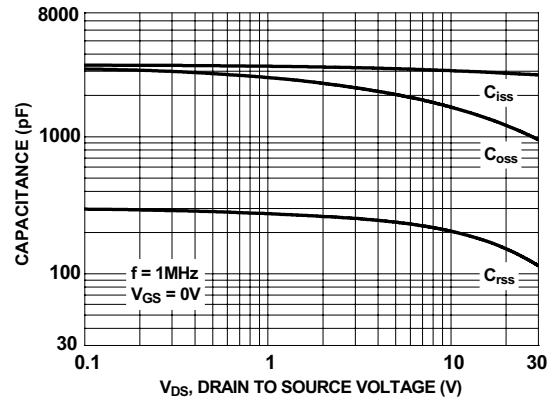**Figure 7. Gate Charge Characteristics**



**Figure 8. Capacitance vs Drain to Source Voltage**
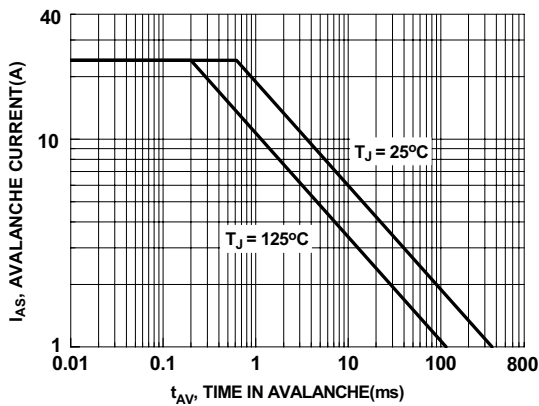


**Figure 9. Unclamped Inductive Switching Capability**
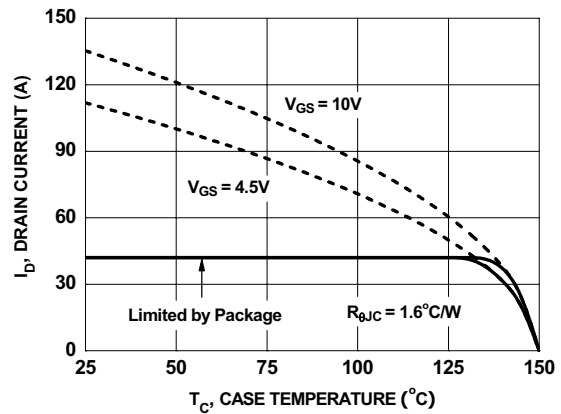


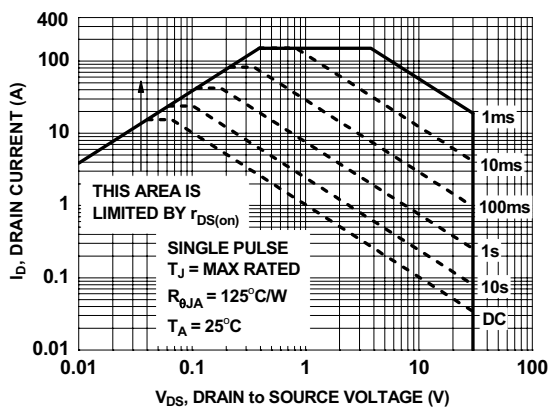**Figure 10. Maximum Continuous Drain Current vs Case Temperature**



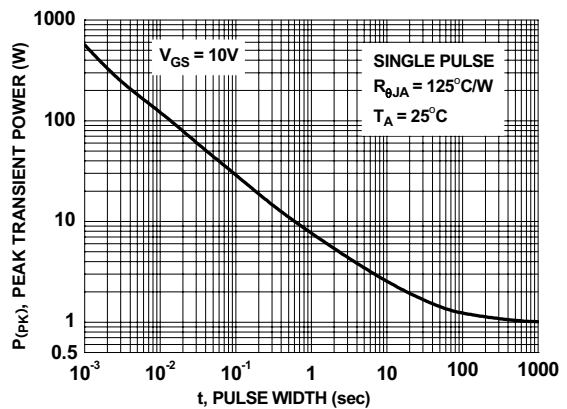**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

## Typical Characteristics $T_J = 25°C$ unless otherwise noted



**DUTY CYCLE-DESCENDING ORDER**

D = 0.5
0.2
0.1
0.05
0.02
0.01

**SINGLE PULSE**
$R_{\theta JA} = 125°C/W$

NORMALIZED THERMAL IMPEDANCE, $Z_{\theta JA}$

t, RECTANGULAR PULSE DURATION (sec)

NOTES:
DUTY FACTOR: $D = t_1/t_2$
PEAK $T_J = P_{DM} \times Z_{\theta JA} \times R_{\theta JA} + T_A$

$P_{DM}$
$t_1$
$t_2$
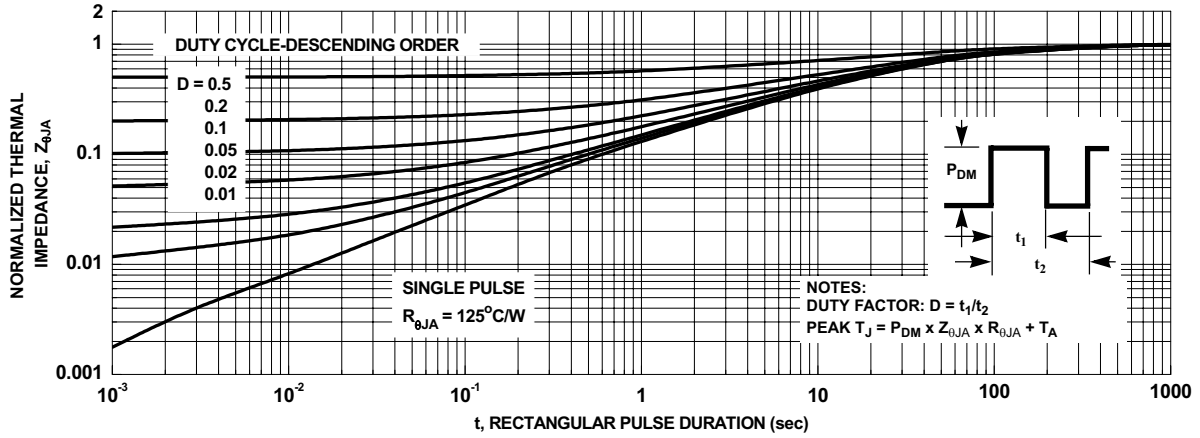
**Figure 13.  Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout

5.00  A

PKG ℄

8    PKG ℄    5    B

PIN #1
IDENT MAY
APPEAR AS
OPTIONAL

1    4    6.00

TOP VIEW

SEE
DETAIL A

SIDE VIEW

3.91    1.27

8    7    6    5

0.77

4.52    6.61

1.27

1    2    3    4

1.27    0.61

3.81

LAND PATTERN
RECOMMENDATION

3.81
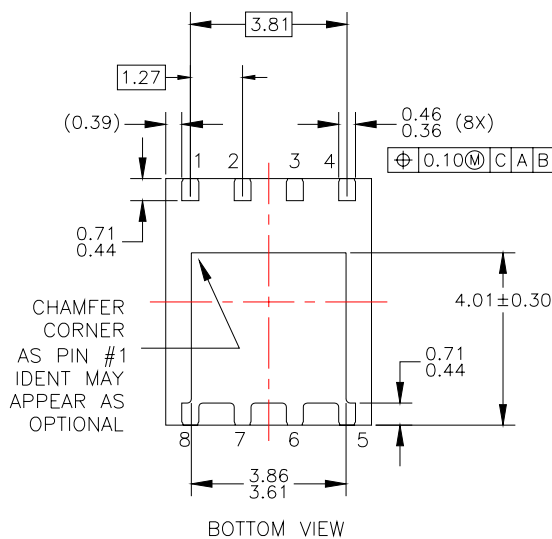
1.27

(0.39)    0.46 / 0.36 (8X)

1    2    3    4    ⊕ 0.10 Ⓜ C A B

0.71 / 0.44

CHAMFER
CORNER
AS PIN #1
IDENT MAY
APPEAR AS
OPTIONAL

4.01±0.30

0.71 / 0.44

8    7    6    5

3.86 / 3.61

BOTTOM VIEW

5.00

OPTIONAL DRAFT
ANGLE MAY APPEAR
ON FOUR SIDES
OF THE PACKAGE

6°

6.15    5.75

OPTIONAL TIE BARS MAY
APPEAR ON THESE AREAS (MAX.
TIE BAR PROTRUSION: 0.15mm)

// 0.10 C

△ 0.08 C

0.30 / 0.20    0.05 / 0.00    C

1.10 / 0.90    SEATING PLANE

DETAIL A
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

A)   PACKAGE STANDARD REFERENCE:
     JEDEC MO-240, ISSUE A, VAR. AA,
     DATED OCTOBER 2002.
B)   ALL DIMENSIONS ARE IN MILLIMETERS.
C)   DIMENSIONS DO NOT INCLUDE BURRS
     OR MOLD FLASH. MOLD FLASH OR
     BURRS DOES NOT EXCEED 0.10MM.
D)   DIMENSIONING AND TOLERANCING PER
     ASME Y14.5M-1994.
E)   DRAWING FILE NAME: PQFN08AREV4
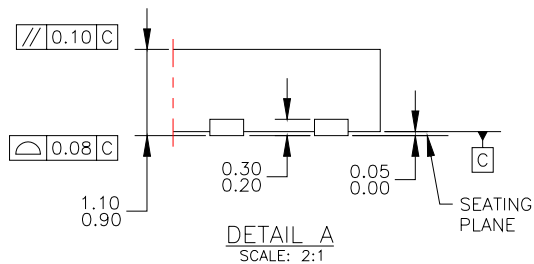
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| EcoSPARK® | IntelliMAX™ | | TINYOPTO™ |
| EfficentMax™ | ISOPLANAR™ | | TinyPower™ |
| EZSWITCH™ * | MegaBuck™ | Saving our world, 1mW /W /kW at a time™ | TinyPWM™ |
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