CHANGE NOTIFICATION

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900

March 17, 2014

Dear Sir/Madam: PCN# 031714

Subject: Notification of Additional Wafer Fab Location Tower Semiconductor Ltd., Israel For Part Number: LTC3411

Linear Technology has successfully qualified the Tower Semiconductor wafer fabrication facility located in Migdal Haemek, Israel. LTC currently owns and operates two wafer fabrication facilities located in Camas, Washington and Milpitas, California. The ability to process wafers in an additional wafer fabrication facility provides an extra measure of safety to insure uninterrupted product flow to our customers.

The qualification of the Tower Semiconductor consisted of 1,000 hours of op-life testing, temp cycle, thermal shock, autoclave, and 1,000 hours of bake at 150°C and 175°C. Additionally, devices have been characterized over the full operating temperature range and have been subjected to ESD testing and latch up immunity testing. The devices have been found to meet the LTC data sheets. Additionally, devices from the Tower Semiconductor were carefully compared to the LTC fabricated devices to ensure identical performance when installed in customer applications.

The first product manufactured in Tower Semiconductor will have the effective date code of approximately 1420. The devices manufactured in Tower Semiconductor will have the same part number and the same top mark as those manufactured at LTC. However, when necessary we can use our lot number traceability system to identify where and when a device was fabricated.

Qualification test results, Tower Semiconductor third party certifications and capacity details are attached for your review. Additional information can be found at www.jazzsemi.com.

Linear Technology is requesting your expeditious approval of this PCN so that LTC can service your delivery requests. Should you have any questions or concerns please contact me at 408-432-1900 ext. 2077, or by e-mail at JASON.HU@linear.com. If I do not hear from you by May 18, 2014, we will consider this change to be approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

Tower Semiconductor Capacity Summary

Plant Address:
Tower Semiconductor Ltd.
Ramat Gavriel Industrial Park
20 Shaul Amor Avenue
P.O. Box 619
Migdal Haemek 23105
Israel
Tel: +972-4-6506611
Fax: +972-4-6547788

Headcount:
1300 employees

Sq. Feet:
- Buildings: 150,000 M^2
- Clean room: 15,000 M^2

Certifications (i.e. ISO-14001, TS16949):
- TS 16949:2009
- ISO 9001:2008
- OHSAS 18001:2007
- SI ISO 27001:2007
- ISO 14001:2004

Floor space Utilization (%utilized):
- Clean room: 15,000 M^2

Land Area:
- 90000 M^2

Fab Capacity:
- The Israeli site (Fab1 and Fab2) has capacity of 720K WPY

LTC3411
TOWER SEMI 0.6um CMOS Reliability Test Data Summary
3/18/2014

• OPERATING LIFE TEST

PACKAGE TYPE	SAMPLE SIZE	OLDEST DATE CODE	NEWEST DATE CODE	K DEVICF HOURS (1) AT +125°C	NUMBER OF (2) FAILURES
SOIC/SOT/MSOP	462	1203	1217	462.00	0
SSOP/TSSOP	231	1147	1150	231.00	0
	693			693.00	0

• HIGHLY ACCELERATED STRESS TEST AT +131°C/85%RH

PACKAGE TYPE	SAMPLE SIZE	OLDEST DATE CODE	NEWEST DATE CODE	K DEVICF HOURS (4) AT +85°C	NUMBER OF FAILURES
SOIC/SOT/MSOP	276	1203	1217	529.92	0
SSOP/TSSOP	180	1147	1150	432.00	0
	456			961.92	0

• PRESSURE COOKER TEST AT 15 PSIG, +121°C

PACKAGE TYPE	SAMPLE SIZE	OLDEST DATE CODE	NEWEST DATE CODE	K DEVICE HOURS	NUMBER OF FAILURES
SOIC/SOT/MSOP	462	1203	1217	119.62	0
SSOP/TSSOP	231	1147	1150	77.62	0
	693			232.84	0

• TEMP CYCLE FROM -65°C to +150°C

PACKAGE TYPE	SAMPLE SIZE	OLDEST DATE CODE	NEWEST DATE CODE	K DEVICE CYCLES	NUMBER OF FAILURES
SOIC/SOT/MSOP	462	1203	1217	462.00	0
SSOP/TSSOP	231	1147	1150	231.00	0
	693			693.00	0

• THERMAL SHOCK FROM -65°C to +150°C

PACKAGE TYPE	SAMPLE SIZE	OLDEST DATE CODE	NEWEST DATE CODE	K DEVICE CYCLES	NUMBER OF FAILURES
SOIC/SOT/MSOP	462	1203	1217	462.00	0
SSOP/TSSOP	231	1147	1150	231.00	0
	693			693.00	0

• HIGH TEMPERATURE BAKE +175°C

PACKAGE TYPE	SAMPLE SIZE	OLDEST DATE CODE	NEWEST DATE CODE	K DEVICE CYCLES	NUMBER OF FAILURES
SOIC/SOT/MSOP	462	1203	1217	462.00	0
SSOP/TSSOP	231	1147	1150	231.00	0
	693			693.00	0

(1) Assumes Activation Energy = 0.7 Electron Volts
(2) Failure Rate Equivalent to +55°C, 60% Confidence Level = 17.05 FITS
(3) Mean Time Between Failures in Years = 6126
(4) Assumes 20X Acceleration from 85°C to +131°C
Note: 1 FIT = 1 Failure in One Billion Hours.