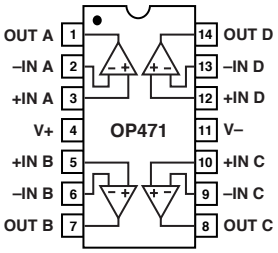
High Speed, Low Noise Quad Operational Amplifier

OP471

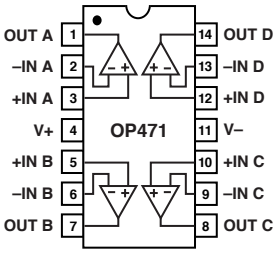
FEATURES
Excellent Speed: 8 V/μs Typ
Low Noise: 11 nV/√Hz @ 1 kHz Max
Unity-Gain Stable
High Gain Bandwidth: 6.5 MHz Typ
Low Input Offset Voltage: 0.8 mV Max
Low Offset Voltage Drift: 4 μV/°C Max
High Gain: 500 V/mV Min
Outstanding CMR: 105 dB Min
Industry Standard Quad Pinouts

PIN CONFIGURATIONS

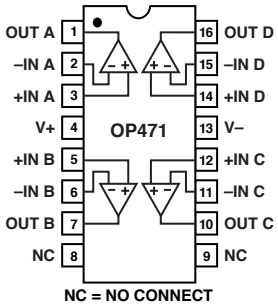
14-Lead Hermetic Dip (Y-Suffix)



14-Lead Plastic Dip (P-Suffix)



16-Lead SOIC (S-Suffix)



GENERAL DESCRIPTION

The OP471 is a monolithic quad op amp featuring low noise, 11 nV/√Hz Max @ 1 kHz, excellent speed, 8 V/μs typical, a gain bandwidth of 6.5 MHz, and unity-gain stability.

The OP471 has an input offset voltage under 0.8 mV and an input offset voltage drift below 4 μV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP471 is over 500,000 into a 10 kΩ load ensuring outstanding gain accuracy and linearity. The input bias current is under 25 nA limiting errors due to signal source resistance. The OP471's CMR of over 105 dB and PSRR of under 5.6 μV/V significantly reduce errors caused by ground noise and power supply fluctuations.

The OP471 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, quad buffers and low-noise active filters.

The OP471 conforms to the industry standard 14-lead DIP pinout. It is pin-compatible with the LM148/LM149, HA4741, RM4156, MC33074, TL084 and TL074 quad op amps and can be used to upgrade systems using these devices.

For applications requiring even lower voltage noise the OP470 with a voltage density of 5 nV/√Hz Max @ 1 kHz is recommended.

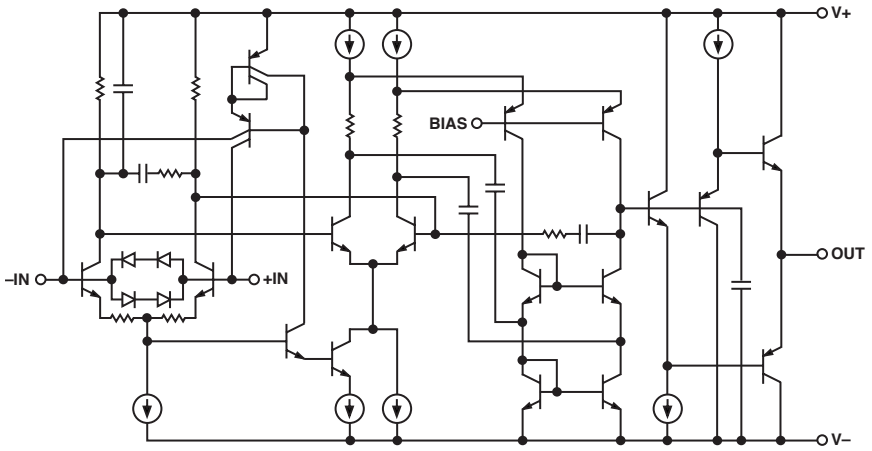


Figure 1. Simplified Schematic

REV. A

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OP471–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP471E Min	OP471E Typ	OP471E Max	OP471F Min	OP471F Typ	OP471F Max	OP471G Min	OP471G Typ	OP471G Max	Unit
Input Offset Voltage	V_{OS}			0.25	0.8		0.5	1.5		1.0	1.8	mV
Input Offset Current	I_{OS}	V_{CM} = 0 V		4	10		7	20		12	30	nA
Input Bias Current	I_B	V_{CM} = 0 V		7	25		15	50		25	60	nA
Input Noise Voltage[1]	e_n p-p	0.1 Hz to 10 Hz		250	500		250	500		250	500	nV p–p
Input Noise Voltage Density[2]	e_n	f_O = 10 Hz f_O = 100 Hz f_O = 1 kHz		9 7 6.5	16 12 11		9 7 6.5	16 12 11		9 7 6.5	16 12 11	nV/√Hz nV/√Hz nV/√Hz
Input Noise Current Density	i_n	f_O = 10 Hz f_O = 100 Hz f_O = 1 kHz		1.7 0.7 0.4			1.7 0.7 0.4			1.7 0 7 0.4		pA√Hz pA√Hz pA√Hz
Large-Signal Voltage Gain	A_{VO}	V = ±10 V R_L = 10 kΩ R_L = 2 kΩ	 500 350	 700 550		 300 175	 500 275		 300 175	 500 275		 V/mV V/mV
Input Voltage Range[3]	IVR		±11	±12		±11	±12		±11	±12		V
Output Voltage Swing	V_O	$R_L \geq$ 2 kΩ	±12	±13		±12	±13		±12	±13		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	105	120		95	115		95	115		dB
Power Supply Rejection Ratio	PSRR	V_S = 4.5 V to 18 V		1	5.6		5.6	17.8		5.6	17.8	µV/V
Slew Rate	SR		6.5	8		6.5	8		6.5	8		V/µs
Supply Current (All Amplifiers)	I_{SY}	No Load		9.2	11		9.2	11		9.2	11	mA
Gain Bandwidth Product	GBW	Av = 10		6.5			6.5			6.5		MHz
Channel Separation[1]	CS	V_O = 20 V p-p f_O = 10 Hz	125	150		125	150		125	150		dB
Input Capacitance	C_{IN}			2.6			2.6			2.6		pF
Input Resistance Differential-Mode	R_{IN}			1.1			1.1			1.1		MΩ
Input Resistance Common-Mode	R_{INCM}			11			11			11		GΩ
Settling Time	t_S	A_V = 1 To 0.1% To 0.01 %	 	 4.5 7.5		 	 4.5 7.5		 	 4.5 7.5		 µs µs

NOTES
[1]Guaranteed but not 100% tested.
[2]Sample tested.
[3]Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, –25°C ≤ T_A ≤ 85°C for OP471E/F, –40°C ≤ T_A ≤ 85° for OP471G, unless otherwise noted.)

Parameter	Symbol	Conditions	OP471E Min	OP471E Typ	OP471E Max	OP471F Min	OP471F Typ	OP471F Max	OP471G Min	OP471G Typ	OP471G Max	Unit
Input Offset Voltage	V_{OS}			0.3	1.1		0.6	2.0		1.2	2.5	mV
Average Input Offset Voltage Drift	TCV_{OS}			1	4		2	7		4		µV/°C
Input Offset Current	los	V_{CM} = 0 V		5	20		8	40		20	50	nA
Input Bias Current	I_B	V_{CM} = 0 V		13	50		25	70		40	75	nA
Large-Signal Voltage Gain	Avo	V_O = ±10 V R_L = 10 kΩ R_L = 2 kΩ	 375 250	 600 400		 200 125	 400 200		 200 125	 400 200		V/mV
Input Voltage Range*	IVR		±11	±12		±11	±12		±11	±12		V
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12	±13		±12	±13		±12	±13		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	100	115		90	110		90	110		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		3.2	10		18	31.6		18	31.6	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load		9.3	11		9.3	11		9.3	11	mA

*Guaranteed by CMR test.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Differential Input Voltage[2] . . . . . ±1.0 V
Differential Input Current[2] . . . . . ±25 mW
Input Voltage . . . . . Supply Voltage
Output Short-Circuit Duration . . . . . Continuous
Storage Temperature Range
P, Y-Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C
Junction Temperature (T_j) . . . . . –65°C to +150°C
Operating Temperature Range
OP471E, OP471F . . . . . –25°C to +85°C
OP471G . . . . . –40°C to +85°C

NOTES
[1]Absolute Maximum Ratings apply to packaged parts, unless otherwise noted.
[2]The OP471's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0 V, the input current should be limited to ±25 mA.

Package Type	θ_{JA}*	θ_{JC}	Unit
14-Lead Hermetic DIP(Y)	94	10	°C/W
14-Lead Plastic DIP(P)	76	33	°C/W
16-Lead SOIC (S)	88	23	°C/W

*θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, CERDIP, PDIP packages; θ_{JA} is specified for device soldered to printed circuit board for SO packages.

ORDERING GUIDE

T_A = 25°C V_{OS} MAX (µV)	Package Options		Operating Temperature Range
	14-Lead CERDIP	Plastic	
800	OP471EY		IND
1,500	OP471FY*		IND
1,800		OP471GP	XIND
1,800		OP471GS	XIND

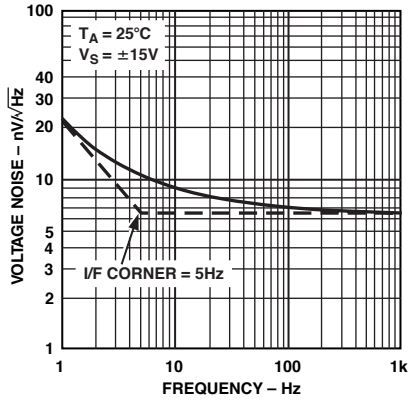
*Not for new design. Obsolete April 2002.

For military processed devices, please refer to the standard microcircuit drawing (SMD) available at
www.dscc.dla.mil/programs/milspec/default.asp
5962-88565022A - OP471ARCMDA
5962-88565023A - OP471ATCMDA
5962-8856502CA - OP471AYMDA

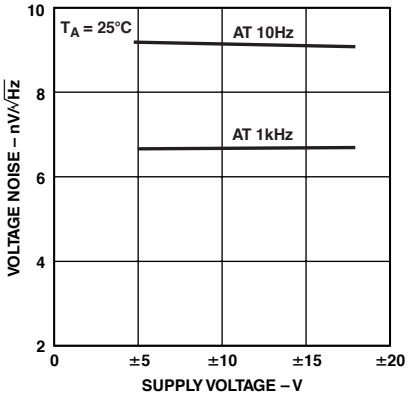
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP471 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

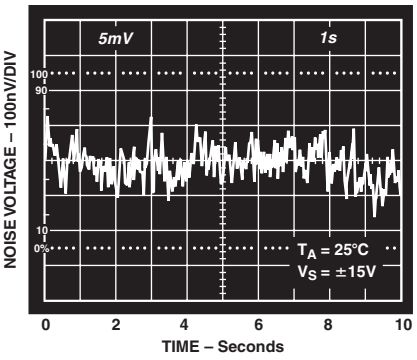
OP471–Typical Performance Characteristics



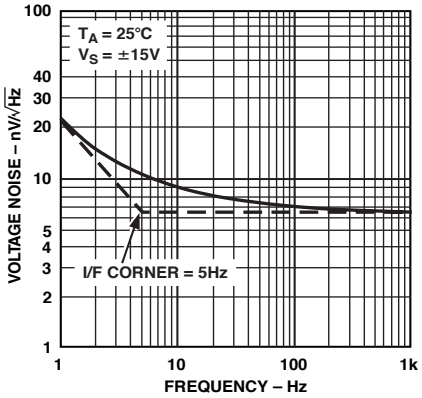
TPC 1. Voltage Noise Density vs. Frequency



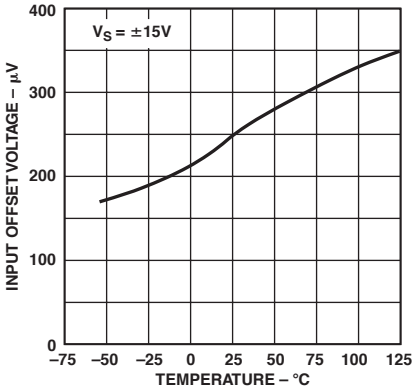
TPC 2. Voltage Noise Density vs. Supply Voltage



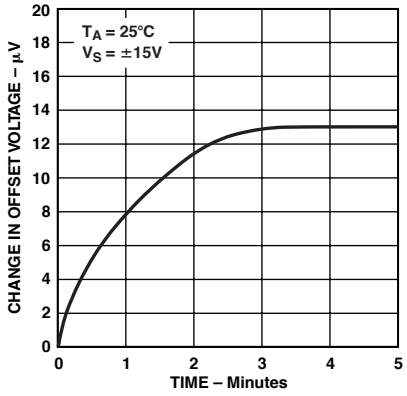
TPC 3. 0.1 Hz to 10 Hz Noise



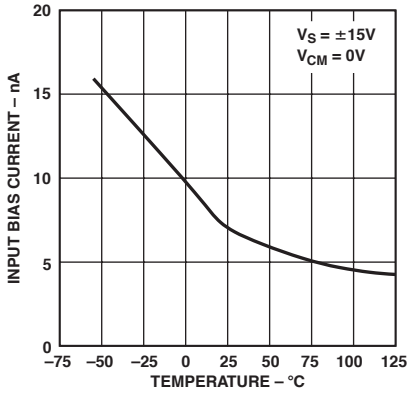
TPC 4. Current Noise Density vs. Frequency



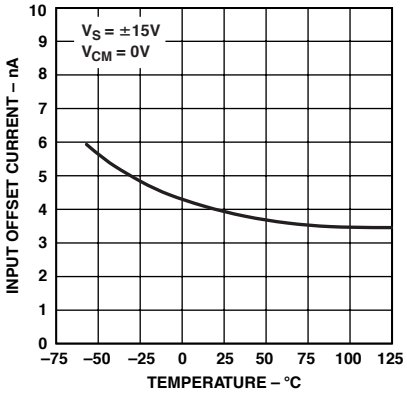
TPC 5. Input Offset Voltage vs. Temperature



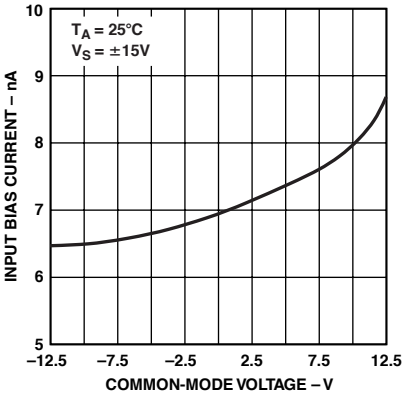
TPC 6. Warm-Up Offset Voltage Drift



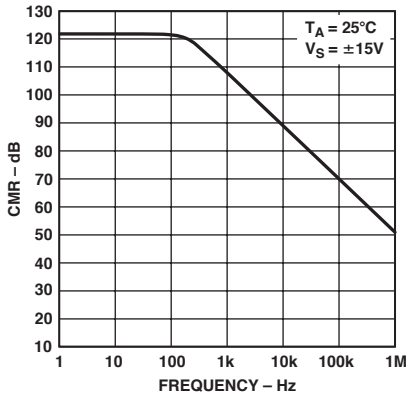
TPC 7. Input Bias Current vs. Temperature



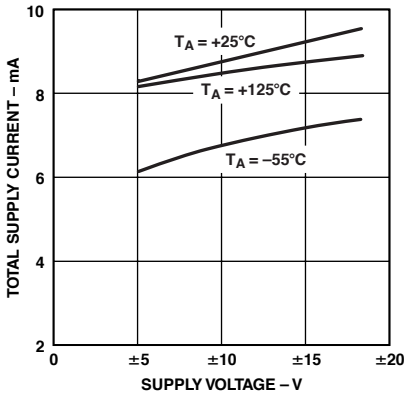
TPC 8. Input Offset Current vs. Temperature



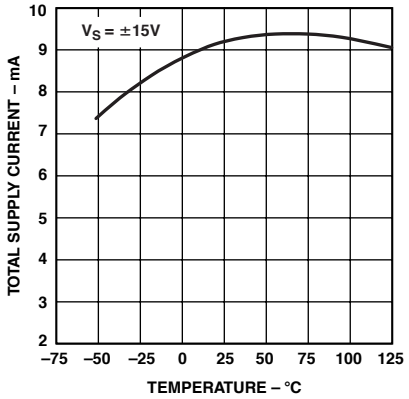
TPC 9. Input Bias Current vs. Common-Mode Voltage



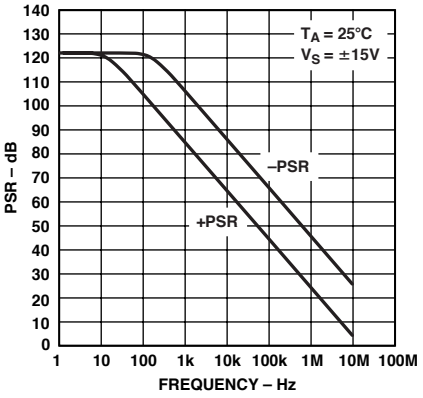
TPC 10. CMR vs. Frequency



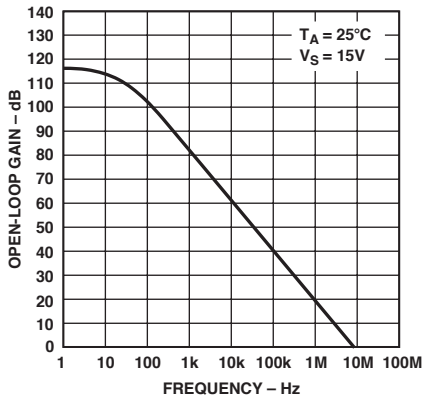
TPC 11. Total Supply Current vs. Supply Voltage



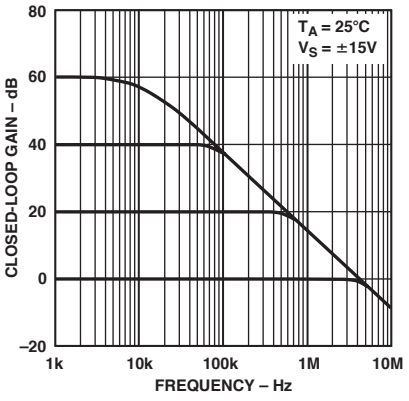
TPC 12. Total Supply Current vs. Temperature



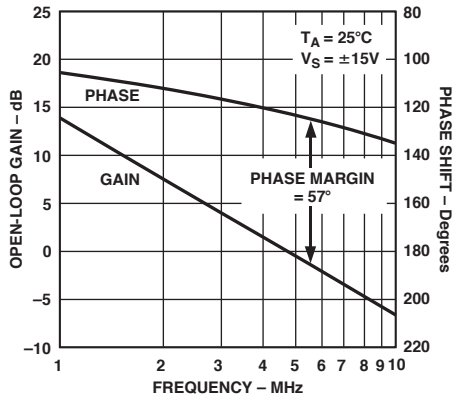
TPC 13. PSR vs. Frequency



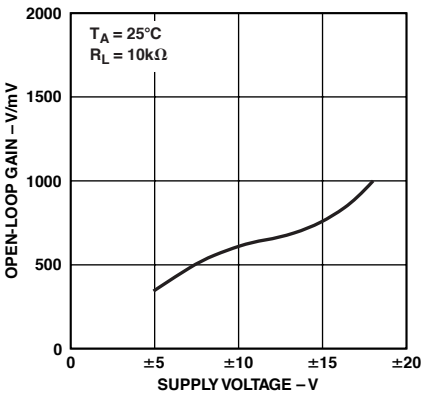
TPC 14. Open-Loop Gain vs. Frequency



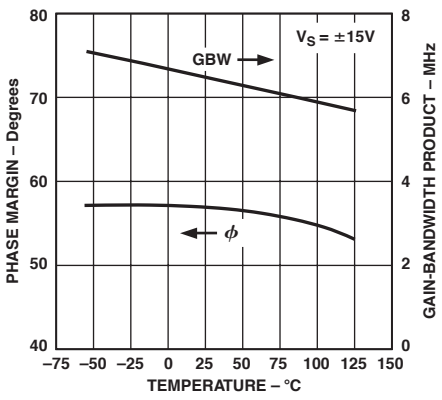
TPC 15. Closed-Loop Gain vs. Frequency



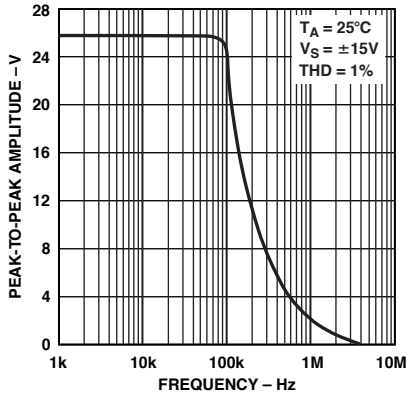
TPC 16. Open-Loop Gain, Phase Shift vs. Frequency



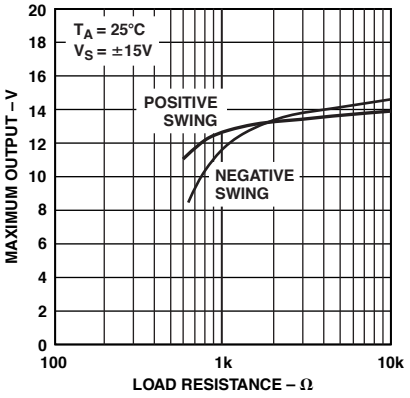
TPC 17. Open-Loop Gain vs. Supply Voltage



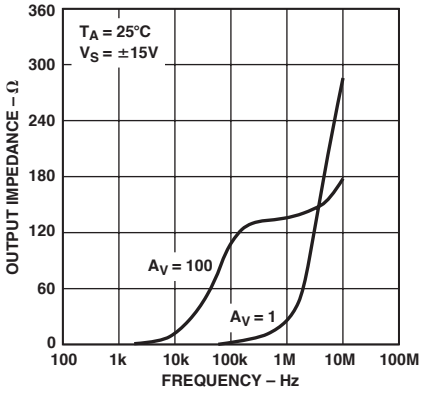
TPC 18. Gain-Bandwidth Product, Phase Margin vs. Temperature



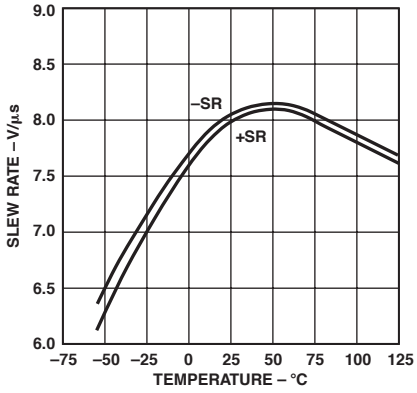
TPC 19. Maximum Output Swing vs. Frequency



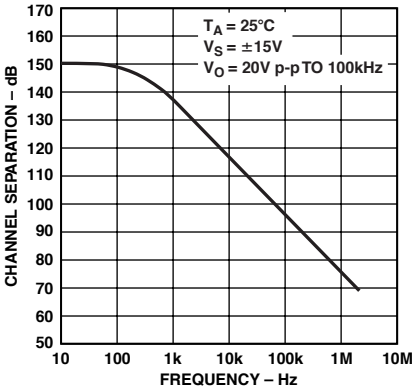
TPC 20. Maximum Output Voltage vs. Load Resistance



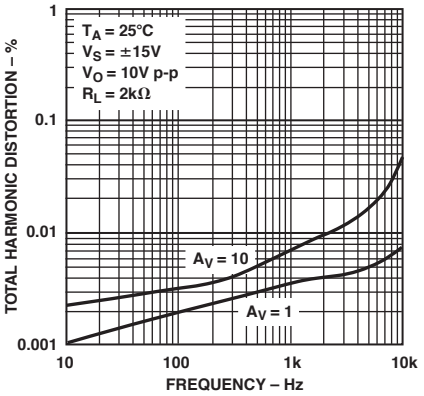
TPC 21. Closed-Loop Output Impedance vs. Frequency



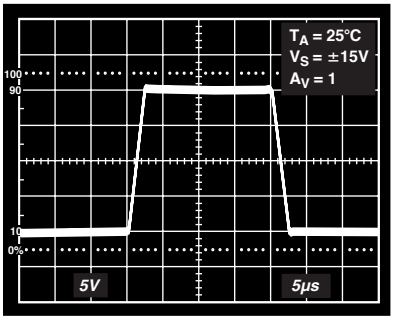
TPC 22. Slew Rate vs. Temperature



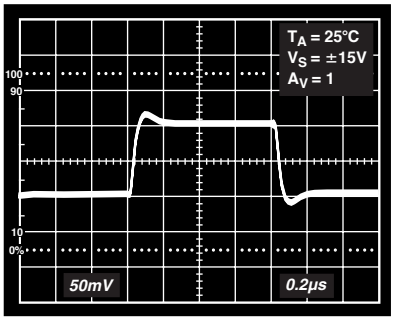
TPC 23. Channel Separation vs. Frequency



TPC 24. Total Harmonic Distortion vs. Frequency



TPC 25. Large-Signal Transient Response



TPC 26. Small-Signal Transient Response

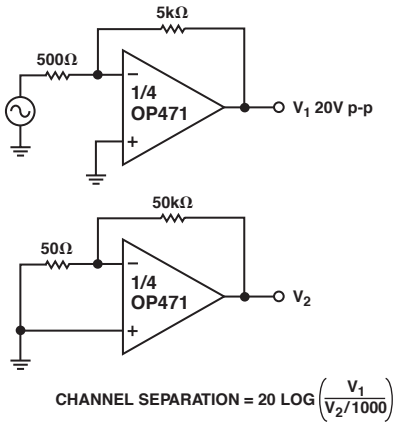


Figure 2. Channel Separation Test Circuit

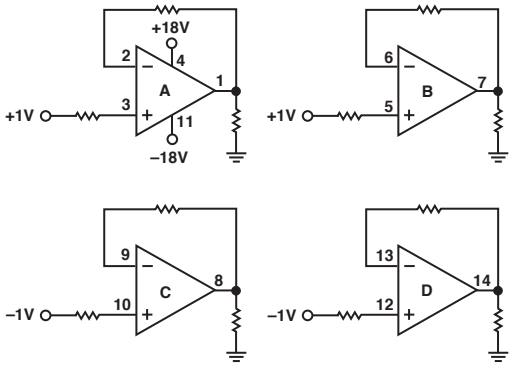


Figure 3. Burn-In Circuit

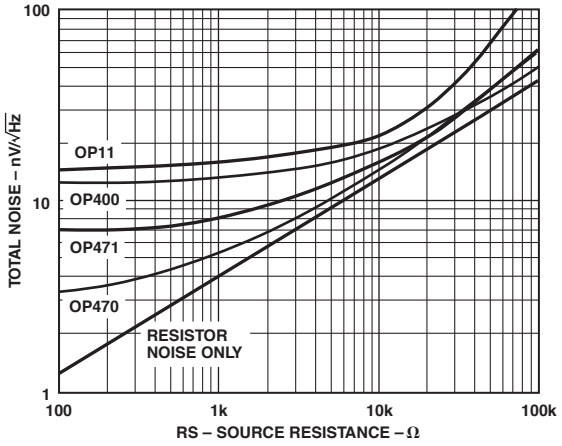


Figure 4. Total Noise vs. Source Resistance (Including Resistor Noise) at 1 kHz

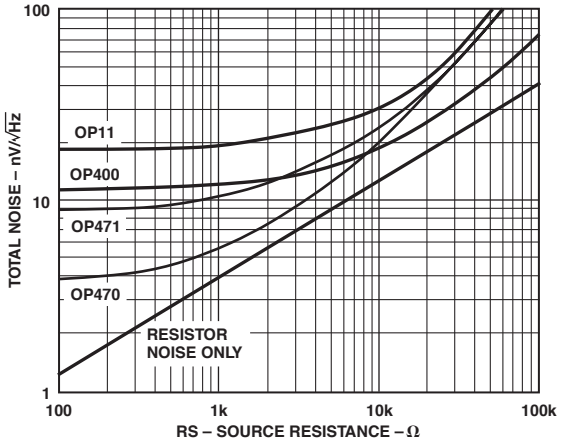


Figure 5. Total Noise vs. Source Resistance (Including Resistor Noise) at 10 Hz

APPLICATIONS INFORMATION

Voltage and Current Noise

The OP471 is a very low-noise quad op amp, exhibiting a typical voltage noise of only 6.5 $\overline{\text{Hz}}$ @ 1 kHz. The low noise characteristic of the OP471 is, in part, achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the OP471 is gained at the expense of current noise performance which is typical for low noise amplifiers.

To obtain the best noise performance in a circuit, it is vital to understand the relationship between voltage noise (e_n), current noise (i_n), and resistor noise (e_t).

Total Noise and Source Resistance

The total noise of an op amp can be calculated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 + (e_t)^2}$$

where:

E_n = total input referred noise
e_n = op amp voltage noise
i_n = op amp current noise
e_t = source resistance thermal noise
R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 4 shows the relationship between total noise at 1 kHz and source resistance. For R_S < 1 kΩ the total noise is dominated by the voltage noise of the OP471. As R_S rises above 1 kΩ, total noise increases and is dominated by resistor noise rather than by voltage or current noise of the OP471. When R_S exceeds 20 kΩ, current noise of the OP471 becomes the major contributor to total noise.

Figure 5 also shows the relationship between total noise and source resistance, but at 10 Hz. Total noise increases more quickly than shown in Figure 4 because current noise is inversely proportional to the square root of frequency. In Figure 5, current noise of the OP471 dominates the total noise when R_S > 5 kΩ.

From Figures 4 and 5, it can be seen that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP400, with lower current noise than the OP471, will provide lower total noise.

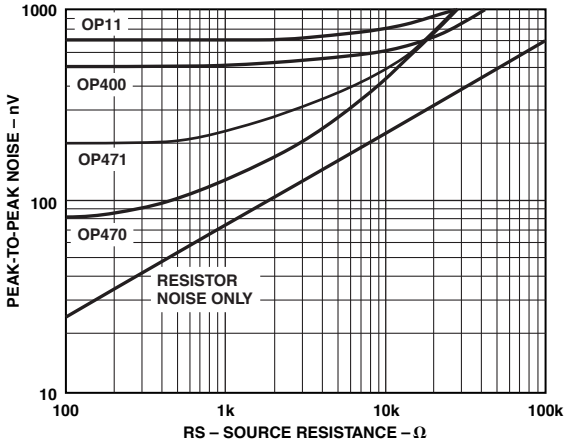


Figure 6. Peak-to-Peak Noise (0.1 Hz to 10 Hz) vs. Source Resistance (Includes Resistor Noise)

Figure 6 shows peak-to-peak noise versus source resistance over the 0.1 Hz to 10 Hz range. Once again, at low values of R_S, the voltage noise of the OP471 is the major contributor to peak-to-peak noise. Current noise becomes the major contributor as R_S increases. The crossover point between the OP471 and the OP400 for peak-to-peak noise is at R_S = 17 Ω.

The OP470 is a lower noise version of the OP471, with a typical noise voltage density of 3.2 nV/√Hz @ 1 kHz. The OP470 offers lower offset voltage and higher gain than the OP471, but is a slower speed device, with a slew rate of 2 V/μs compared to a slew rate of 8 V/μs for the OP471.

For reference, typical source resistances of some signal sources are listed in Table I.

TABLE I.

Device	Source Impedance	Comments
Strain gauge	< 500 Ω	Typically used in low-frequency applications.
Magnetic tapehead	< 1,500 Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP471 I_B can be neglected.
Magnetic phonograph cartridges	< 1,500 Ω	Similar need for low I_B in direct coupled applications. OP471 will not introduce any self -magnetization problem.
Linear variable differential transformer	< 1,500 Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400 Hz to 5 kHz.

*For further information regarding noise calculations, see "Minimization of Noise in Op Amp Applications," Application Note AN-15.

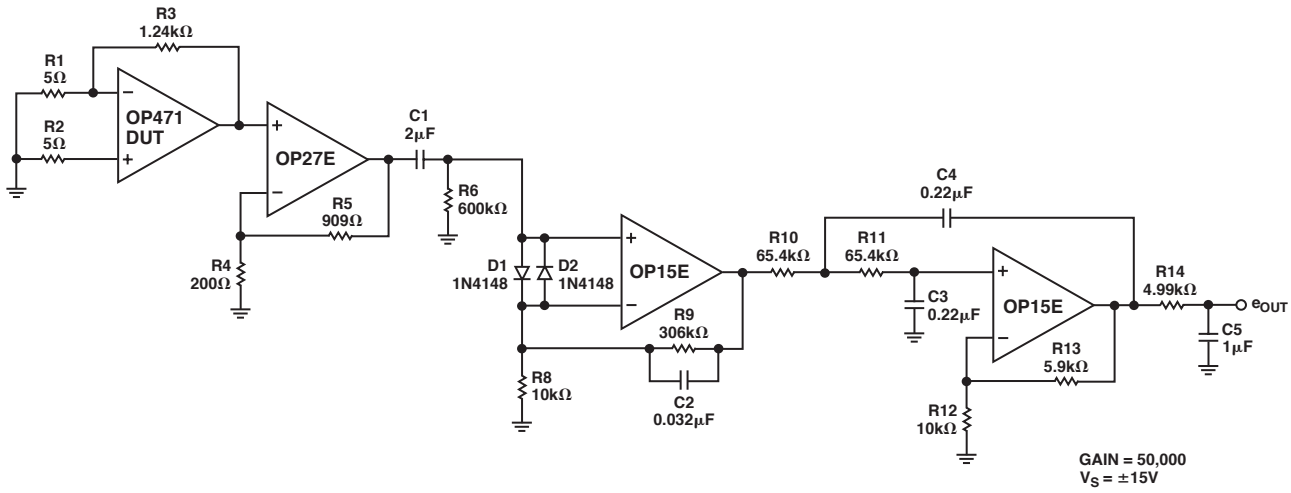


Figure 7. Peak-to-Peak Voltage Noise Test Circuit (0.1 Hz to 10 Hz)

Noise Measurements - Peak-to-Peak Voltage Noise
The circuit of Figure 7 is a test setup for measuring peak-to-peak voltage noise. To measure the 500 nV peak-to-peak noise specification of the OP471 in the 0.1 Hz to 10 Hz range, the following precautions must be observed:

1. The device must be warmed up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 13 µV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
2. For similar reasons, the device must be well-shielded from air currents. Shielding also minimizes thermocouple effects.
3. Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.
4. The test time to measure 0.1 Hz to 10 Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 8, the 0.1 Hz corner is defined by only one pole. The test time of 10 seconds acts as an additional pole to eliminate noise contribution from the frequency band below 0.1 Hz.
5. A noise voltage density test is recommended when measuring noise on a large number of units. A 10 Hz noise voltage density measurement will correlate well with a 0.1 Hz to 10 Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.
6. Power should be supplied to the test circuit by well bypassed, low noise supplies, e.g, batteries. These will minimize output noise introduced through the amplifier supply pins.

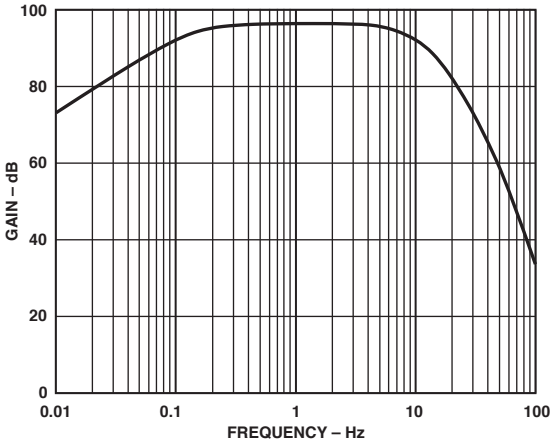


Figure 8. 0.1 Hz to 10 Hz Peak-to-Peak Voltage Noise Test Circuit Frequency Response

Noise Measurement - Noise Voltage Density
The circuit of Figure 9 shows a quick and reliable method of measuring the noise voltage density of quad op amps. Each individual amplifier is series connected and is in unity-gain, save the final amplifier which is in a noninverting gain of 101. Since the ac noise voltages of each amplifier are uncorrelated, they add in rms fashion to yield:

$$e_{OUT} = 101\left(\sqrt{e_{nA}^2 + e_{nB}^2 + e_{nC}^2 + e_{nD}^2}\right)$$

The OP471 is a monolithic device with four identical amplifiers. The noise voltage density of each individual amplifier will match, giving:

$$e_{OUT} = 101\left(\sqrt{4e_n^2}\right) = 101\left(2e_n\right)$$

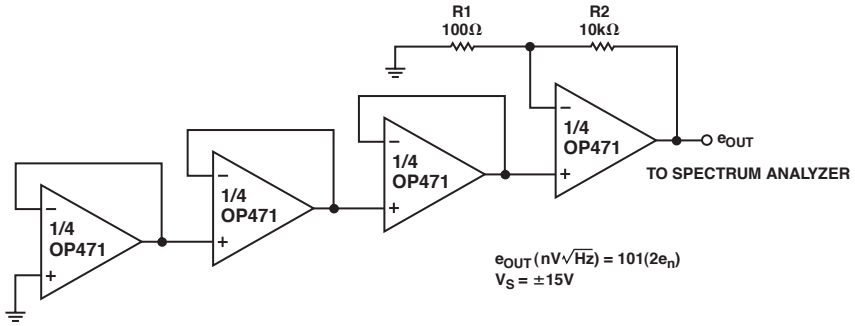


Figure 9. Noise Voltage Density Test Circuit

Noise Measurement - Current Noise Density
The test circuit shown in Figure 10 can be used to measure current noise density. The formula relating the voltage output to current noise density is:

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - \left(40nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

G = gain of 10,000
R_S = 100 kΩ source resistance

Capacative Load Driving and Power Supply Considerations
The OP471 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP471.

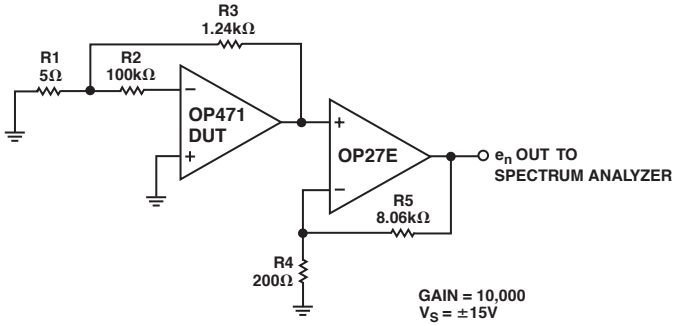


Figure 10. Current Noise Density Test Circuit

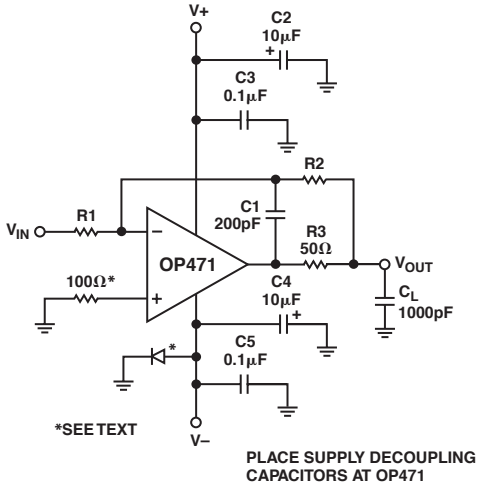


Figure 11. Driving Large Capacitive Loads

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a lowpass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 11. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 11 are for load capacitances of up to 1,000 pF when used with the OP471.

In applications where the OP471's inverting or noninverting inputs are driven by a low source impedance (under 100 Ω) or connected to ground, if V+ is applied before V–, or when V– is disconnected, excessive parasitic currents will flow.

Most applications use dual tracking supplies and with the device supply pins properly bypassed, power-up will not present a problem. A source resistance of at least 100 Ω in series with all inputs (Figure 11) will limit the parasitic currents to a safe level if V– is disconnected. It should be noted that any source resistance, even 100 Ω, adds noise to the circuit. Where noise is required to be kept at a minimum, a germanium or Schottky diode can be used to clamp the V– pin and eliminate the parasitic current flow instead of using series limiting resistors. For most applications, only one diode clamp is required per board or system.

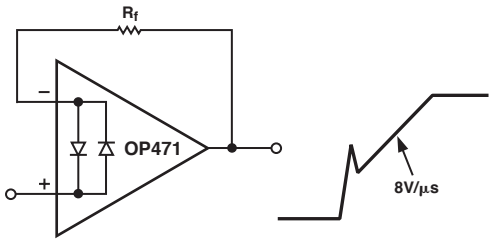


Figure 12. Pulsed Operation

Unity-Gain Buffer Applications
When $R_f \leq 100\ \Omega$ and the input is driven with a fast, large signal pulse (>1 V), the output waveform will look as shown in Figure 12.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\ \Omega$, the output is capable of handling the current requirements ($I_L \leq 20$ mA at 10 V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 3$ kΩ, a pole created by R_f and the amplifier's input capacitance (2.6 pF) creates additional phase shift and reduces phase margin. A small capacitor (20 pF to 50 pF) in parallel with R_f helps eliminate this problem.

APPLICATIONS

Low Noise Amplifier
A simple method of reducing amplifier noise by paralleling amplifiers is shown in Figure 13. Amplifier noise, depicted in Figure 14, is around 5 nV/√Hz @ 1 kHz (R.T.I.). Gain for each paralleled amplifier and the entire circuit is 100. The 200 Ω resistors limit circulating currents and provide an effective output resistance of 50 Ω. The amplifier is stable with a 10 nF capacitive load and can supply up to 30 mA of output drive.

High-Speed Differential Line Driver

The circuit of Figure 15 is a unique line driver widely used in professional audio applications. With ±18 V supplies, the line driver can deliver a differential signal of 30 V p-p into a 1.5 kΩ load. The output of the differential line driver looks exactly like a transformer. Either output can be shorted to ground without changing the circuit gain of 5, so the amplifier can easily be set for inverting, noninverting, or differential operation. The line driver can drive unbalanced loads, like a true transformer.

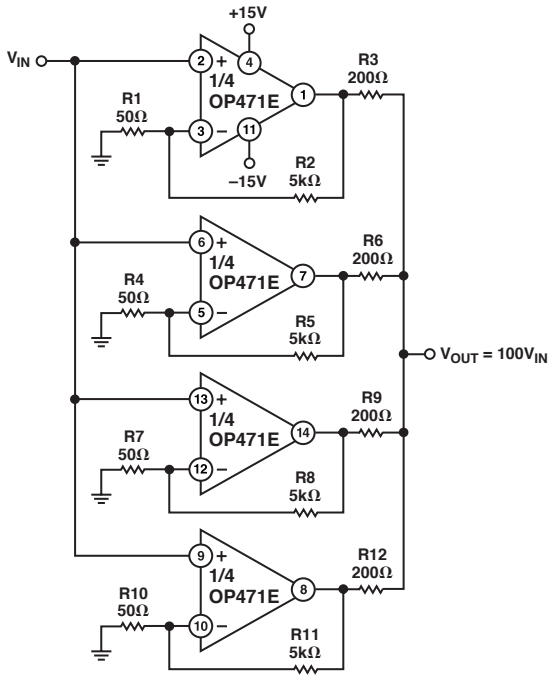


Figure 13. Low-Noise Amplifier

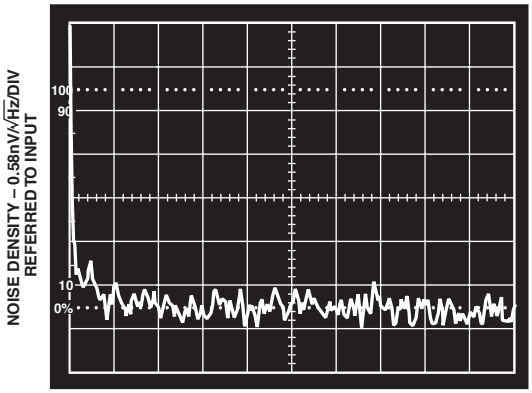


Figure 14. Noise Density of Low-Noise Amplifier, G = 100

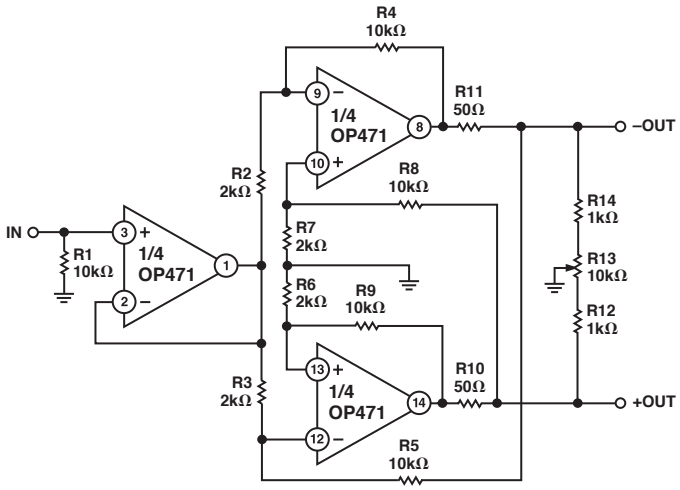


Figure 15. High-Speed Differential Line Driver

High-Output Amplifier

The amplifier shown in Figure 16 is capable of driving 20 V p-p into a floating 400 Ω load. Design of the amplifier is based on a bridge configuration. A1 amplifies the input signal and drives the load with the help of A2. Amplifier A3 is a unity-gain inverter which drives the load with help from A4. Gain of the high output amplifier with the component values shown is 10, but can easily be changed by varying R1 or R2.

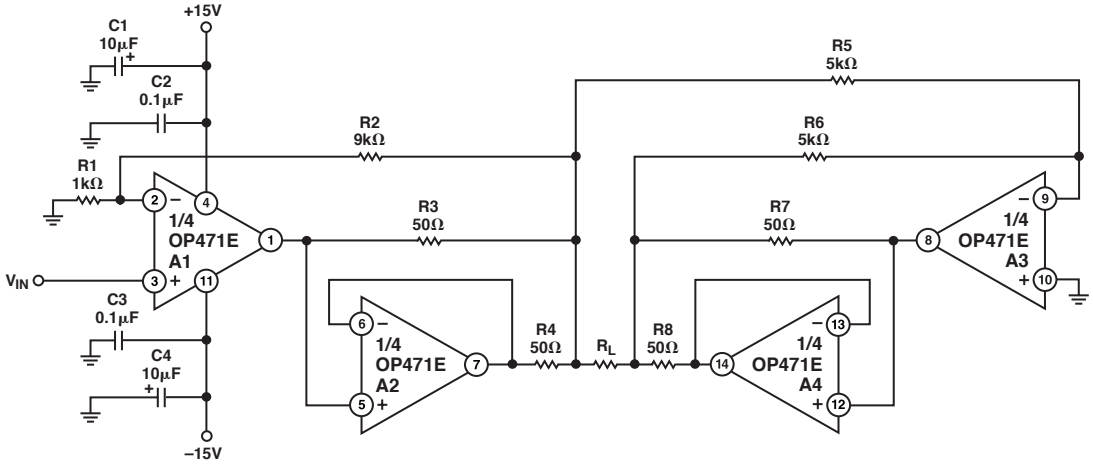


Figure 16. High-Output Amplifier

Quad Programmable Gain Amplifier

The combination of the quad OP471 and the DAC8408, a quad 8-bit CMOS DAC, creates a space-saving quad programmable gain amplifier. The digital code present at the DAC, which is easily set by a microprocessor, determines the ratio between the fixed DAC feedback resistor and the impedance the DAC ladder presents to the op amp feedback loop. Gain of each amplifier is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{256}{n}$$

where n equals the decimal equivalent of the 8-bit digital code present at the DAC. If the digital code present at the DAC consists of all zeros, the feedback loop will be open causing the op amp output to saturate. The 20 MΩ resistors placed in parallel with the DAC feedback loop eliminates this problem with a very small reduction in gain accuracy.

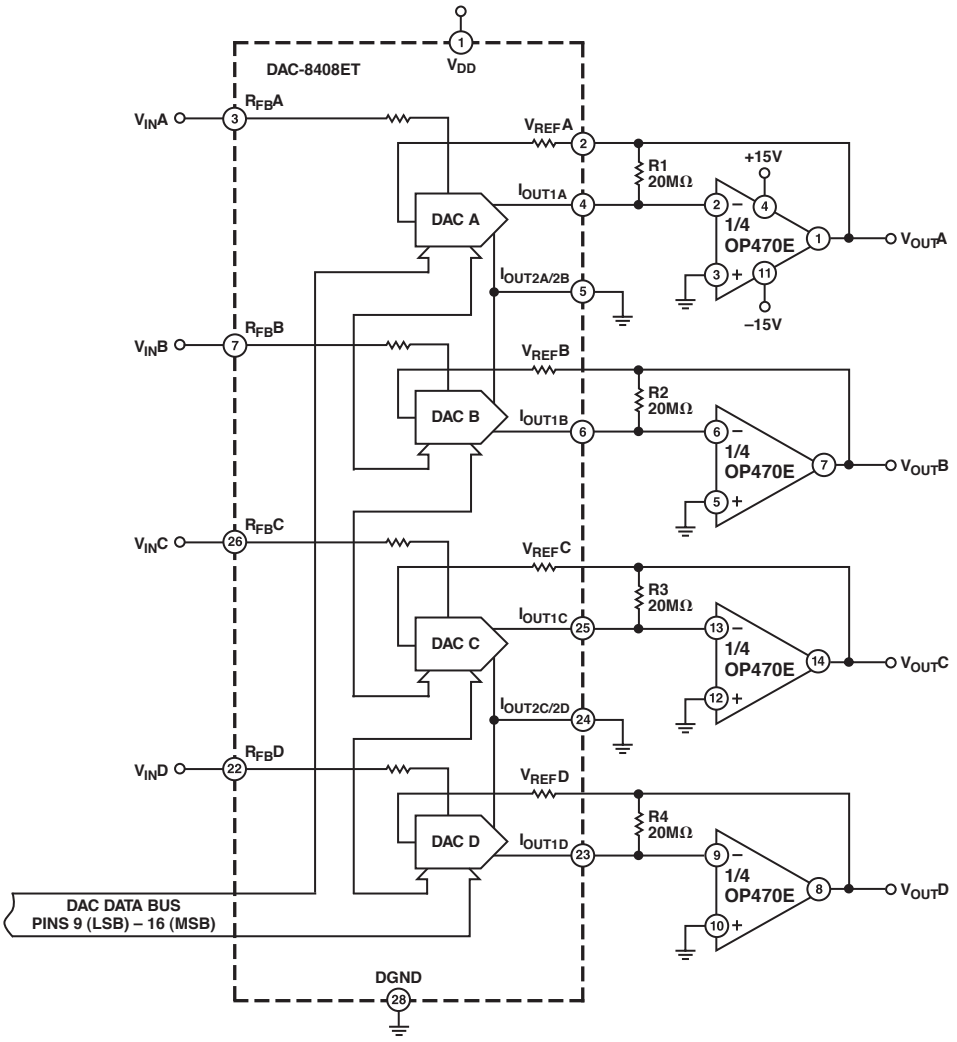


Figure 17. Quad Programmable Gain Amplifier

Low Phase Error Amplifier

The simple amplifier depicted in Figure 18 utilizes monolithic matched operational amplifiers and a few resistors to substantially reduce phase error compared to conventional amplifier designs. At a given gain, the frequency range for a specified phase accuracy is over a decade greater than for a standard single op amp amplifier.

The low phase error amplifier performs second-order frequency compensation through the response of op amp A2 in the feedback loop of A1. Both op amps must be extremely well matched in frequency response. At low frequencies, the A1 feedback loop forces $V_2/(K1 + 1) = V_{IN}$. The A2 feedback loop forces Vo/(K1 +1) = $V_2/(K1 + 1)$ yielding an overall transfer function of V_O/V_{IN} = K1 + 1. The dc gain is determined by the resistor divider at the output, V_O, and is not directly affected by the resistor divider around A2. Note that similar to a conventional single op amp amplifier, the dc gain is set by resistor ratios only. Minimum gain for the low phase error amplifier is 10.

Figure 19 compares the phase error performance of the low phase error amplifier with a conventional single op amp amplifier and a cascaded two-stage amplifier. The low phase error amplifier shows a much lower phase error, particularly for frequencies where $\omega/\beta\omega_T < 0.1$. For example, phase error of –0.1° occurs at 0.002 $\omega/\beta\omega_T$ for the single op amp amplifier, but at 0.11 $\omega/\beta\omega_T$ for the low phase error amplifier.

For more detailed information on the low phase error amplifier, see Application Note AN-107.

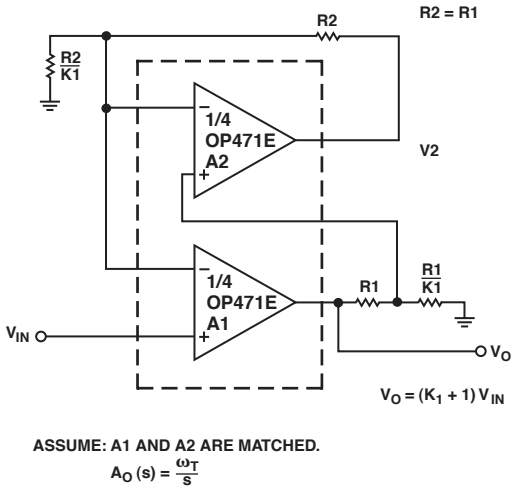


Figure 18. Low Phase Error Amplifier

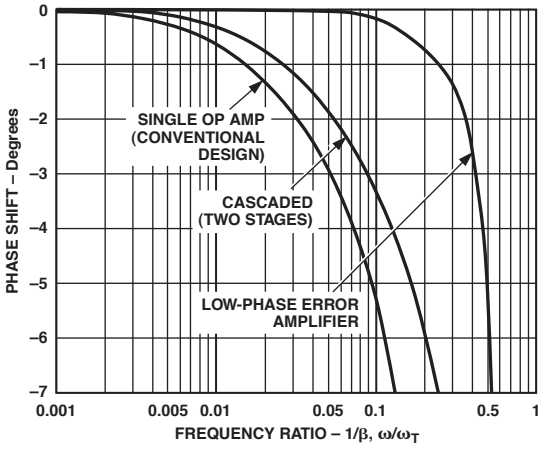


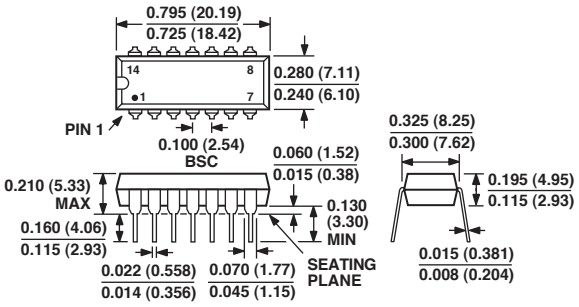
Figure 19. Phase Error Comparison

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

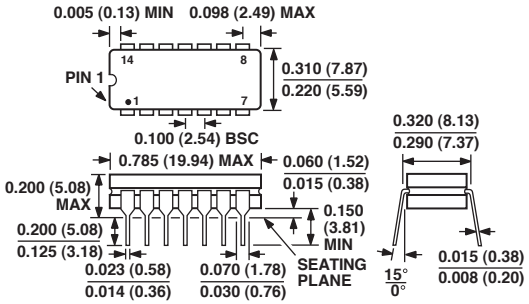
14-Lead PDIP Package

(N-14)



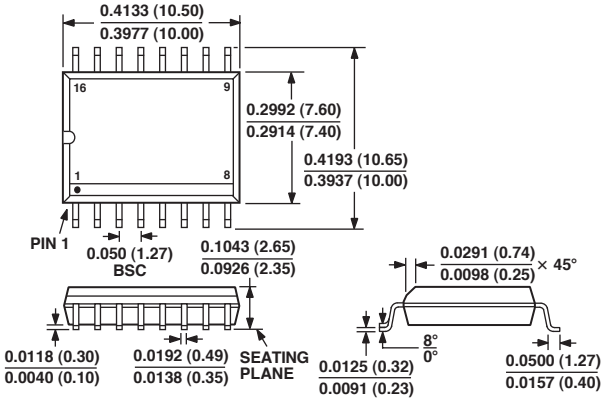
14-Lead CERDIP Package

(Q-14)



16-Lead SOIC Package

(R-16)



Revision History

Location	Page
Data Sheet changed from REV. 0 to REV. A.	
Edits to FEATURES	1
Edits to ELECTRICAL CHARACTERISTICS	2
Edits to ABSOLUTE MAXIMUM RATINGS	3
Edits to ORDERING GUIDE	3
Deleted DICE CHARACTERISTICS	5
Deleted WAFER TEST CHARACTERISTICS	5

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