

## EL7581

### 3-Channel DC/DC Converter

FN7100  
 Rev 5.00  
 March 9, 2006

The EL7581 is a 3-channel DC/DC converter IC which is designed primarily for use in TFT/LCD applications. It features a PWM boost converter with 2.7V to 14V input capability and 5V to 17V output, which powers the column drivers and provides up to 720mA @12V, 570mA @ 15V from 5V input. A pair of charge pump control circuits provide regulated outputs of  $V_{ON}$  and  $V_{OFF}$  supplies at 8V to 40V and -5V to -40V, respectively, each at up to 60mA.

The EL7581 features adjustable switching frequency, adjustable soft start, and a separate output  $V_{ON}$  enable control to allow selection of supply start-up sequence. An over-temperature feature is provided to allow the IC to be automatically protected from excessive power dissipation.

The EL7581 is available in a 20 Ld HTSSOP package and is specified for operation over the full  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range.

### Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL7581IRE	7581IRE	-	20 Ld HTSSOP	MDP0048
EL7581IRE-T7	7581IRE	7"	20 Ld HTSSOP	MDP0048
EL7581IRE-T13	7581IRE	13"	20 Ld HTSSOP	MDP0048
EL7581IREZ (Note)	7581IREZ	-	20 Ld HTSSOP (Pb-Free)	MDP0048
EL7581IREZ-T7 (Note)	7581IREZ	7"	20 Ld HTSSOP (Pb-Free)	MDP0048
EL7581IREZ-T13 (Note)	7581IREZ	13"	20 Ld HTSSOP (Pb-Free)	MDP0048

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

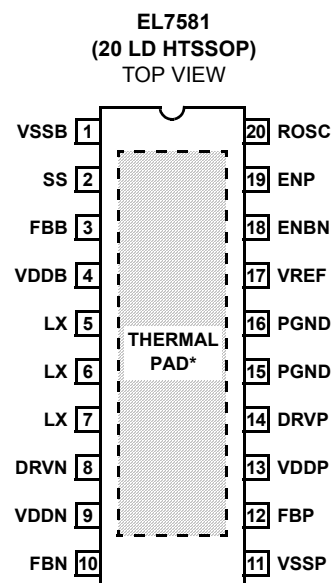
### Features

- TFT/LCD display supply
  - Boost regulator
  - $V_{ON}$  charge pump
  - $V_{OFF}$  charge pump
- 2.7V to 14V  $V_{IN}$  supply
- $5\text{V} < V_{BOOST} < 17\text{V}$
- $5\text{V} < V_{ON} < 40\text{V}$
- $-40\text{V} < V_{OFF} < 0\text{V}$
- $V_{BOOST} = 12\text{V} @ 720\text{mA}$
- $V_{BOOST} = 15\text{V} @ 570\text{mA}$
- High frequency, small inductor DC/DC boost circuit
- Over 90% efficient DC/DC boost converter capability
- Adjustable frequency
- Adjustable soft-start
- Adjustable outputs
- Small parts count
- Pb-free plus anneal available (RoHS compliant)

### Applications

- TFT-LCD panels
- PDAs

### Pinout



\*Refer to PCB layout guideline.

**Absolute Maximum Ratings** (T<sub>A</sub> = 25°C)

V <sub>IN</sub> Input Voltage	14V	Storage Temperature	-65°C to +150°C
V <sub>DDB</sub> , V <sub>DDP</sub> , V <sub>DDN</sub>	18V	Die Junction Temperature	125°C
LX Voltage	18V	Power Dissipation	See Curves
Maximum Continuous Output Current	1A	Operating Ambient Temperature	-40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T<sub>J</sub> = T<sub>C</sub> = T<sub>A</sub>

**Electrical Specifications** V<sub>IN</sub> = 3.3V, V<sub>BOOST</sub> = 12V, R<sub>OSC</sub> = 100kΩ, T<sub>A</sub> = 25°C Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
<b>DC/DC BOOST CONVERTER</b>						
IQ1_B	Quiescent Current - Shut-down	ENBN = ENP = 0V		0.8	10	μA
IQ2_B	Quiescent Current - Switching	ENBN = V <sub>DDB</sub>		4.8	8	mA
V(FBB)	Feedback Voltage		1.275	1.300	1.325	V
V <sub>REF</sub>	Reference Voltage		1.260	1.310	1.360	V
V <sub>ROSC</sub>	Oscillator Set Voltage		1.260	1.325	1.390	V
I(FBB)	Feedback Input Bias Current			0.1		μA
V <sub>DDB</sub>	Boost Converter Supply Range		2.7		17	V
D <sub>MAX</sub>	Maximum Duty Cycle		85	92		%
I(LX) <sub>MAX</sub>	Peak Internal FET Current			2.75		A
R <sub>DS-ON</sub>	Switch On Resistance	at V <sub>BOOST</sub> = 10V, I(LX) total = 500mA		0.15		Ω
I <sub>LEAK-SWITCH</sub>	Switch Leakage Current	I(LX) total			2	μA
V <sub>BOOST</sub>	Output Range	V <sub>BOOST</sub> > V <sub>IN</sub> + V <sub>DIODE</sub>	5		17	V
ΔV <sub>BOOST</sub> /ΔV <sub>IN</sub>	Line Regulation	2.7V < V <sub>IN</sub> < 13.2V, V <sub>BOOST</sub> = 15V		0.1		%
ΔV <sub>BOOST</sub> /ΔI <sub>O1</sub>	Load Regulation	50mA < I <sub>O1</sub> < 300mA		0.5		%
F <sub>OSC-RANGE</sub>	Frequency Range	R <sub>OSC</sub> range = 240kΩ to 60kΩ	200		1000	kHz
F <sub>OSC1</sub>	Switching Frequency	R <sub>OSC</sub> = 100kΩ	620	680	750	kHz
<b>POSITIVE REGULATED CHARGE PUMP (V<sub>ON</sub>)</b>						
Most positive V <sub>ON</sub> output depends on the magnitude of the V <sub>DDP</sub> input voltage (normally connected to V <sub>BOOST</sub> ) and the external component configuration (doubler or tripler)						
V <sub>DDP</sub>	Supply Input for Positive Charge Pump	Usually connected to V <sub>BOOST</sub> output	5		17	V
IQ1(V <sub>DDP</sub> )	Quiescent Current - Shut-down	ENP = 0V		11.5	20	μA
IQ2(V <sub>DDP</sub> )	Quiescent Current - Switching	ENBN = ENP = V <sub>DDB</sub>		2.3	5	mA
V(FBP)	Feedback Reference Voltage		1.245	1.310	1.375	V
I(FBP)	Feedback Input Bias Current			0.1		μA
I(DRVP)	RMS DRVP Output Current	V <sub>DDP</sub> = 12V		60		mA
		V <sub>DDP</sub> = 6V	15			mA
ILR_V <sub>ON</sub>	Load Regulation	5mA < I <sub>L</sub> < 15mA	-0.5	0.03	0.5	%/mA
F <sub>PUMP</sub>	Charge Pump Frequency	Frequency set by R <sub>OSC</sub> - see boost section	0.5*F <sub>OSC</sub>			

**Electrical Specifications**  $V_{IN} = 3.3V$ ,  $V_{BOOST} = 12V$ ,  $R_{OSC} = 100k\Omega$ ,  $T_A = 25^\circ C$  Unless Otherwise Specified. (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
<b>NEGATIVE REGULATED CHARGE PUMP (<math>V_{OFF}</math>)</b>						
Most negative $V_{OFF}$ output depends on the magnitude of the $V_{DDN}$ input voltage (normally connected to $V_{BOOST}$ ) and the external component configuration (doubler or tripler)						
$V_{DDN}$	Supply Input for Negative Charge Pump	Usually connected to $V_{BOOST}$ output	5		17	V
$I_{Q1}(V_{DDN})$	Quiescent Current - Shut-down	$ENBN = 0V$		1.2	10	$\mu A$
$I_{Q2}(V_{DDN})$	Quiescent Current - Switching	$ENBN = V_{DDB}$		2.3	5	mA
$V(FBN)$	Feedback Reference Voltage		-80	0	+80	mV
$I(FBN)$	Feedback Input Bias Current	Magnitude of input bias		0.1		$\mu A$
$I(DRVN)$	RMS $DRVN$ Output Current	$V_{DDN} = 12V$		60		mA
		$V_{DDN} = 6V$	15			mA
$ILR_{V_{OFF}}$	Load Regulation	$-15mA < I_L < -5mA$	-0.5	0.03	0.5	%/mA
$F_{PUMP}$	Charge Pump Frequency	Frequency set by $R_{OSC}$ - see boost section	0.5* $F_{OSC}$			
<b>ENABLE CONTROL LOGIC</b>						
$V_{HI-ENX}$	Enable Input High Threshold	$X = "BN", "P"$	1.4			V
$V_{LO-ENX}$	Enable Input Low Threshold	$X = "BN", "P"$			0.6	V
$IL(EN"X")$	Logic Low Bias Current	$X = "BN", "P" = 0V$		0.1		$\mu A$
$IL(ENBN)$	Logic High Bias Current	$ENBN = 5V$		7.5	15	$\mu A$
$IL(ENP)$	Logic High Bias Current	$ENP = 5V$		3.3	7.5	$\mu A$
<b>OVER-TEMPERATURE PROTECTION</b>						
$T_{OT}$	Over-temperature Threshold			130		$^\circ C$
$T_{HYS}$	Over-temperature Hysteresis			40		$^\circ C$

**Pin Descriptions** I = Input, O = Output, S = Supply

PIN NUMBER	PIN NAME	PIN TYPE	PIN FUNCTION
1	VSSB	S	Ground for DC/DC boost and reference circuits; chip substrate
2	SS	I	Soft-start input; the capacitor connected to this pin sets the current limited start time
3	FBB	I	Voltage feedback input for boost circuit; determines boost output voltage, $V_{BOOST}$
4	VDDB	S	Positive supply input for DC/DC boost circuits
5	LX	O	Boost regulator inductor drive connected to drain of internal NFET
6	LX	O	Boost regulator inductor drive connected to drain of internal NFET
7	LX	O	Boost regulator inductor drive connected to drain of internal NFET
8	DRVN	O	Driver output for the external generation of negative charge pump voltage, $V_{OFF}$
9	VDDN	S	Positive supply for input for $V_{OFF}$ generator
10	FBN	I	Voltage feedback input to determine negative charge pump output, $V_{OFF}$
11	VSSP	S	Negative supply pin for both the positive and negative charge pumps
12	FBP	I	Voltage feedback to determine positive charge pump output, $V_{ON}$
13	VDDP	S	Positive supply input for $V_{ON}$ generator
14	DRVP	O	Voltage driver output for the external generation of positive charge pump, $V_{ON}$
15	PGND	O	Power ground, connected to source of internal NFET
16	PGND	O	Power ground, connected to source of internal NFET
17	VREF	I	Voltage reference for charge pump circuits; decouple to ground
18	ENBN	I	Enable pin for boost ( $V_{BOOST}$ generation) and negative charge pump ( $V_{OFF}$ generation); active high
19	ENP	I	Enable for DRVP ( $V_{ON}$ generation); active high
20	ROSC	I	Connected to an external resistor to ground; sets the switching frequency of the DC/DC boost

Typical Performance Curves

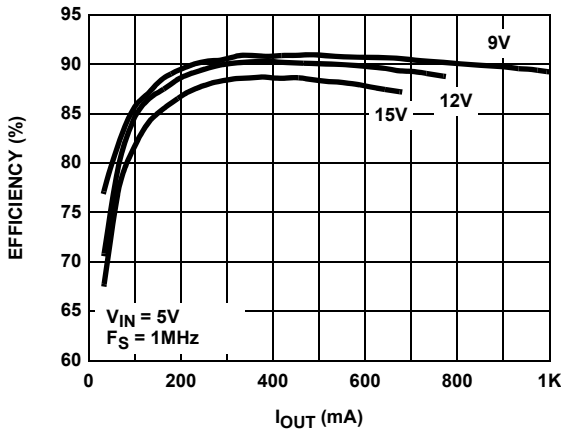


FIGURE 1. EFFICIENCY vs IOUT

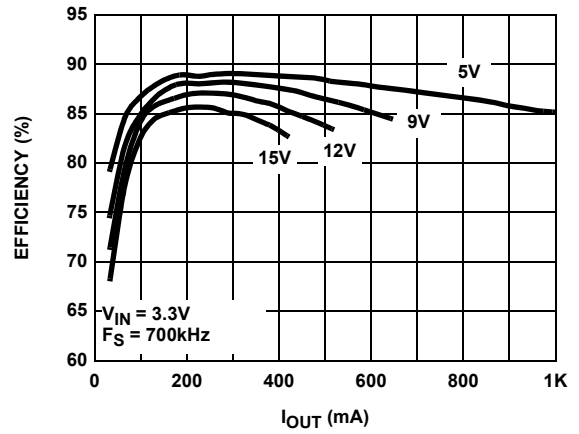


FIGURE 2. EFFICIENCY vs IOUT

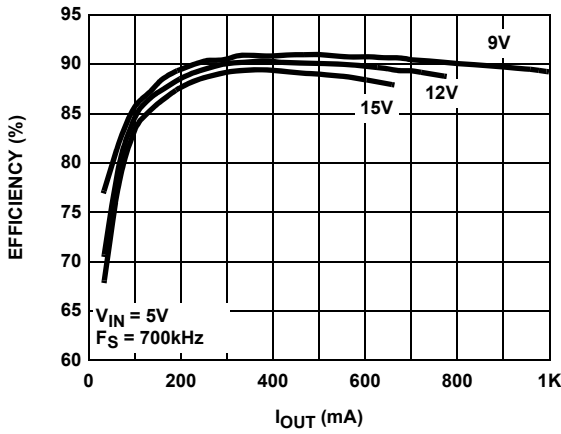


FIGURE 3. EFFICIENCY vs IOUT

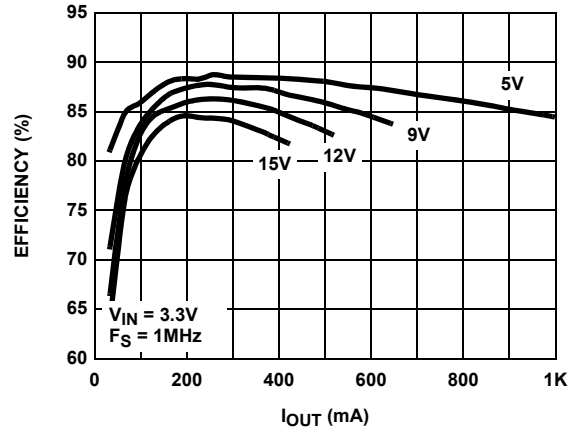


FIGURE 4. EFFICIENCY vs IOUT

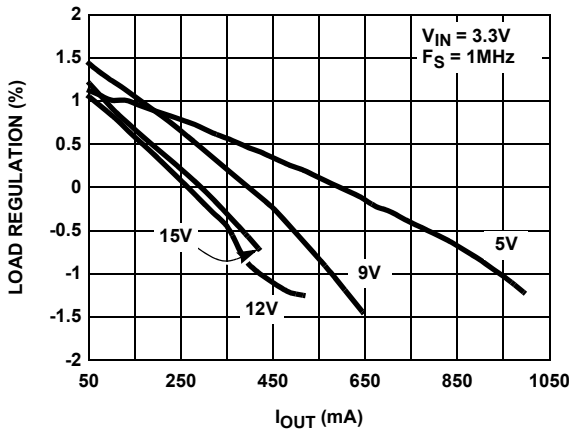


FIGURE 5. LOAD REGULATION

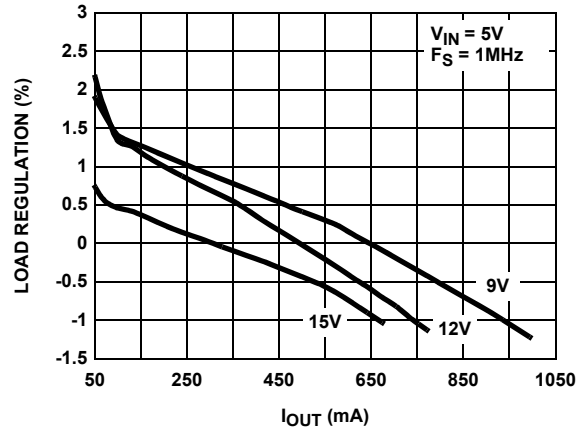


FIGURE 6. LOAD REGULATION

Typical Performance Curves (Continued)

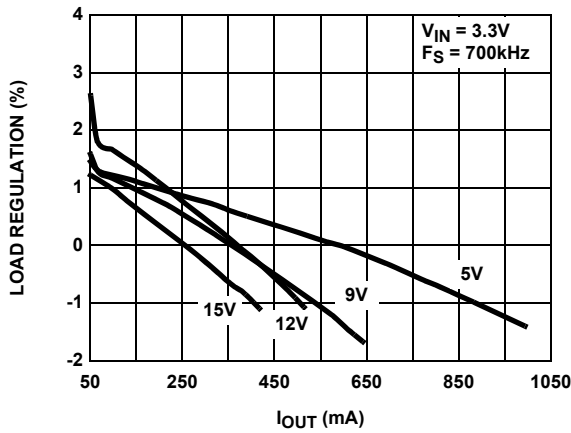


FIGURE 7. LOAD REGULATION

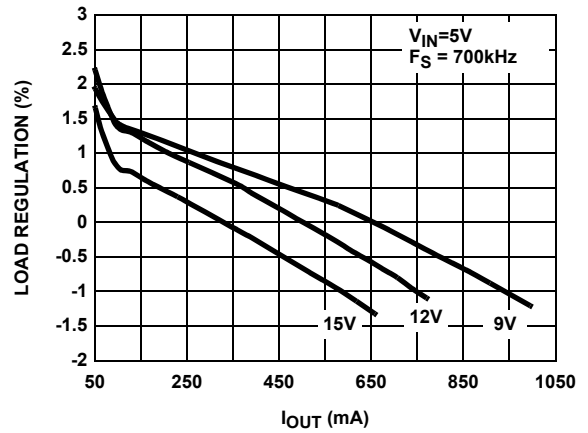


FIGURE 8. LOAD REGULATION

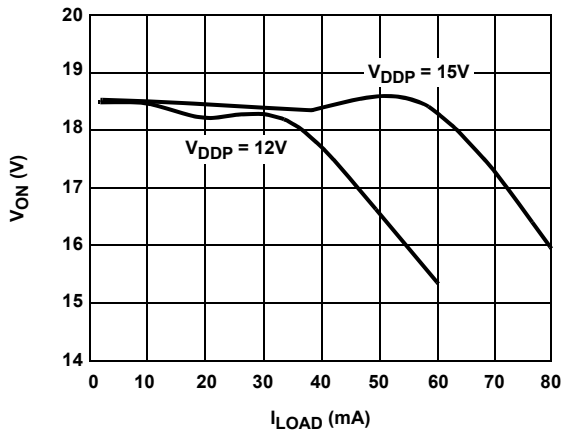


FIGURE 9. V<sub>ON</sub> vs I<sub>ON</sub>

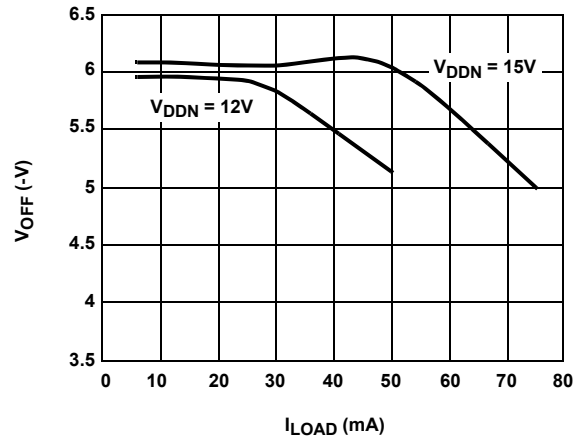


FIGURE 10. V<sub>OFF</sub> vs I<sub>OFF</sub>

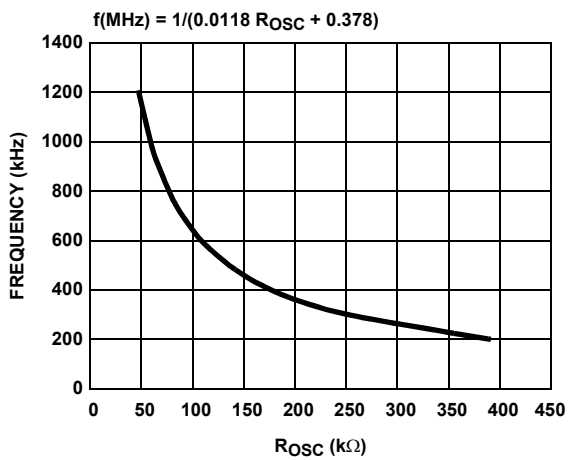


FIGURE 11. F<sub>S</sub> vs R<sub>OSC</sub>

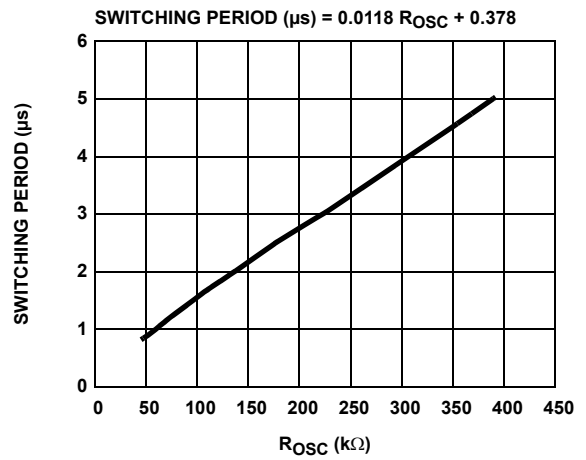


FIGURE 12. SWITCHING PERIOD vs R<sub>OSC</sub>

**Typical Performance Curves** (Continued)

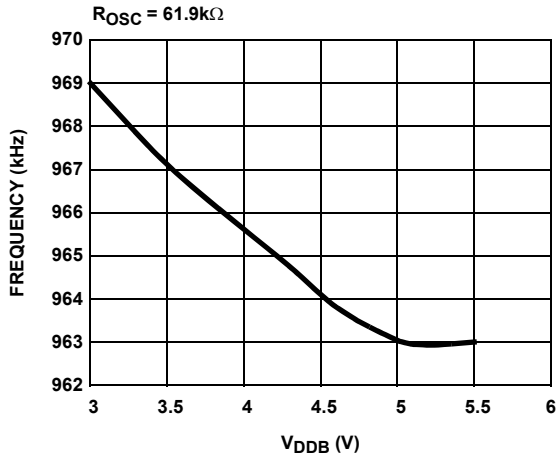


FIGURE 13.  $F_S$  vs  $V_{DDB}$

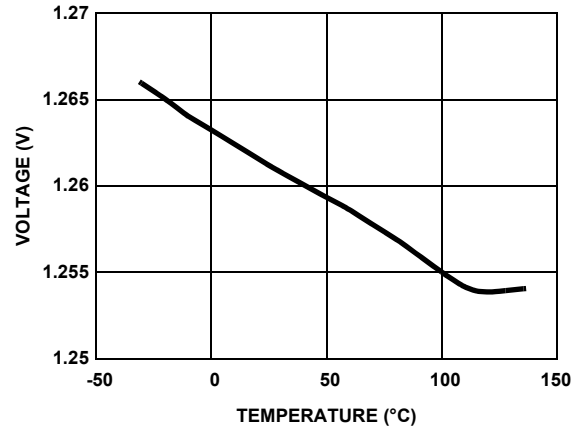


FIGURE 14.  $V_{REF}$  vs TEMPERATURE

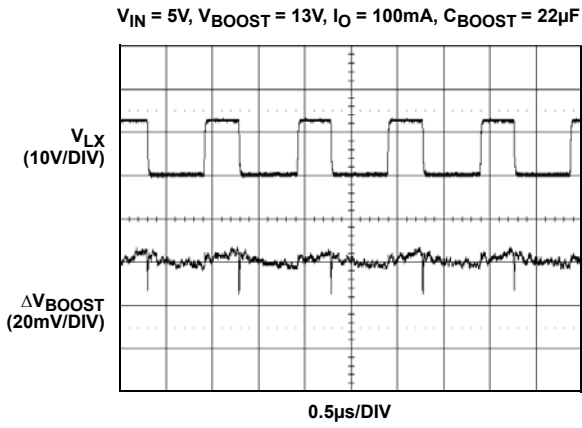


FIGURE 15. BOOST STAGE

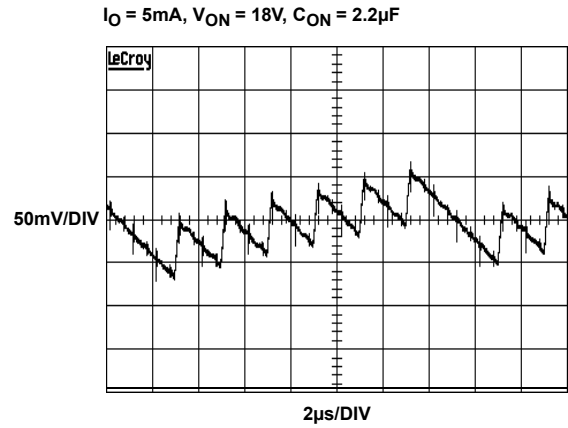


FIGURE 16.  $V_{ON}$  RIPPLE

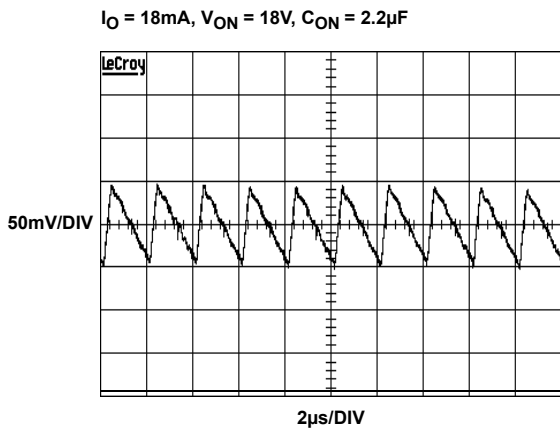


FIGURE 17.  $V_{ON}$  RIPPLE

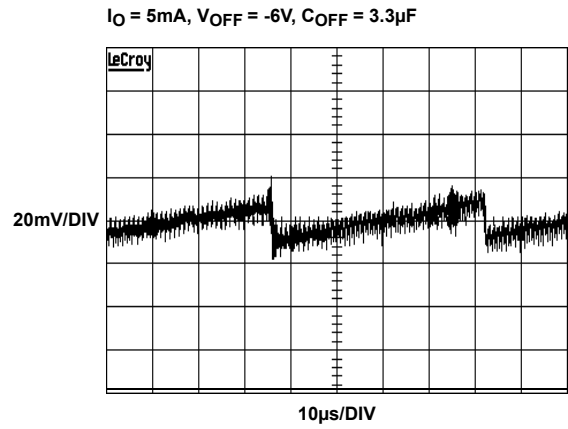


FIGURE 18.  $V_{OFF}$  RIPPLE

**Typical Performance Curves** (Continued)

$I_O = 15\text{mA}$ ,  $V_{OFF} = -6\text{V}$ ,  $C_{OFF} = 3.3\mu\text{F}$

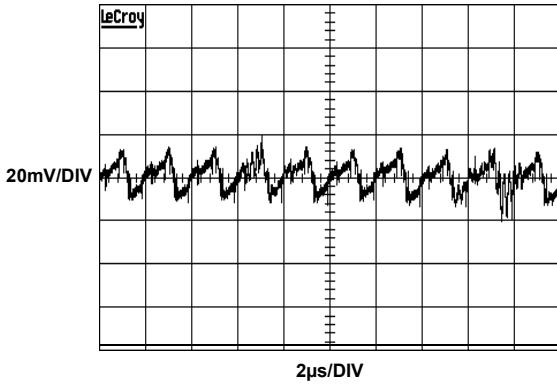


FIGURE 19.  $V_{OFF}$  RIPPLE

$V_{BOOST} = 13\text{V}$ ,  $I_O = 100\text{mA}$  to  $420\text{mA}$ ,  $C_{BOOST} = 22\mu\text{F}$

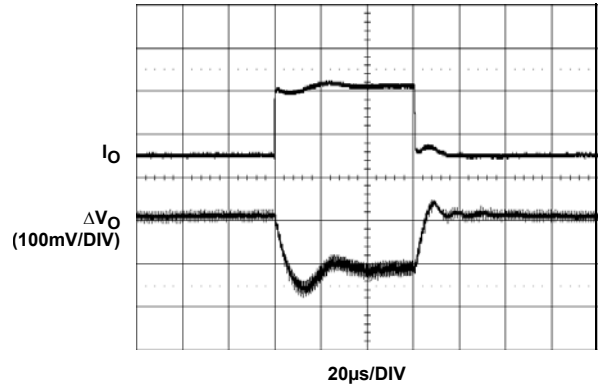


FIGURE 20. BOOST CONVERTER TRANSIENT RESPONSE

$C_{SS} = 0.033\mu\text{F}$

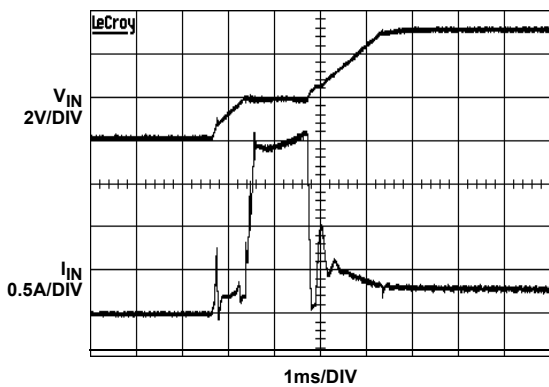


FIGURE 21. START-UP VOLTAGE AND CURRENT

$C_{SS} = 0.1\mu\text{F}$

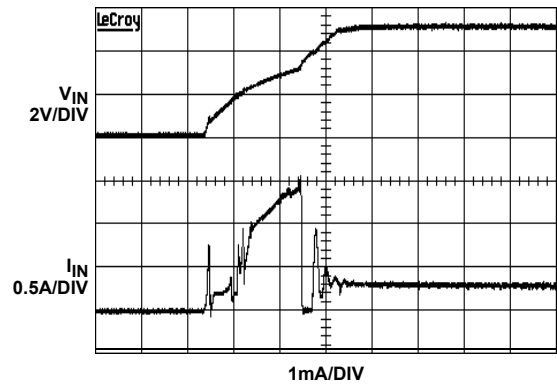


FIGURE 22. START-UP VOLTAGE AND CURRENT

$C_{SS} = 0.1\mu\text{F}$

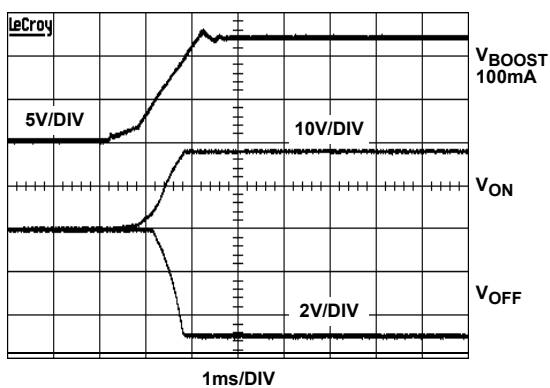


FIGURE 23. POWER-UP, NO DELAY RC NETWORK ON ENABLE PINS

$C_{SS} = 0.1\mu\text{F}$

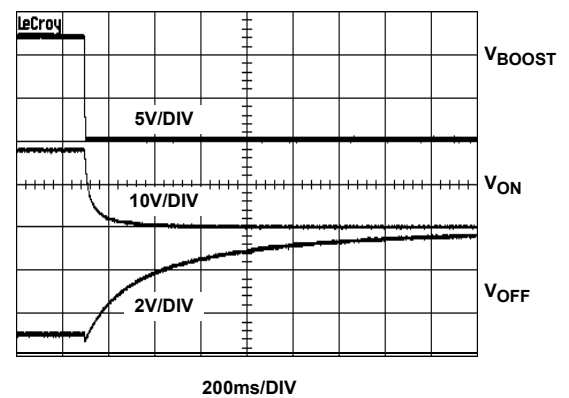


FIGURE 24. POWER-DOWN, NO DELAY RC NETWORK ON ENABLE PINS



Typical Performance Curves (Continued)

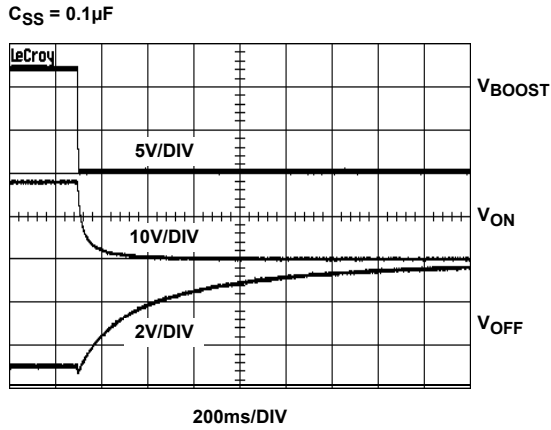


FIGURE 25. POWER-DOWN, 100K AND 0.1μF DELAY NETWORK ON ENP

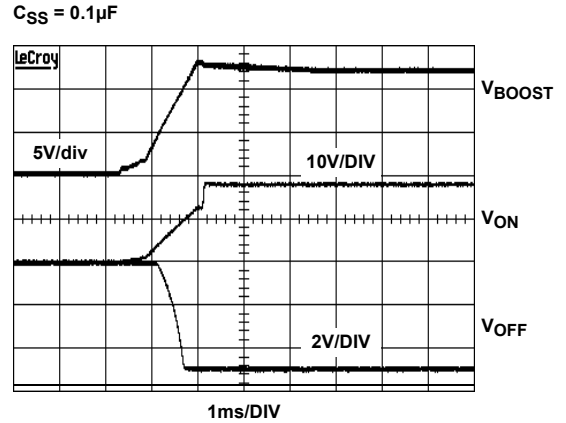


FIGURE 26. POWER-UP, 100K AND 0.1μF DELAY NETWORK ON ENP

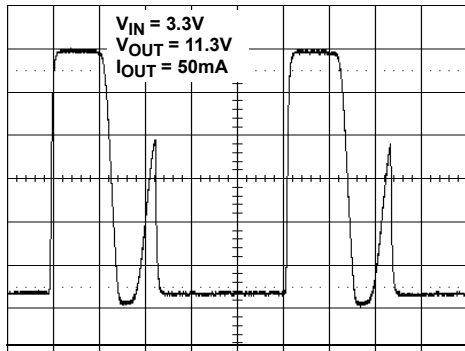


FIGURE 27. LX WAVEFORM - DISCONTINUOUS MODE

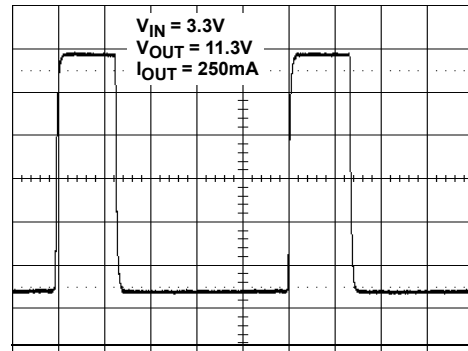


FIGURE 28. LX WAVEFORM - CONTINUOUS MODE

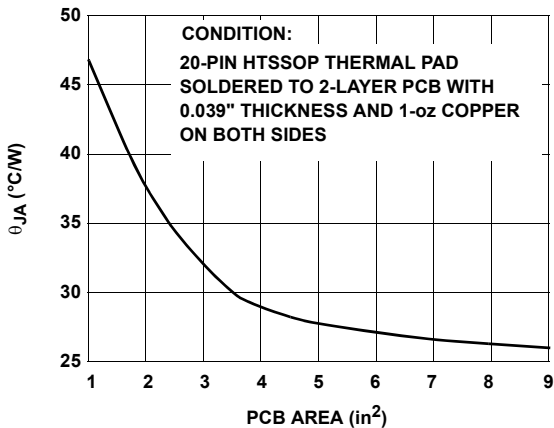


FIGURE 29. 20-PIN HTSSOP THERMAL RESISTANCE vs PCB AREA, NO AIR FLOW

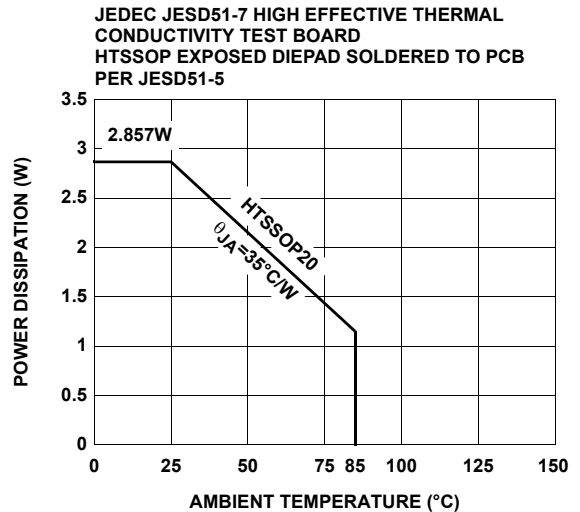


FIGURE 30. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

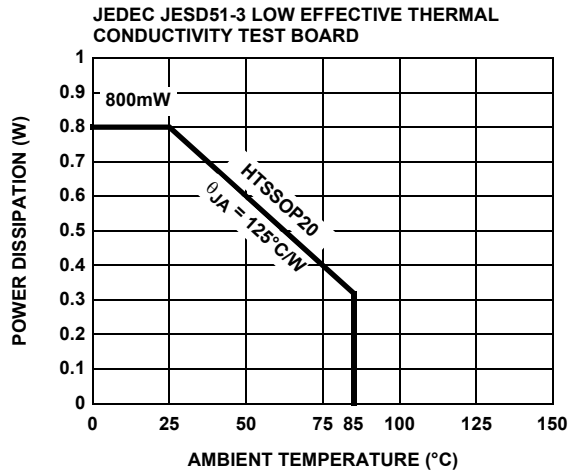
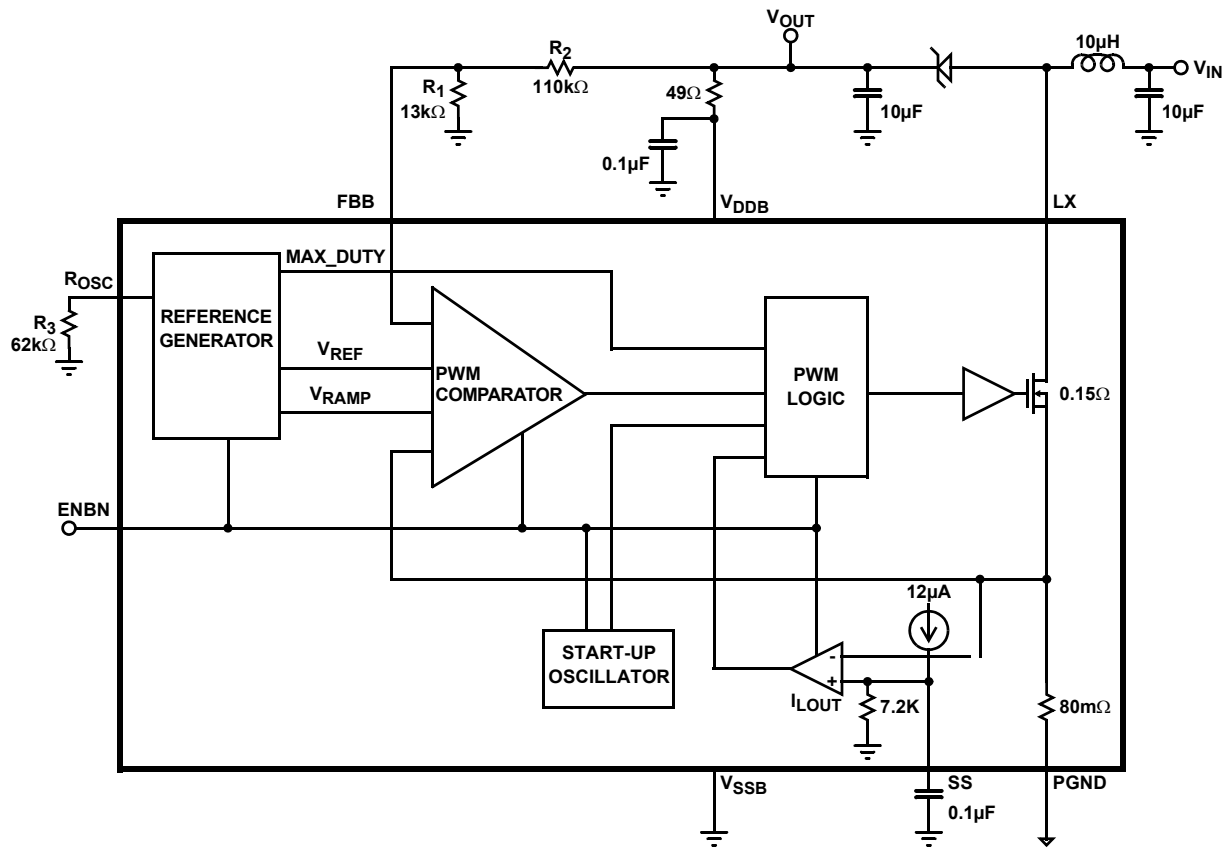


FIGURE 31. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Block Diagram



## Applications Information

The EL7581 is high efficiency multiple output power solution designed specifically for thin-film transistor (TFT) liquid crystal display (LCD) applications. The device contains one high current boost converter and two low power charge pumps ( $V_{ON}$  and  $V_{OFF}$ ).

The boost converter contains an integrated N-channel MOSFET to minimize the number of external components. The converter output voltage can be set from 5V to 18V with external resistors. The  $V_{ON}$  and  $V_{OFF}$  charge pumps are independently regulated to positive and negative voltages using external resistors. Output voltages as high as 40V can be achieved with additional capacitors and diodes.

### Boost Converter

The boost converter operates in constant frequency pulse-width-modulation (PWM) mode. Quiescent current for the EL7581 is only 5mA when enabled, and since only the low side MOSFET is used, switch drive current is minimized. 90% efficiency is achieved in most common application operating conditions.

A functional block diagram with typical circuit configuration is shown on the previous page. Regulation is performed by the PWM comparator which regulates the output voltage by comparing a divided output voltage with an internal reference voltage. The PWM comparator outputs its result to the PWM logic. The PWM logic switches the MOSFET on and off through the gate drive circuit. Its switching frequency is external adjustable with a resistor from timing control pin ( $R_{OSC}$ ) to ground. The boost converter has 200kHz to 1.2MHz operating frequency range.

### Start-Up

After  $V_{DDB}$  reaches a threshold of about 2V, the power MOSFET is controlled by the start-up oscillator, which generates fixed duty-ratio of 0.5 - 0.7 at a frequency of several hundred kilohertz. This will boost the output voltage, providing the initial output current load is not too great (<250mA).

When  $V_{DDB}$  reaches about 3.7V, the PWM comparator takes over the control. The duty ratio will be decided by the multiple-input direct summing comparator, Max\_Duty signal (about 90% duty-ratio), and the Current Limit Comparator, whichever is the smallest.

The soft-start is provided by the current limit comparator. As the internal 12 $\mu$ A current source charges the external soft-start capacitor, the peak MOSFET current is limited by the voltage on the capacitor. This in turn controls the rising rate of output voltage.

The regulator goes through the start-up sequence as well after the ENBN signal is pulled to HI.

### Steady-State Operation

When the output reaches the preset voltage, the regulator operates at steady state. Depending on the input/output

condition and component, the inductor operates at either continuous-conduction mode or discontinuous-conduction mode.

In the continuous-conduction mode, the inductor current is a triangular waveform and LX voltage a pulse waveform. In the discontinuous-conduction mode, the inductor current is completely 'dried-out' before the MOSFET is turned on again. The input voltage source, the inductor, and the MOSFET and output diode parasitic capacitors forms a resonant circuit. Oscillation will occur in this period. This oscillation is normal and will not affect the regulation.

At very low load, the MOSFET will skip pulse sometimes. This is normal.

### Current Limit

The MOSFET current limit is nominal  $I_{LMT} = 2.75A$ . This restricts the maximum output current  $I_{OMAX}$  based on the following formula:

$$I_{OMAX} = \left( I_{LMT} - \frac{\Delta I_L}{2} \right) \times \frac{V_{IN}}{V_O}$$

where:

- $\Delta I_L$  is the inductor peak-to-peak current ripple and is decided by:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{F_S}$$

- D is the MOSFET turn-on ratio and is decided by:

$$D = \frac{V_O - V_{IN}}{V_O}$$

- $F_S$  is the switching frequency.

The following table gives typical values:

(Margins are considered in deriving  $I_{OMAX}$ . They are 10%, 3%, 20%, 10%, and 20% on  $V_{IN}$ ,  $V_O$ , L,  $F_S$ , and  $I_{LMT}$ , respectively.)

TABLE 1. MAXIMUM CONTINUOUS OUTPUT CURRENT

$V_{IN}$ (V)	$V_O$ (V)	L ( $\mu$ H)	$F_S$ (kHz)	$I_{OMAX}$ (mA)
3.3	5	10	1000	1200
3.3	9	10	1000	660
3.3	12	10	1000	490
3.3	15	10	1000	390
5	9	10	1000	980
5	12	10	1000	720
5	15	10	1000	570
12	15	10	1000	1300
12	18	10	1000	1100

## Component Considerations

### Input Capacitor

It is recommended that  $C_{IN}$  is larger than  $10\mu\text{F}$ . Theoretically, the input capacitor has ripple current of  $\Delta I_L$ . Due to high-frequency noise in the circuit, the input current ripple may exceed the theoretical value. Larger capacitor will reduce the ripple further.

### Boost Inductor

The inductor has peak and average current decided by:

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2}$$

$$I_{LAVG} = \frac{I_O}{1 - D}$$

The inductor should be chosen to be able to handle this current. Furthermore, due to the fixed internal compensation, it is recommended that maximum inductance of  $10\mu\text{H}$  and  $15\mu\text{H}$  to be used in the 5V and 12V or higher output voltage, respectively.

The output diode has average current of  $I_O$ , and peak current the same as the inductor's peak current. Schottky diode is recommended and it should be able to handle those currents.

### Feedback Resistor Network

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of  $200\text{k}\Omega$  is recommended. The boost converter output voltage is determined by the following relationship:

$$V_{BOOST} = \frac{R_1 + R_2}{R_1} \times V_{FBB}$$

Where  $V_{FBB}$  is 1.300V as specified.

A  $3.9\text{nF}$  compensation capacitor across the feedback resistor to ground is recommended to keep the converter in stable operation at low output current and high frequency conditions.

### Schottky Diode

Speed, forward voltage drop, and reverse current are the three most critical specifications for selecting the Schottky diode. The entire output current flows through the diode, so the diode average current is the same as the average load current and the peak current is the same as the inductor peak current. When selecting the diode, one must consider the forward voltage drop at the peak diode current. On the Elantec demo board, MBRM120 is selected. Its forward voltage drop is  $450\text{mV}$  at  $1\text{A}$  forward current.

### Output Capacitor

The EL7581 is specially compensated to be stable with capacitors which have a worst-case minimum value of  $10\mu\text{F}$  at the particular  $V_{OUT}$  being set. Output ripple voltage requirements also determine the minimum value and the type of capacitors. Output ripple voltage consists of two components - the voltage drop caused by the switching current through the ESR of the output capacitor and the charging and discharging of the output capacitor:

$$V_{RIPPLE} = I_{LPK} \times \text{ESR} + \frac{V_{OUT} - V_{IN}}{V_{OUT}} \times \frac{I_{OUT}}{C_{OUT} \times \text{FS}}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging/discharging of the output capacitor.

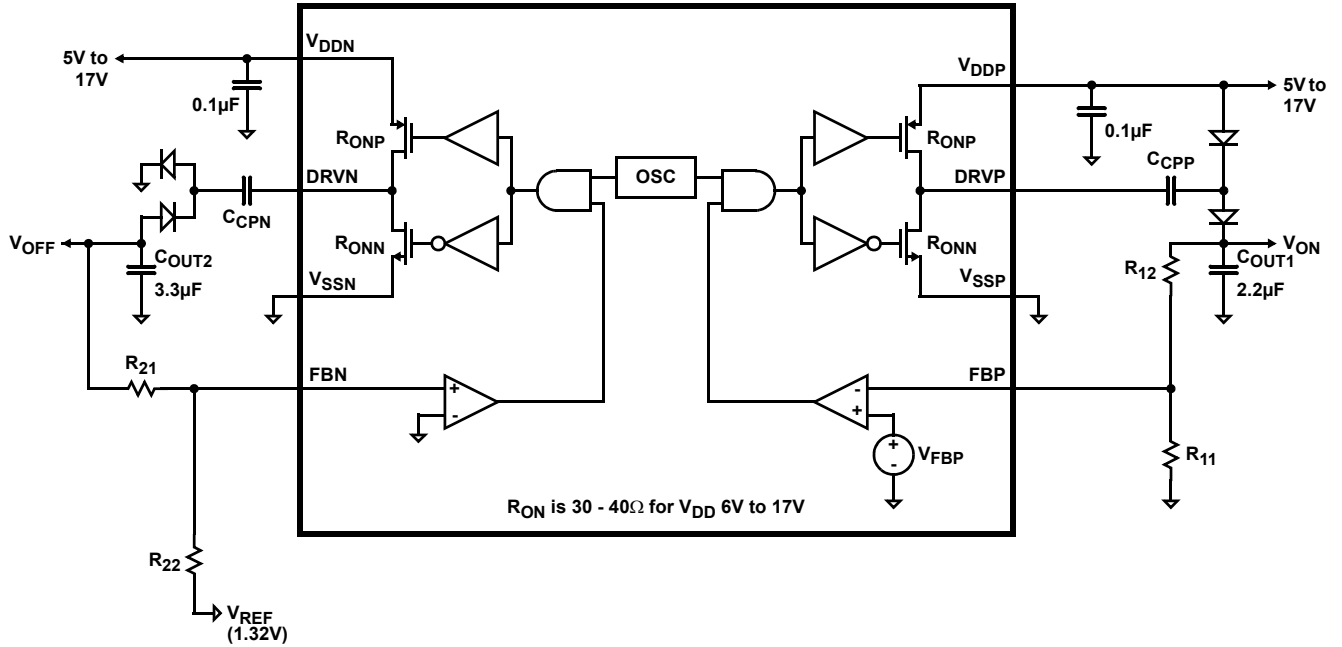
In addition to the voltage rating, the output capacitor should also be able to handle the RMS current is given by:

$$I_{CORMS} = \sqrt{(1 - D) \times \left( D + \frac{\Delta I_L^2}{I_{LAVG}^2} \times \frac{1}{12} \right)} \times I_{LAVG}$$

### Positive and Negative Charge Pump ( $V_{ON}$ and $V_{OFF}$ )

The EL7581 contains two independent charge pumps (see charge pump block and connection diagram.) The negative charge pump inverts the  $V_{DDN}$  supply voltage and provides a regulated negative output voltage. The positive charge pump doubles the  $V_{DDP}$  supply voltage and provides a regulated positive output voltage. The regulation of both the negative and positive charge pumps is generated by the internal comparator that senses the output voltage and compares it with an internal reference. The switching frequency of the charge pump is set to  $\frac{1}{2}$  the boost converter switching frequency.

The pumps use pulse width modulation to adjust the pump period, depending on the load present. The pumps are short-circuit protected to  $180\text{mA}$  at  $12\text{V}$  supply and can provide  $15\text{mA}$  to  $60\text{mA}$  for  $6\text{V}$  to  $12\text{V}$  supply.



**Positive Charge Pump Design Considerations**

A single stage charge pump is shown above. The maximum  $V_{ON}$  output voltage is determined by the following equation:

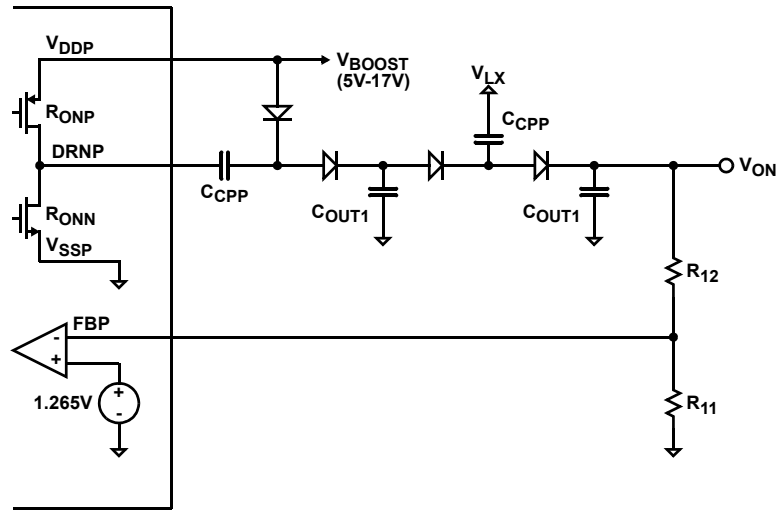
$$V_{ON(max)} \leq 2 \times V_{DDCPP} - I_{OUT} \times 2 \times (R_{ONN} + R_{ONP}) - 2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPP}} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT1}}$$

where:

- $R_{ONN}$  and  $R_{ONP}$  resistance values depend on the  $V_{DDP}$  voltage levels. For 12V supply,  $R_{ON}$  is typically 33Ω. For 6V supply,  $R_{ON}$  is typically 45Ω.

If additional stage is required, the LX switching signal is recommended to drive the additional charge pump diodes. The drive impedance at the LX switching is typically 150mΩ. The figure on the next page illustrates an implementation for two-stage positive charge pump circuit.

## Two-Stage Positive Charge Pump Circuit



The maximum  $V_{ON}$  output voltage for  $N+1$  stage charge pump is:

$$V_{ON(max)} \leq 2 \times V_{DDP} - I_{OUT} \times 2 \times (R_{ONN} + R_{ONP}) - 2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPP}} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT1}} + N \times V_{LX(max)} - N \times \left( 2 \times V_{DIODE} + I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPP}} + I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT1}} \right)$$

$R_{11}$  and  $R_{12}$  set the  $V_{ON}$  output voltage:

$$V_{ON} = V_{FBP} \times \frac{R_{11} + R_{12}}{R_{11}}$$

Where  $V_{FBP}$  is nominal 1.310V.

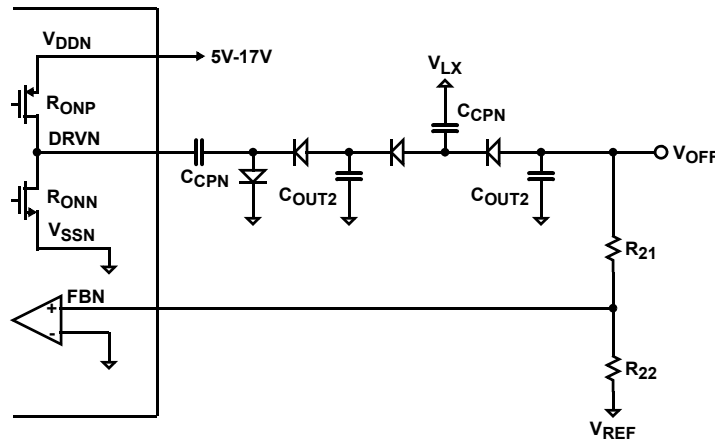
### Negative Charge Pump Design Considerations

The criteria for the negative charge pump is similar to the positive charge pump. For a single stage charge pump, the maximum  $V_{OFF}$  output voltage is:

$$V_{OFF(max)} \geq I_{OUT} \times 2 \times (R_{ONN} + R_{ONP}) + 2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPN}} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT2}} - V_{DDN}$$

Similar to positive charge pump, if additional stage is required, the LX switching signal is recommended to drive the additional charge pump diodes. The figure on the next page shows a two stage negative charge pump circuit.

## Two-Stage Negative Charge Pump Circuit



The maximum  $V_{OFF}$  output voltage for  $N+1$  stage charge pump is:

$$V_{OFF(max)} \geq I_{OUT} \times 2 \times (R_{ONN} + R_{ONP}) + 2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPN}} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT2}} - V_{DDN} - N \times V_{LX(max)} + N \times \left( 2 \times V_{DIODE} + I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPN}} + I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT2}} \right)$$

$R_{21}$  and  $R_{22}$  determine  $V_{OFF}$  output voltage:

$$V_{OFF} = -V_{REF} \times \frac{R_{21}}{R_{22}}$$

Where  $V_{REF}$  is nominal 1.310V.

### Over-Temperature Protection

An internal temperature sensor continuously monitors the die temperature. In the event that die temperature exceeds the thermal trip point, the device will shut down and disable itself. The upper and lower trip points are typically set to 130°C and 90°C respectively.

### PCB Layout Guidelines

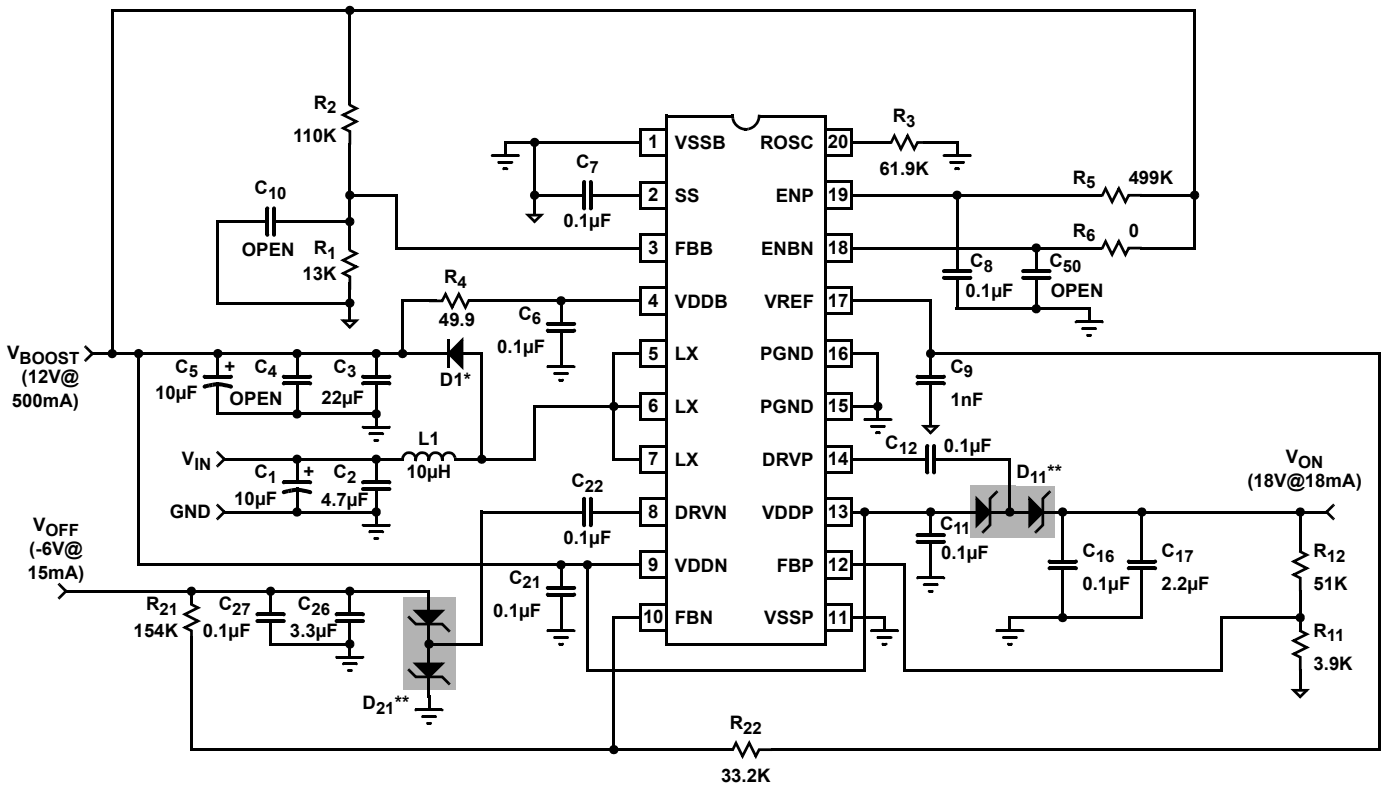
Careful layout is critical in the successful operation of the application. The following layout guidelines are recommended to achieve optimum performance.

- $V_{REF}$  and  $V_{DDB}$  bypass capacitors should be placed next to the pins.
- Place the boost converter diode and inductor close to the LX pins.
- Place the boost converter output capacitor close to the PGND pins.
- Locate feedback dividers close to their respected feedback pins to avoid switching noise coupling into the high impedance node.
- Place the charge pump feedback resistor network after the diode and output capacitor node to avoid switching noise.

- Thermal pad needs to be connected to PGND pins electrically, and it should be soldered to PCB with thermal vias connecting to ground plane for maximum heat dissipation.
- All low-side feedback resistors should be connected directly to  $V_{SSB}$ .  $V_{SSB}$  should be connected to the power ground close at one point only.

A demo board is available to illustrate the proper layout implementation.

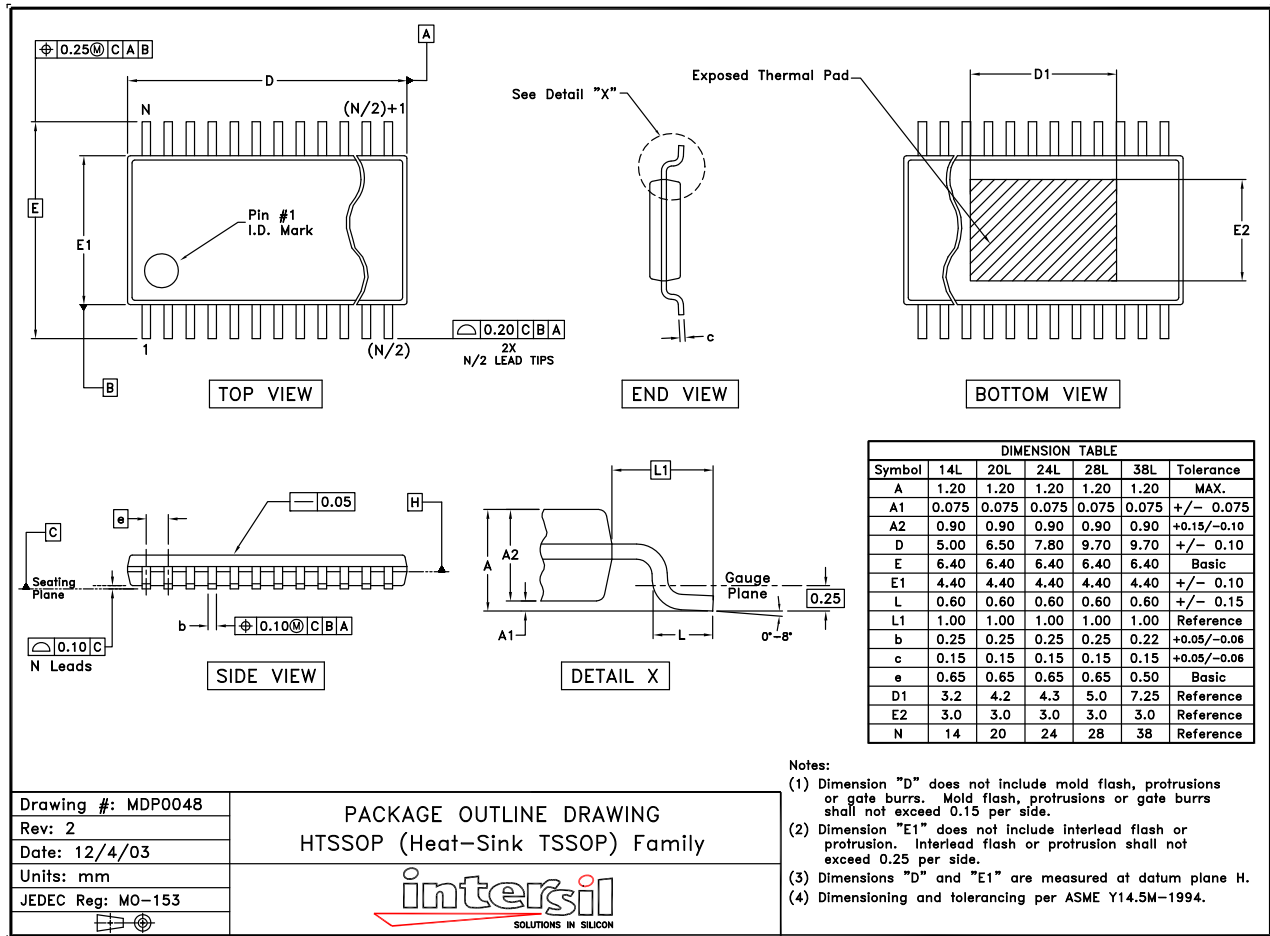
Typical Application Circuit



\* MBRM120LT3  
 \*\* BAT54S



# Package Outline Drawing



NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>

© Copyright Intersil Americas LLC 2004-2006. All Rights Reserved.  
 All trademarks and registered trademarks are the property of their respective owners.

For additional products, see [www.intersil.com/en/products.html](http://www.intersil.com/en/products.html)

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at [www.intersil.com/en/support/qualandreliability.html](http://www.intersil.com/en/support/qualandreliability.html)

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)