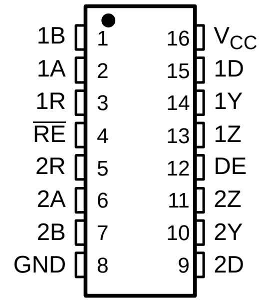
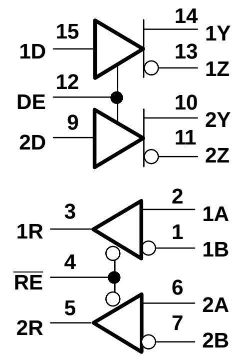
HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

FEATURES

- Typically Meets or Exceeds ANSI TIA/EIA-644-1995 Standard
- Operates From a Single 2.4-V to 3.6-V Supply
- Signaling Rates up to 400 Mbit/s
- Bus-Terminal ESD Exceeds 12 kV
- Low-Voltage Differential Signaling With Typical Output Voltages of 285 mV and a 100-Ω Load
- Propagation Delay Times
  - Driver: 1.7-ns Typical
  - Receiver: 3.7-ns Typical
  - Driver: 25-mW Typical
  - Receiver: 60-mW Typical
- Power Dissipation at 200 MHz
  - Driver: 25-mW Typical
  - Receiver: 60-mW Typical
- LVTTL Input Levels Are 5-V Tolerant
- Receiver Maintains High Input Impedance
- Receiver Has Open-Circuit Fail Safe
- Available in Thin Shink Outline Packaging With 20-mil Lead Pitch

SN65LVDS1050PW
(Marked as **DL1050** or **LDS1050**)
(TOP VIEW)





DRIVER FUNCTION TABLE

INPUTS		OUTPUTS	
D	DE	Y	Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z

H = high level, L = low level, Z = high impedance, X = don't care

RECEIVER FUNCTION TABLE

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 100$ mV	L	H
$-100 \text{ mV} < V_{ID} < 100$ mV	L	?
$V_{ID} \leq -100$ mV	L	L
Open	L	H
X	H	Z

H = high level, L = low level, Z = high impedance, X = don't care

DESCRIPTION

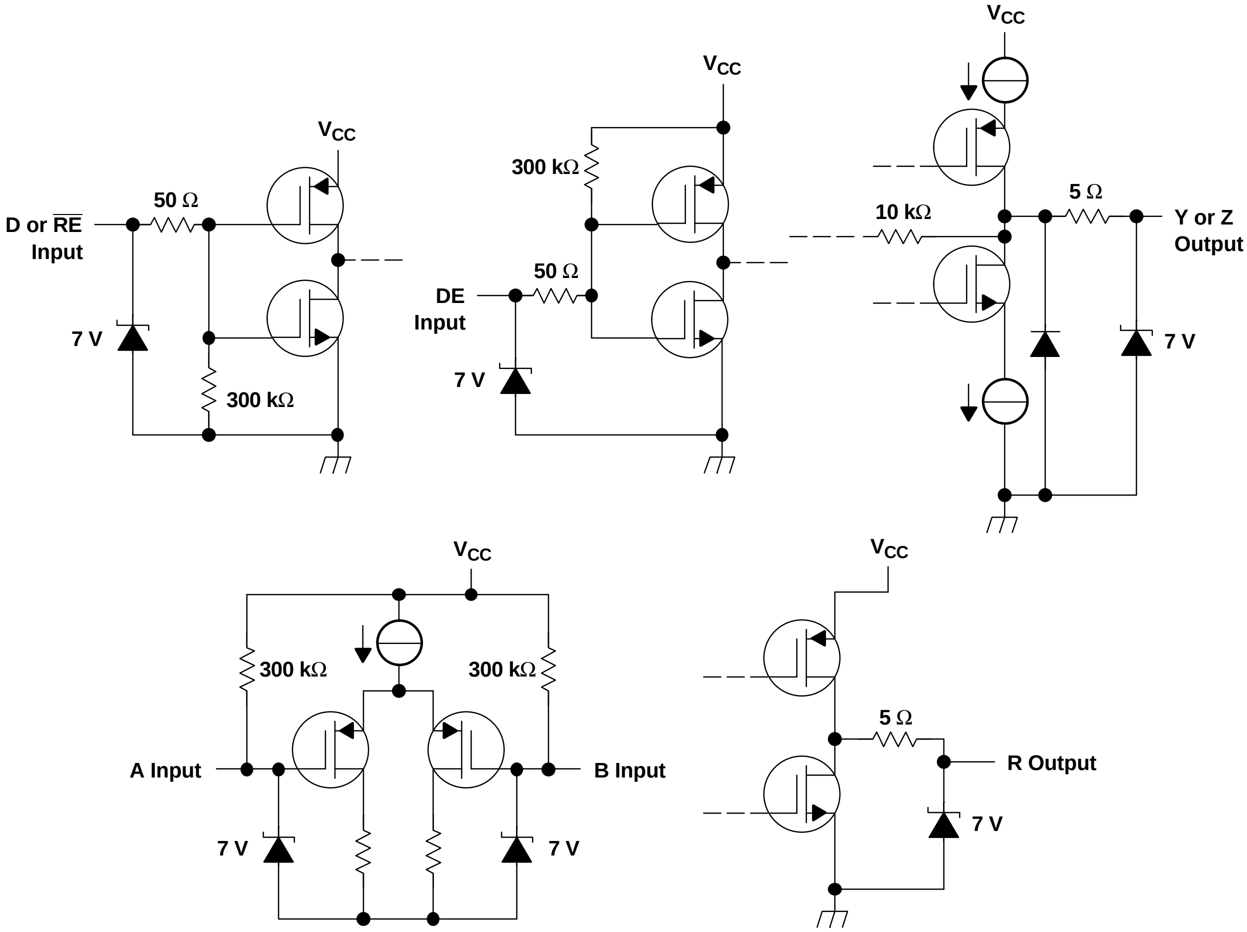
The SN65LVDS1050 is similar to the SN65LVDS050 except that it is characterized for operation with a lower supply voltage range and packaged in the thin shrink outline package for portable battery-powered applications.

The differential line drivers and receivers use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbps. The drivers provide a minimum differential output voltage magnitude of 247 mV into a 100-Ω load and receipt of 100-mV signals with up to 1 V of ground potential difference between a transmitter and receiver.

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100-Ω characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables. Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment and other application-specific characteristics.

The SN65LVDS1050 is characterized for operation from -40°C to 85°C.

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		UNIT
Supply voltage range, V_{CC} (2)		-0.5 V to 4 V
Voltage range (D, R, DE, $\overline{RE}$)		-0.5 V to 6 V
Voltage range (Y, Z, A, and B)		-0.5 V to 4 V
Electrostatic discharge	Y, Z, A, B , and GND (3)	CLass 3, A:12 kV, B:600 V
	All terminals	Class 3, A:7 kV, B:500 V
Continuous power dissipation		See Dissipation Rating Table
Storage temperature range		-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		250°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages are with respect to network ground terminal.
(3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq$ 25°C POWER RATING	DERATING FACTOR ABOVE T_A=25°C	T_A=85°C POWER RATING
PW	774 mW	6.2 mW/°C	402 mW

RECOMMENDED OPERATING CONDITIONS (1)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	2.4	2.7	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Magnitude of differential input voltage, $\|V_{ID}\|$	0.1		0.6	V
Driver output voltage, V_{OY} or V_{OZ}	0		2.4	V
Magnitude of differential output voltage with disabled driver, $\|V_{OD(dis)}\|$			520	mV
Common-mode input voltage, V_{IC} (see Figure 5)	0		$2.4 - \frac{\|V_{ID}\|}{2}$	V
			V_{CC}-0.8	
Operating free-air temperature, T_A	40		85	°C

(1) The common-mode input voltage, V_{IC}, is not fully 644 compliant when V_{CC} = 2.4 V.

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
I_{CC} Supply current	Driver and receiver enabled, No receiver load, Driver R_L=100 Ω		12	20	mA
	Driver enabled, Receiver disabled, R_L=100 Ω		10	16	
	Driver disabled, Receiver enabled, No load		3	6	
	Disabled		0.5	1	

(1) All typical values are at 25°C and with a 2.7-V supply.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude		R_L=100Ω, See Figure 1 and Figure 2	247	285	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states			50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 3	1.125		1.37 5	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				50	150	mV
I_{IH}	High-level input current	DE	V_{IH}=5 V		0.5	20	µA
		D			2	20	
I_{IL}	Low-level input current	DE	V_{IL}=0.8 V		0.5	10	µA
		D			2	20	
I_{OS}	Short-circuit output current		V_{OY} or V_{OZ}=0 V		3	10	mA
			V_{OD}=0 V		3	10	
$I_{O(OFF)}$	Off-state output current		DE=0 V, V_{OY}=V_{OZ}=0 V	-1		1	µA
			DE=V_{CC}, V_{OY}=V_{OZ}=0 V, V_{CC} < 1.5 V				
C_{IN}	Input capacitance				3		pF

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 5 and Table 1			100	mV
V_{ITH-}	Negative-going differential input voltage threshold		100			
V_{OH}	High-level output voltage	I_{OH}=-8 mA	2			V
V_{OL}	Low-level output voltage	I_{OL}=8 mA			0.4	V
I_I	Input current (A or B inputs)	V_I=0	2		20	µA
		V_I=2.4 V	1.2			
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_{CC}=0			±20	µA
I_{IH}	High-level input current (enables)	V_{IH}=5 V			±10	µA
I_{IL}	Low-level input current (enables)	V_{IL}=0.8 V			±10	µA
I_{OZ}	High-impedance output current	V_O =0 or 5 V			±10	µA

(1) All typical values are at 25°C and with a 2.7-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	M	AXUNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L=100Ω, C_L=10 pF, See Figure 2		1.7	2.7	ns
t_{PHL}	Propagation delay time, high-to-low-level output			1.7	3	ns
t_r	Differential output signal rise time			0.8	1	ns
t_f	Differential output signal fall time			0.8	1	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHL}$ - $t_{pLH}\|$)			300		ps
$t_{sk(o)}$	Channel-to-channel output skew (2)			150		ps
t_{en}	Enable time	See Figure 4		7.8	10	ns
t_{dis}	Disable time			6.6	10	ns

(1) All typical values are at 25°C and with a 2.7-V supply.
(2) $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.

RECEIVER SWITCHING CHARCTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=10 pF, See Figure 6		3.7	5.2	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3.7	4.5	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHL}$ - $t_{pLH}\|$)			0.3		ns
t_r	Output signal rise time			0.8	1.5	ns
t_f	Output signal fall time			0.8	1.5	ns
t_{PZH}	Propagation delay time, high-level-to-high-impedance output	See Figure 7		5.4		ns
t_{PZL}	Propagation delay time, low-level-to-low-impedance output			6.3		ns
t_{PHZ}	Propagation delay time, high-impedance-to-high-level output			6.1		ns
t_{PLZ}	Propagation delay time, low-impedance-to-high-level output			6.9		ns

(1) All typical values are at 25°C and with a 2.7-V supply.

PARAMETER MEASUREMENT INFORMATION

DRIVER

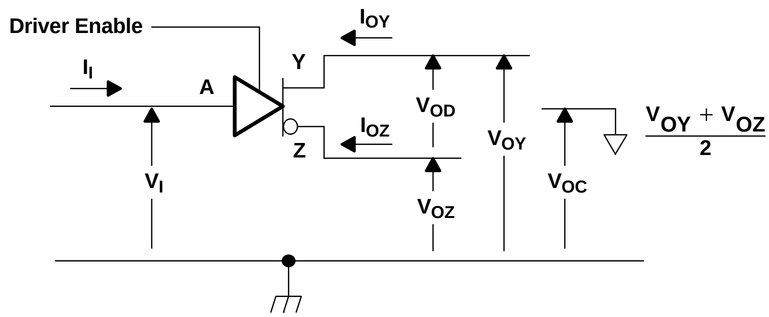
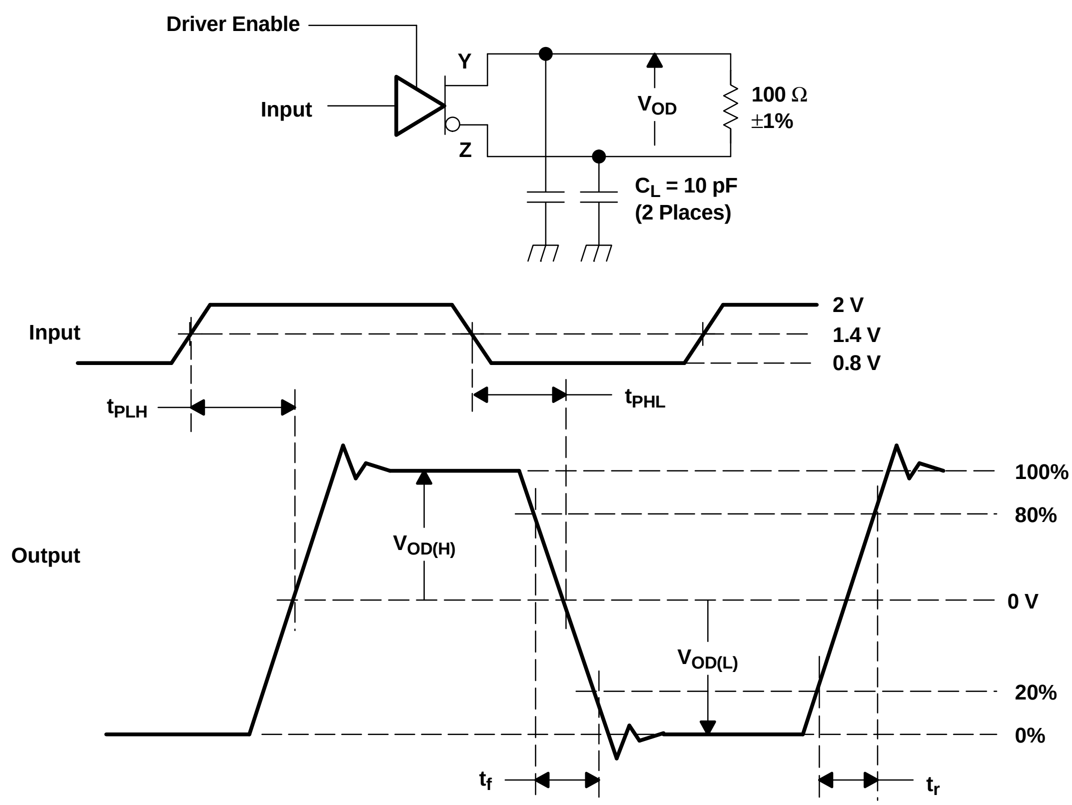
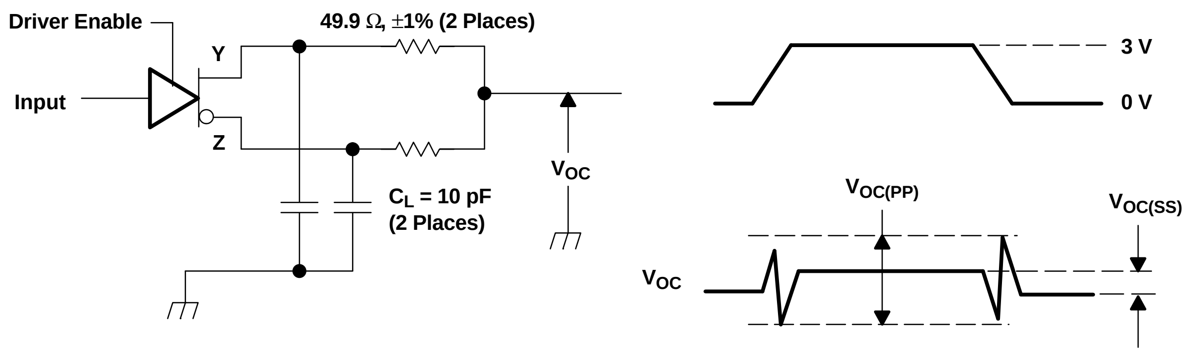


Figure 1. Driver Voltage and Current Definitions



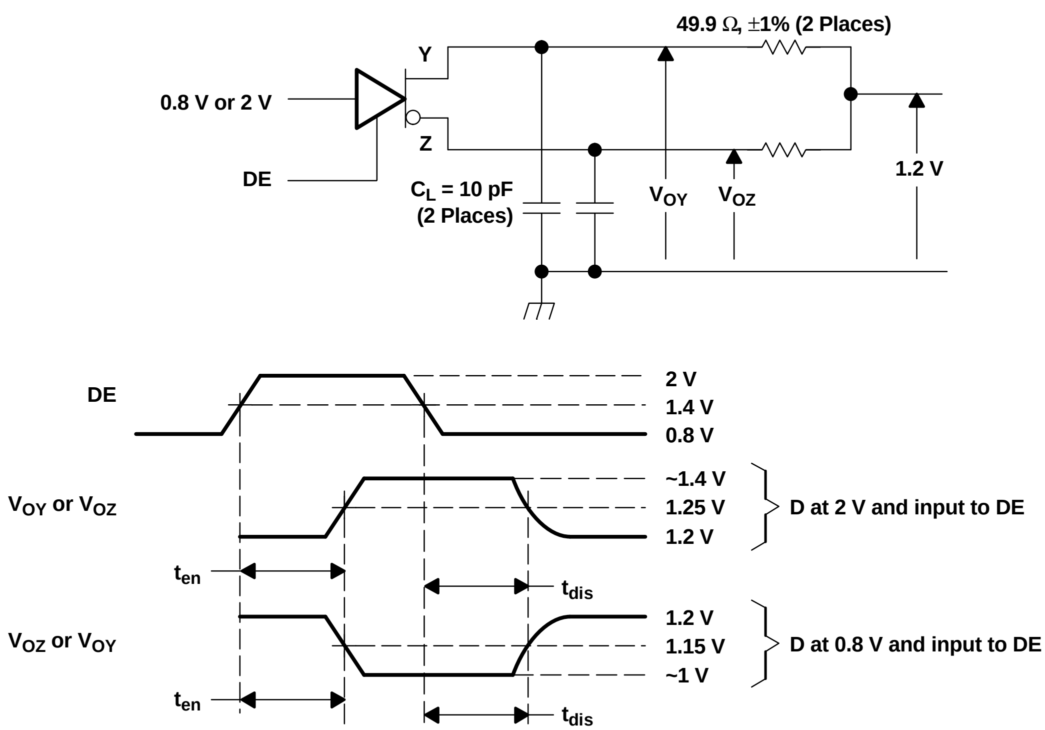
All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Driver Enable and Disable Time Circuit and Definitions

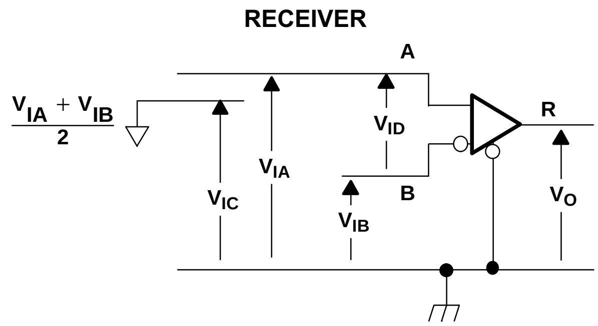
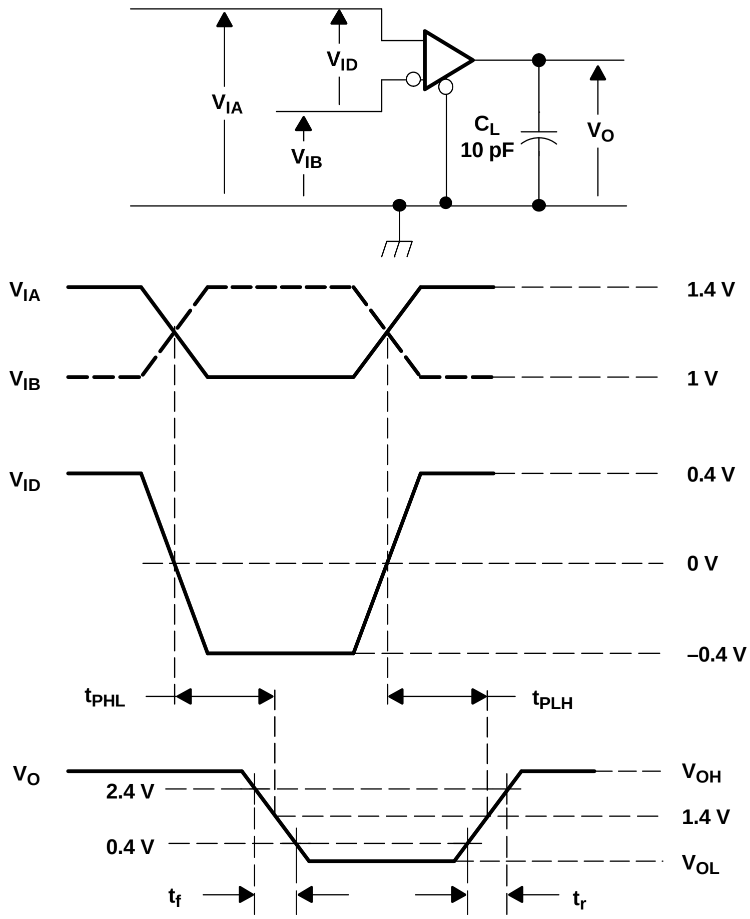


Figure 5. Receiver Voltage Definitions

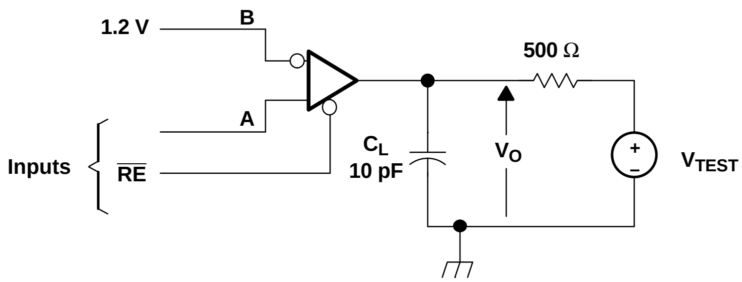
Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES (V)		RESULTING DIFFERENTIAL INPUT VOLTAGE (mV)	RESULTING COMMON-MODE INPUT VOLTAGE (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.15	100	1.2
1.15	1.25	100	1.2
2.4	2.3	100	2.35
2.3	2.4	100	2.35
0.1	0	100	0.05
0	0.1	100	0.05
1.5	0.9	600	1.2
0.9	1.5	600	1.2
2.4	1.8	600	2.1
1.8	2.4	600	2.1
0.6	0	600	0.3
0	0.6	600	0.3



All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 6. Timing Test Circuit and Waveforms



All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

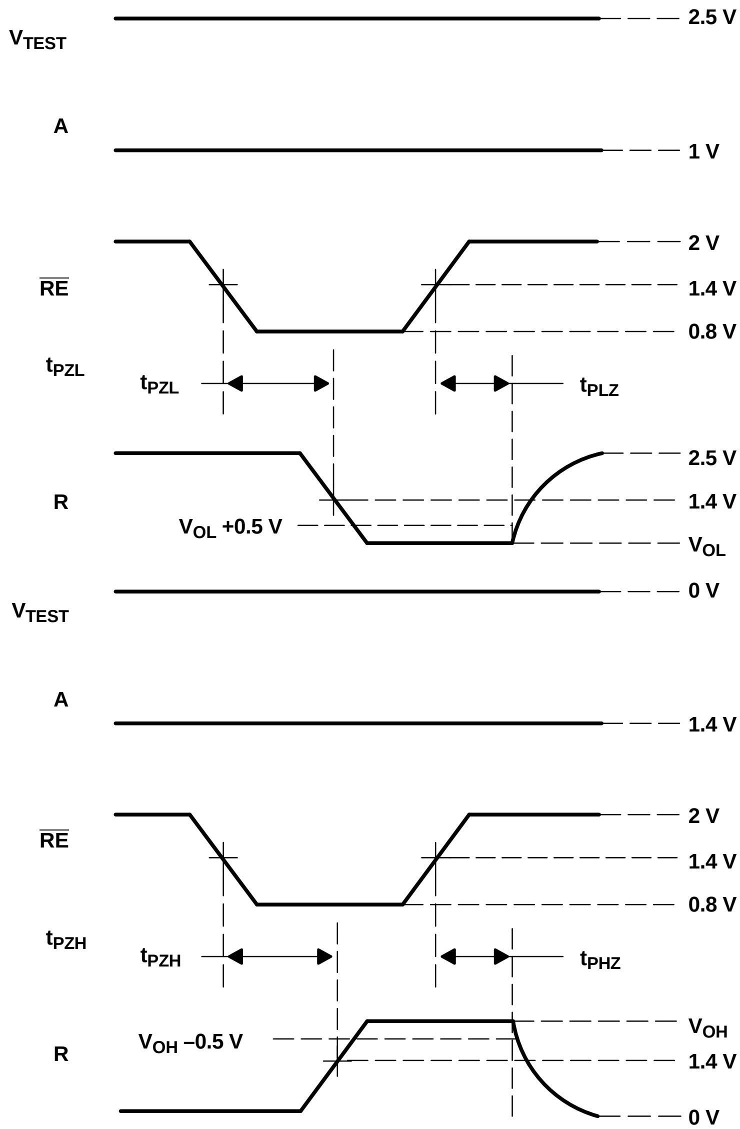


Figure 7. Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

**RECEIVER
DISABLED DRIVER OUTPUT CURRENT
vs
OUTPUT VOLTAGE**

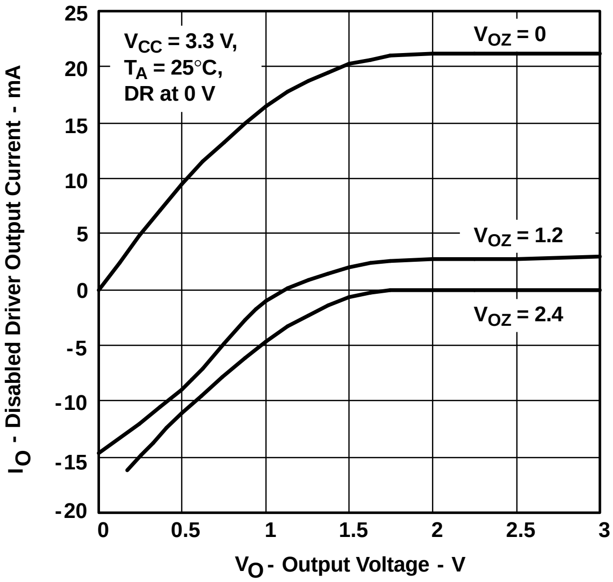


Figure 8.

**DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

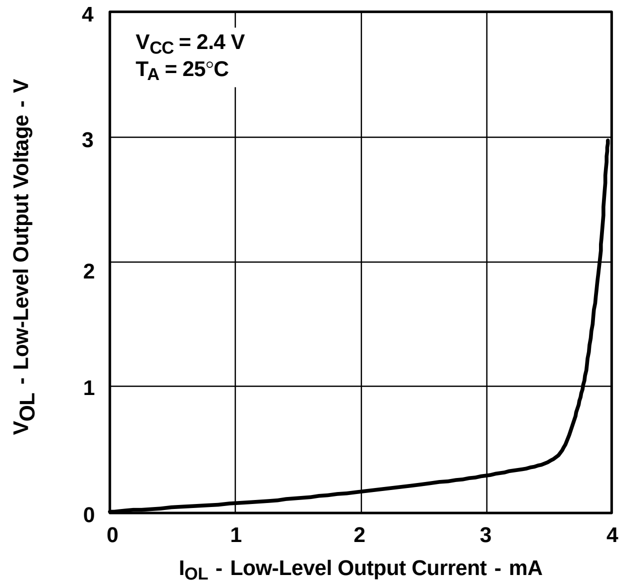


Figure 9.

**DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

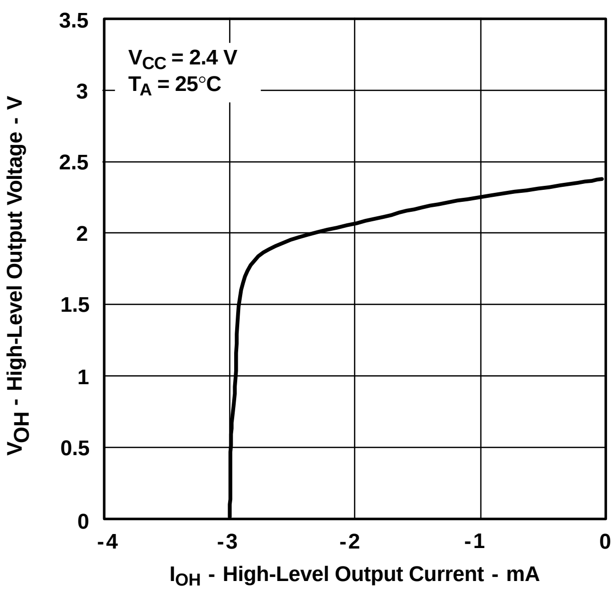


Figure 10.

**RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

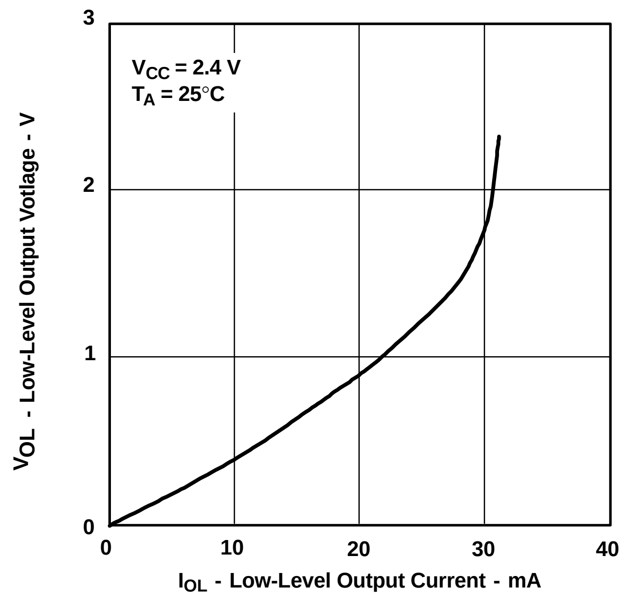


Figure 11.

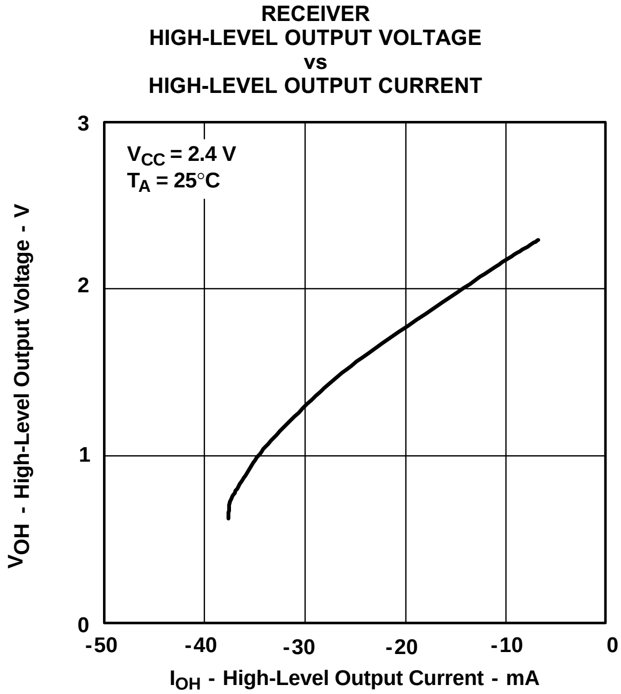


Figure 12.

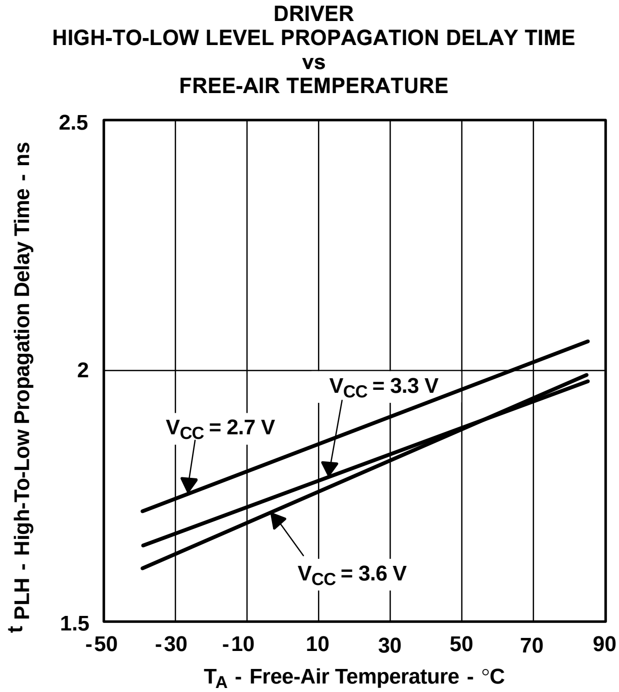


Figure 13.

DRIVER
LOW-TO-HIGH LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

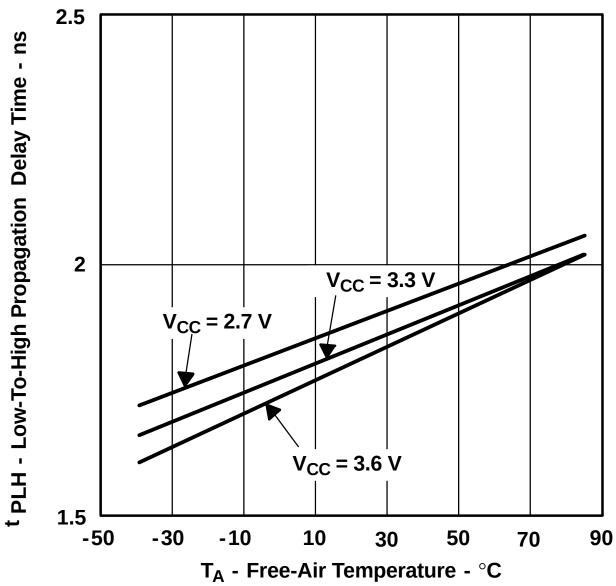


Figure 14.

RECEIVER
HIGH-TO-LOW LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

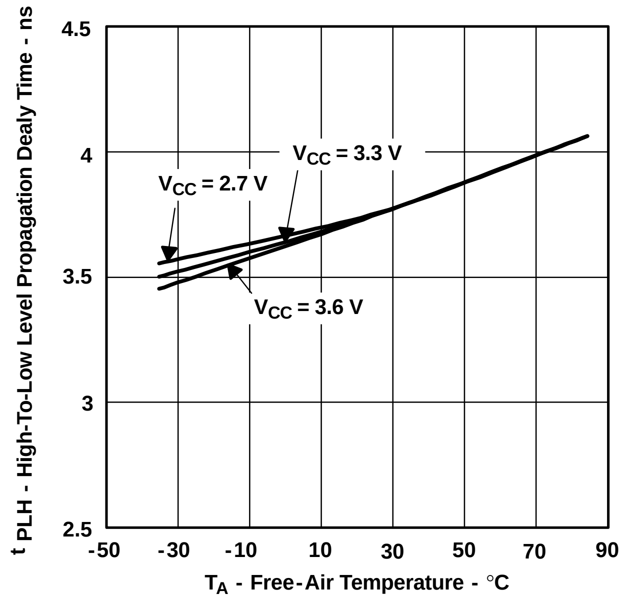


Figure 15.

RECEIVER
LOW-TO-HIGH LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

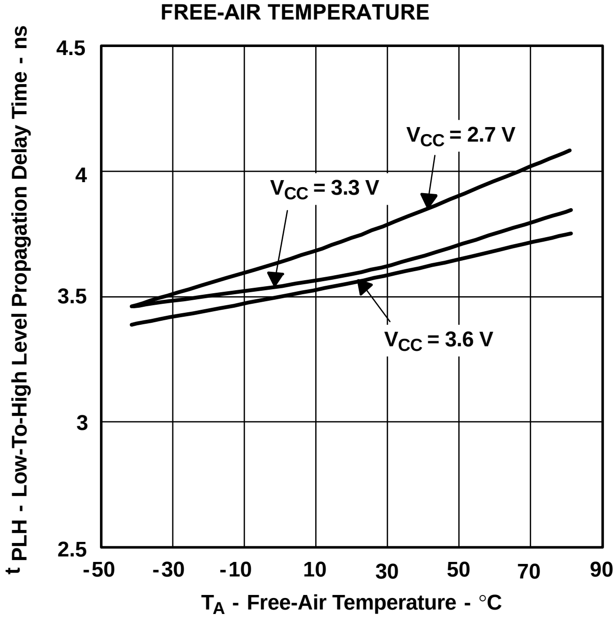


Figure 16

APPLICATION INFORMATION

The devices are generally used as building blocks for high-speed point-to-point data transmission. Ground differences are less than 1 V with a low common-mode output and balanced interface for very low noise emissions. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/Receivers maintain ECL speeds without the power and dual supply requirements.

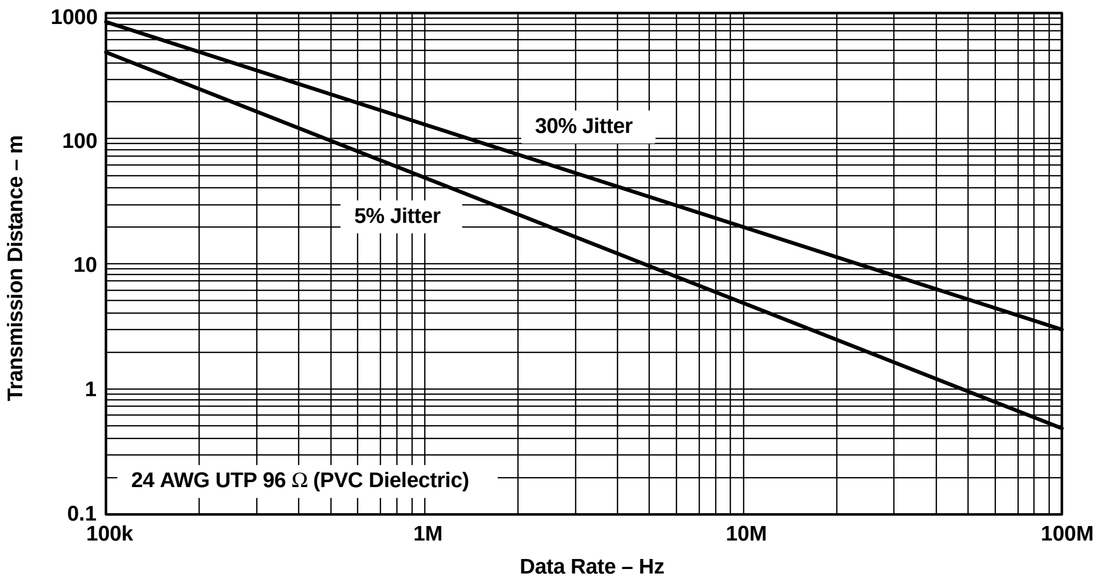


Figure 17. Data Transmission Distance Versus Rate

Fail Safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between -100 mV and100 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near V_{CC} through 300-kΩ resistors as shown in Figure 11. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level, regardless of the differential input voltage.

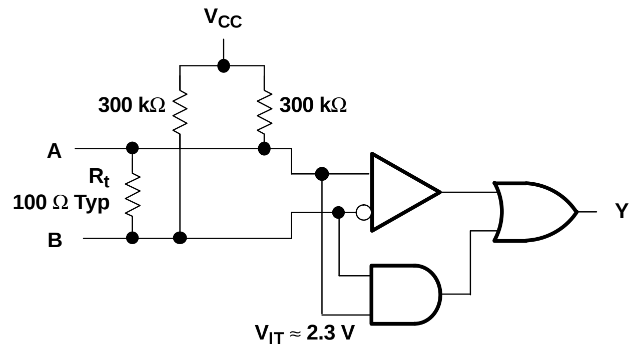


Figure 18. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver is valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS1050PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL1050	Samples
SN65LVDS1050PWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL1050	Samples
SN65LVDS1050PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL1050	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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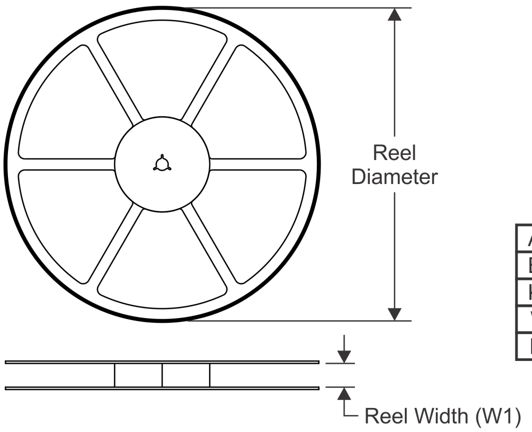
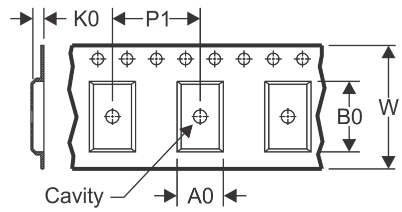
TAPE AND REEL INFORMATION

REEL DIMENSIONS

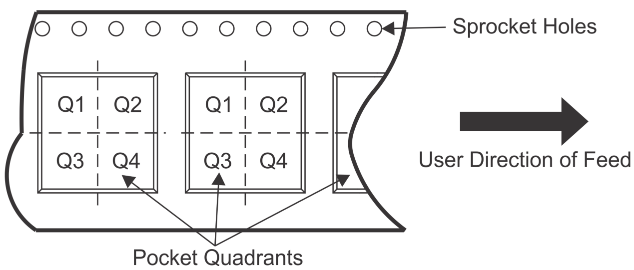


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

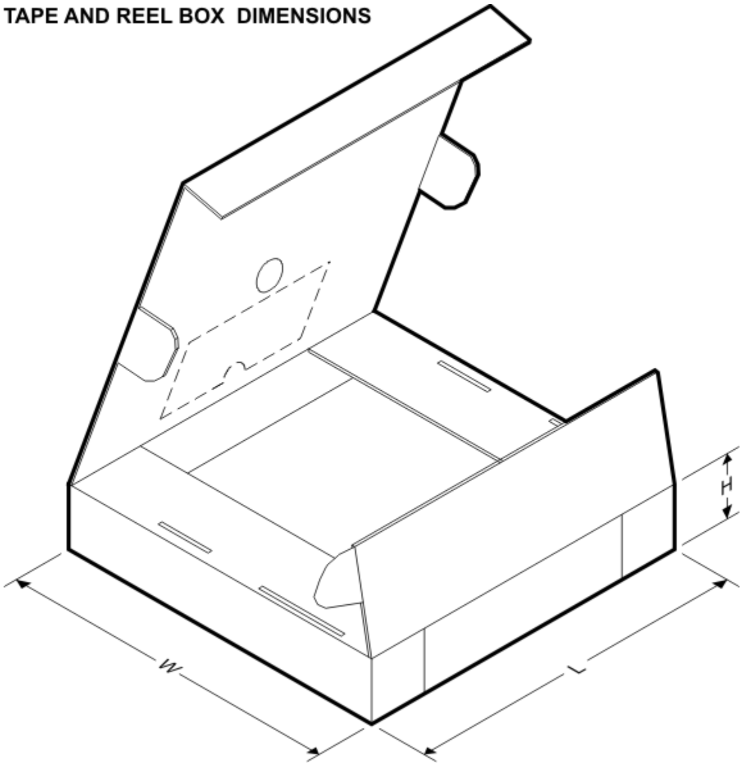
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS1050PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

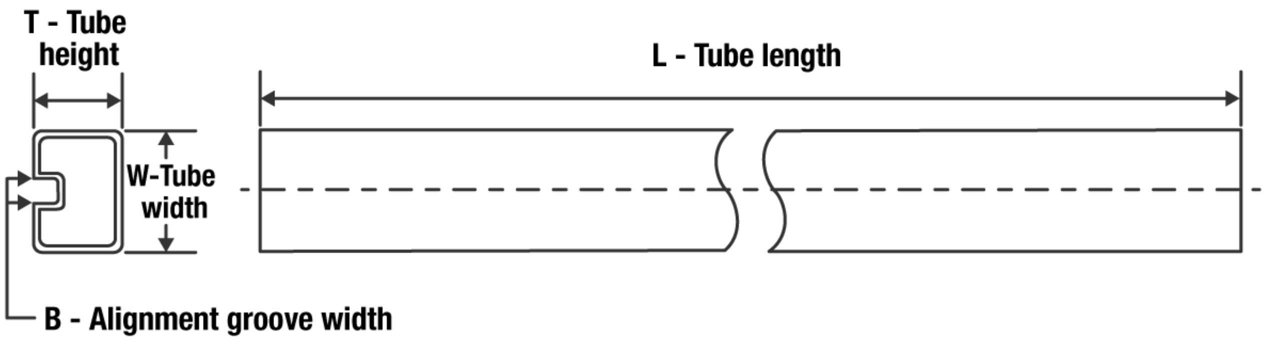
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

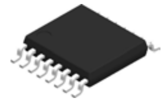
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS1050PWR	TSSOP	PW	16	2000	853.0	449.0	35.0

TUBE

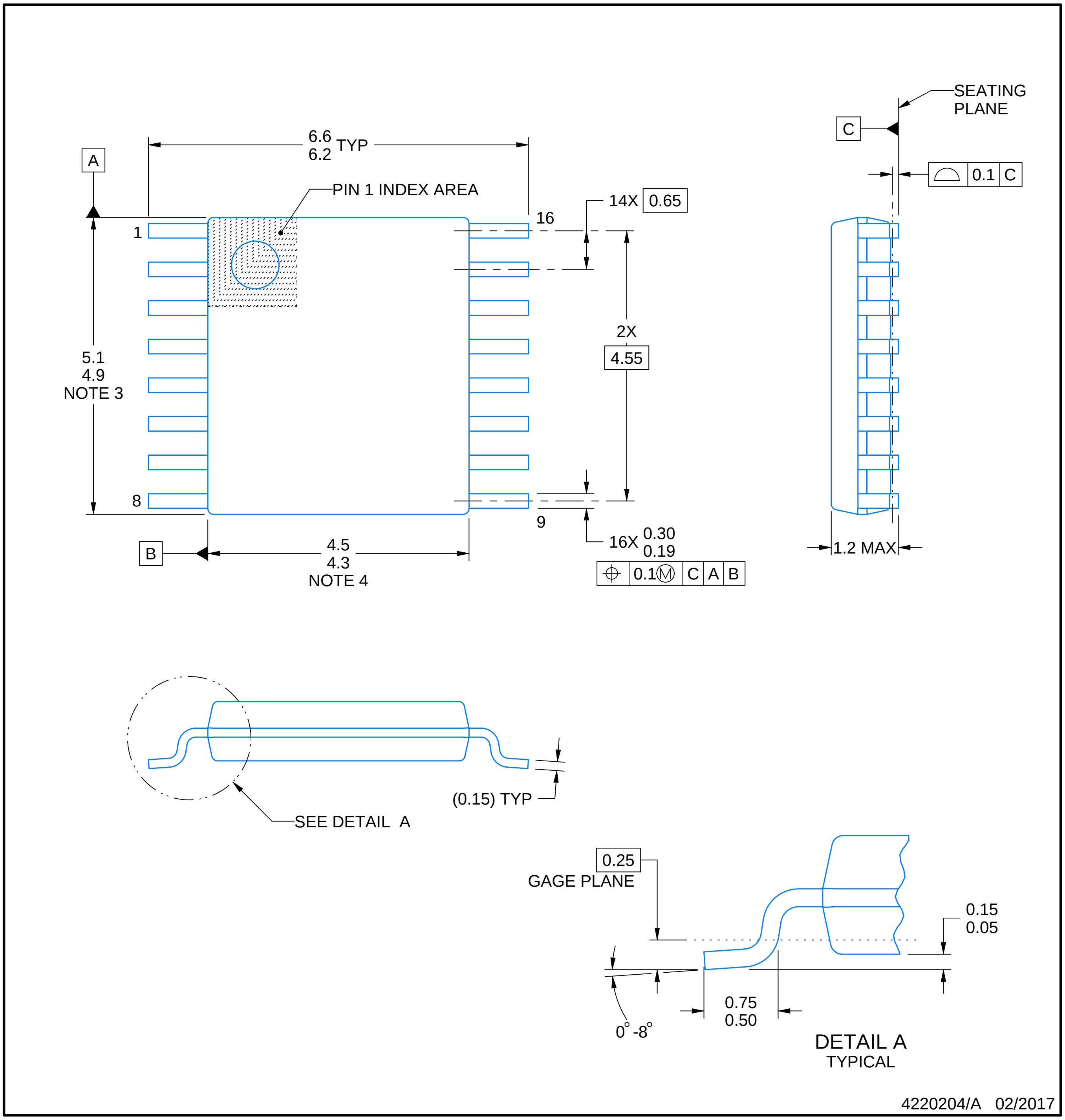


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS1050PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS1050PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

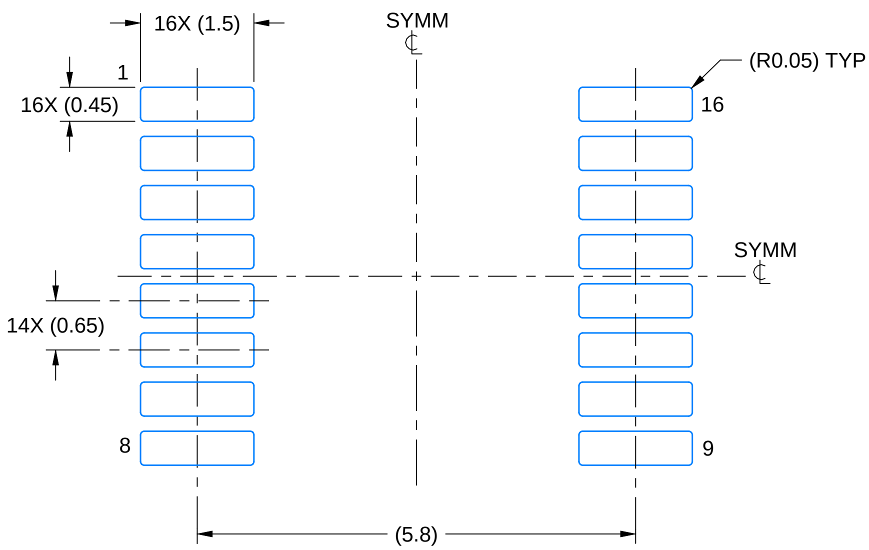


SMALL OUTLINE PACKAGE

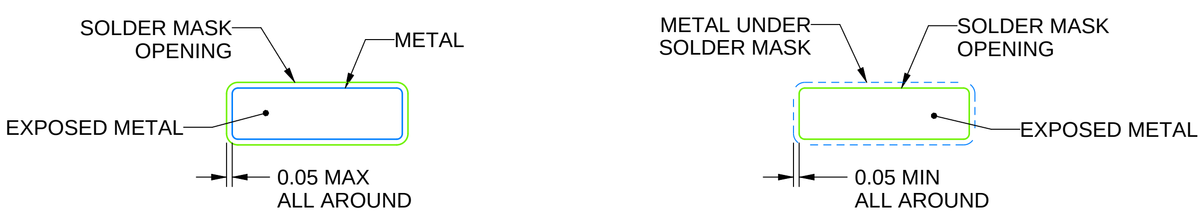


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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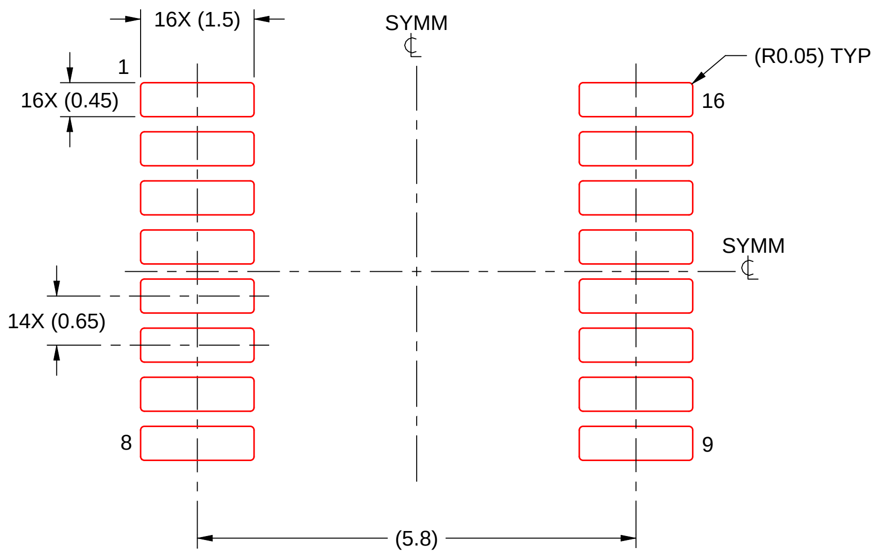
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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