# TPS6518xx PMIC for E Ink® Vizplex™-Enabled Electronic Paper Display

## 1 Features

- Single-Chip Power Management Solution for E Ink® Vizplex™ Electronic Paper Displays
- Generates Positive and Negative Gate and Source Driver Voltages and Back-Plane Bias from a Single, Low-Voltage Input Supply
- 3-V to 6-V Input Voltage Range
- Boost Converter for Positive Rail Base
- Inverting Buck-Boost Converter for Negative Rail Base
- Two Adjustable LDOs for Source Driver Supply
  - LDO1: 15 V, 120 mA (VPOS)
  - LDO2: –15 V, 120 mA (VNEG)
- Accurate Output Voltage Tracking
  - VPOS - VNEG = ±50 mV
- Two Charge Pumps for Gate Driver Supply
  - CP1: 22 V, 10 mA (VDDH)
  - CP2: –20 V, 12 mA, (VEE)
- Adjustable VCOM Driver for Accurate Panel-Backplane Biasing
  - –0.3 V to –2.5 V
  - ±1.5% Accuracy (±18 mV)
  - 8-Bit Control (11-mV Nominal Step Size)
  - 15-mA Maximum Integrated Switch
- Integrated 3.3-V Power Switch for Disabling System Power Rail
- Thermistor Monitoring
  - –10°C to +85°C Temperature Range
  - ±1°C Accuracy from 0°C to 50°C
- $I^2C$ Serial Interface
  - Slave Address 0x48h (1001000)
- Flexible Power-Up Sequencing
- Interrupt and Sleep Mode Support
- Thermally-Enhanced Package for Efficient Heat Management
  (48-Pin 7 mm × 7 mm × 0.9 mm VQFN)

## 2 Applications

- Power Supply for Active Matrix E Ink Vizplex Panels
- EPD Power Supply
- E-Book Readers
- EPSON® S1D13522 (ISIS) Timing Controller
- EPSON S1D13521 (Broadsheet) Timing Controller
- Application Processors With Integrated or Software Timing Controller (OMAP™)

## 3 Description

The TPS6518x and TPS65181xB family of devices are single-chip power supplies designed to for E Ink Vizplex displays used in portable e-reader applications and support panel sizes up to 9.7 inches. Two high-efficiency DC–DC boost converters generate ±17-V rails which are boosted to 22 V and –20 V by two change pumps to provide the gate driver supply for the Vizplex panel. Two tracking LDOs create the ±15-V source driver supplies which support up to 120-mA of output current. All rails are adjustable through the $I^2C$ interface to accommodate specific panel requirements.

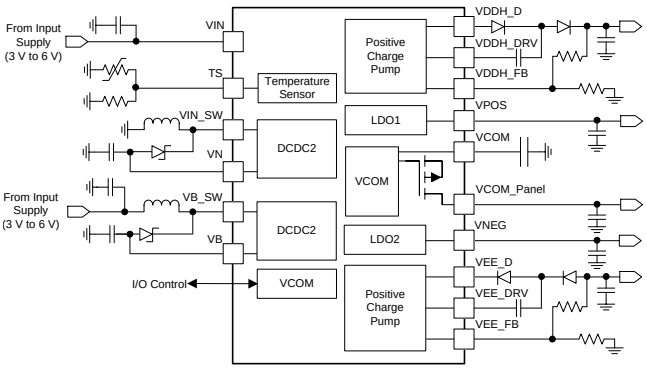
**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS65180(2) | VQFN (48) | 7.00 mm × 7.00 mm |
| TPS65180B | | |
| TPS65181(2) | | |
| TPS65181B | | |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Not recommended for new design (NRND).

**Typical Application Schematic**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision F (February 2011) to Revision G | Page |
|---|---|
| • Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. | 1 |

## 5 Description (continued)

Accurate back-plane biasing is provided by a linear amplifier and can be adjusted either by an external resistor or the $I^2C$ interface. The VCOM driver can source or sink current depending on panel condition. For automatic VCOM adjustment in production line, VCOM can be set from –0.3 V to –2.5 V with 8-bit control through the serial interface. The power switch is integrated to isolate VCOM driver from E Ink® panel.

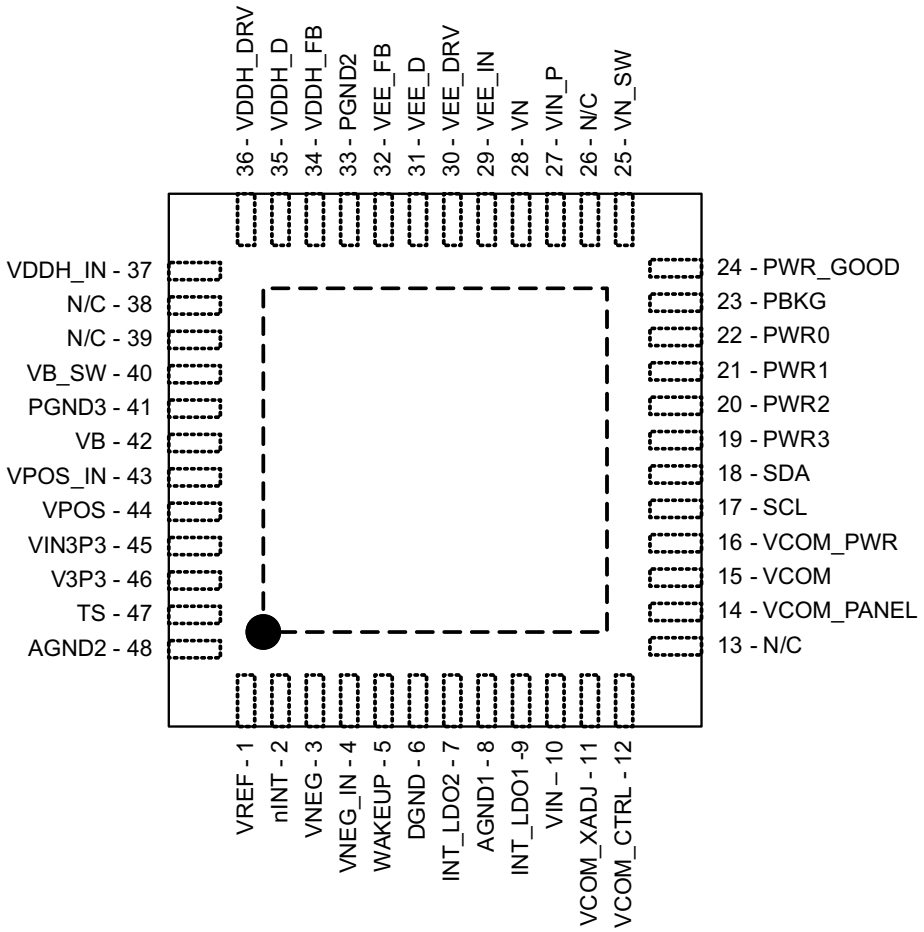
The TPS6518x and TPS65181xB devices provide precise temperature measurement function to monitor the panel temperature during operation. The TPS65180 and TPS65180B requires the host processor to trigger the temperature acquisition through an $I^2C$ write whereas the TPS65181 and TPS65181B automatically updates the temperature every 60 s.

## 6 Device Comparison Table

| FUNCTION | TPS65180<br>TPS65180B | TPS65181<br>TPS65181B |
|---|---|---|
| Compatibility | EPSON ISIS (S1D113522) | EPSON ISIS (S1D113522) |
| | | EPSON Broadsheet (S1D13521) |
| | OMAP | OMAP |
| | ST | ST |
| Temperature sensor | Triggered by host | Automatically triggers every 60 s |
| $I^2C$ interface | Standard | Supports standard and Broadsheet protocol |
| Fault recovery | INT register must be read before rails can be re-enabled after a fault | Interrupts are automatically reset when faults clear. No need to read INT register. |
| VCOM adjust default | $I^2C$ control | External potentiometer |

# 7 Pin Configuration and Functions

**RGZ Package**
**48-Pin VQFN With Exposed Thermal Pad**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | VREF | O | Filter pin for 2.25-V internal reference to ADC |
| 2 | nINT | O | Open-drain interrupt pin (active low) |
| 3 | VNEG | O | Negative supply output pin for panel source drivers |
| 4 | VNEG_IN | I | Input pin for LDO2 (VNEG) |
| 5 | WAKEUP | I | Wake-up pin (active high). Pull this pin high to wake up from sleep mode. |
| 6 | DGND | — | Digital ground |
| 7 | INT_LDO2 | O | Internal supply (digital circuitry) filter pin |
| 8 | AGND1 | — | Analog ground for general analog circuitry |
| 9 | INT_LDO1 | O | Internal supply (analog circuitry) filter pin |
| 10 | VIN | I | Input power supply to general circuitry |
| 11 | VCOM_XADJ | I | Analog input for conventional VCOM setup method. Tie this pin to ground if VCOM is set through $I^2C$ interface. |
| 12 | VCOM_CTRL | I | VCOM_PANEL gate driver enable (active high) |

## Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 13 | N/C | — | Not connected |
| 14 | VCOM_PANEL | O | Panel common-voltage output pin |
| 15 | VCOM | O | Filter pin for panel common-voltage driver |
| 16 | VCOM_PWR | I | Internal supply input pin to VCOM buffer. Connect to the output of DCDC2. |
| 17 | SCL | I | Serial interface ($I^2C$) clock input |
| 18 | SDA | I/O | Serial interface ($I^2C$) data input and output |
| 19 | PWR3 | I | Enable pin for CP1 (VDDH) (active-high) |
| 20 | PWR2 | I | Enable pin for LDO1 (VPOS) (active-high) |
| 21 | PWR1 | I | Enable pin for CP2 (VEE) (active-high) |
| 22 | PWR0 | I | Enable pin for LDO2 (VNEG) and VCOM (active-high) |
| 23 | PowerPAD (PBKG) | — | Die substrate/thermal pad. Connect to VN with short, wide trace. Wide copper trace improves heat dissipation. PowerPad must not be connected to ground. |
| 24 | PWR_GOOD | O | Open-drain power-good output pin (active-low) |
| 25 | VN_SW | O | Inverting buck-boost converter switch out (DCDC2) |
| 26 | N/C | — | Not connected |
| 27 | VIN_P | I | Input power supply to inverting buck-boost converter (DCDC2) |
| 28 | VN | I | Feedback pin for inverting buck-boost converter (DCDC2) |
| 29 | VEE_IN | I | Input supply pin for CP1 (VEE) |
| 30 | VEE_DRV | O | Driver output pin for negative charge pump (CP2) |
| 31 | VEE_D | O | Base voltage output pin for negative charge pump (CP2) |
| 32 | VEE_FB | I | Feedback pin for negative charge pump (CP2) |
| 33 | PGND2 | — | Power ground for CP1 (VDDH) and CP2 (VEE) charge pumps |
| 34 | VDDH_FB | I | Feedback pin for positive charge pump (CP1) |
| 35 | VDDH_D | O | Base voltage output pin for positive charge pump (CP1) |
| 36 | VDDH_DRV | O | Driver output pin for positive charge pump (CP1) |
| 37 | VDDH_IN | I | Input supply pin for positive charge pump (CP1) |
| 38 | N/C | — | Not connected |
| 39 | N/C | — | Not connected |
| 40 | VB_SW | O | Boost converter switch out (DCDC1) |
| 41 | PGND3 | — | Power ground for DCDC1 |
| 42 | VB | I | Feedback pin for boost converter (DCDC1) |
| 43 | VPOS_IN | I | Input pin for LDO1 (VPOS) |
| 44 | VPOS | O | Positive supply output pin for panel source drivers |
| 45 | VIN3P3 | I | Input pin to 3.3-V power switch |
| 46 | V3P3 | O | Output pin of 3.3-V power switch |
| 47 | TS | I | Thermistor input pin. Connect a 10k NTC thermistor and a 43k linearization resistor between this pin and AGND2. |
| 48 | AGND2 | — | Reference point to external thermistor and linearization resistor |

# 8 Specifications

## 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| | Input voltage at VIN, VINP, VIN3P3 | –0.3 | 7 | V |
| | Ground pins to system ground | –0.3 | 0.3 | V |
| | Voltage range at SDA, SCL, WAKEUP, PWR3, PWR2, PWR1, PWR0, VCOM_CTRL, VDDH_FB, VEE_FB, PWR_GOOD, nINT | –0.3 | 3.6 | V |
| | VCOM_XADJ | –3.6 | 0.3 | V |
| | Voltage on VB, VB_SW, VPOS_IN, VDDH_IN | –0.3 | 20 | V |
| | Voltage on VN, VNEG_IN, VEE_IN, VCOM_PWR | –20 | 0.3 | V |
| | Voltage from VINP to VN_SW | –0.3 | 30 | V |
| | Peak output current | Internally limited | | mA |
| | Continuous total power dissipation | | 2 | W |
| $T_J$ | Operating junction temperature | –10 | 125 | °C |
| $T_A$ | Operating ambient temperature(3) | –10 | 85 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) TI recommends that copper plane in proper size on board be in contact with die thermal pad to dissipate heat efficiently. Thermal pad is electrically connected to PBKG, which is supposed to be tied to the output of buck-boost converter. Thus wide copper trace in the buck-boost output helps heat dissipated efficiently.

## 8.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| | Input voltage at VIN, VINP, VIN3P3 | 3 | 3.7 | 6 | V |
| | Voltage at SDA, SCL, WAKEUP, PWR3, PWR2, PWR1, PWR0, VCOM_CTRL, VDDH_FB, VEE_FB, VCOM_XADJ, PWR_GOOD, nINT | 0 | | 3.6 | V |
| $T_A$ | Operating ambient temperature | –10 | | 85 | °C |
| $T_J$ | Operating junction temperature | –10 | | 125 | °C |

## 8.4 Thermal Information

| THERMAL METRIC(1) | | TPS6518x TPS6518xB RGZ (VQFN) 48 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (2) | 30.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 16.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 7.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 7.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Estimated when mounted on high K JEDEC board per JESD 51-7 with thickness of 1.6 mm, 4 layers, size of 76.2 mm × 114.3 mm, and 2-oz. copper for top and bottom plane. Actual thermal impedance depends on PCB used in the application.

## 8.5 Electrical Characteristics

$V_{IN}$ = 3.7 V, $T_A$ = –10°C to 85ºC, Typical values are at $T_A$ = 25ºC (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT VOLTAGE** | | | | | | |
| $V_{IN}$ | Input voltage range | | 3 | 3.7 | 6 | V |
| $V_{UVLO}$ | Undervoltage lockout threshold | $V_{IN}$ falling | | 2.9 | | V |
| $V_{HYS}$ | Undervoltage lockout hysteresis | $V_{IN}$ rising | | 400 | | mV |
| **INPUT CURRENT** | | | | | | |
| $I_Q$ | Operating quiescent current into VIN | Device switching, no load | | 5.5 | | mA |
| $I_{STD}$ | Operating quiescent current into VIN | Device in standby mode | | 130 | | µA |
| $I_{SLEEP}$ | Shutdown current | Device in sleep mode | | 2.8 | 10 | µA |
| **INTERNAL SUPPLIES** | | | | | | |
| $VI_{NT\_LDO1}$ | Internal supply | | | 2.7 | | V |
| $V_{INT\_LDO2}$ | Internal supply | | | 2.7 | | V |
| $V_{REF}$ | Internal supply | | | 2.25 | | V |
| **DCDC1 (POSITIVE BOOST REGULATOR)** | | | | | | |
| $V_{IN}$ | Input voltage range | | 3 | 3.7 | 6 | V |
| $V_{OUT}$ | Output voltage range | | | 17 | | V |
| | DC set tolerance | | –5% | | 5% | |
| $I_{OUT}$ | Output current | | | | 160 | mA |
| $R_{DS(ON)}$ | MOSFET on resistance | $V_{IN}$ = 3.7 V | | 350 | | mΩ |
| $I_{LIMIT}$ | Switch current limit | | | 1.5 | | A |
| | Switch current accuracy | | –30% | | 30% | |
| $f_{SW}$ | Switching frequency | | | 1 | | MHz |
| L | Inductor | | | 2.2 | | µH |
| C | Capacitor | | | 2 × 4.7 | | µF |
| ESR | Capacitor ESR | | | 20 | | mΩ |
| **DCDC2 (INVERTING BUCK-BOOST REGULATOR)** | | | | | | |
| $V_{IN}$ | Input voltage range | | 3 | 3.7 | 6 | V |
| $V_{OUT}$ | Output voltage range | | | –17 | | V |
| | DC set tolerance | | –5% | | 5% | |
| $I_{OUT}$ | Output current | | | | 160 | mA |
| $R_{DS(ON)}$ | MOSFET on resistance | $V_{IN}$ = 3.7 V | | 350 | | mΩ |
| $I_{LIMIT}$ | Switch current limit | | | 1.5 | | A |
| | Switch current accuracy | | –30% | | 30% | |
| L | Inductor | | | 4.7 | | µH |
| C | Capacitor | | | 2 × 4.7 | | µF |
| ESR | Capacitor ESR | | | 20 | | mΩ |
| **LDO1 (VPOS)** | | | | | | |
| $V_{POS\_IN}$ | Input voltage range | | 16.15 | 17 | 17.85 | V |
| $V_{SET}$ | Output voltage set value | $V_{IN}$ = 17 V, $V_{POS\_SET[2:0]}$ = 0x0h to 0x7h | 14.25 | 15 | 15.75 | V |
| $V_{INTERVAL}$ | Output voltage set resolution | $V_{IN}$ = 17 V | | 250 | | mV |
| $V_{POS\_OUT}$ | Output voltage range | $V_{SET}$ = 15 V, $I_{LOAD}$ = 20 mA | 14.85 | 15 | 15.15 | V |
| $V_{OUTTOL}$ | Output tolerance | $V_{SET}$ = 15 V, $I_{LOAD}$ = 20 mA | –1% | | 1% | |
| $V_{DROPOUT}$ | Dropout voltage | $I_{LOAD}$ = 120 mA | | | 250 | mV |
| $V_{LOADREG}$ | Load regulation – DC | $I_{LOAD}$ = 10% to 90% | | | 1% | |
| $I_{LOAD}$ | Load current range | | | 120 | | mA |

## Electrical Characteristics (continued)

$V_{IN}$ = 3.7 V, $T_A$ = –10°C to 85ºC, Typical values are at $T_A$ = 25ºC (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{LIMIT}$ | Output current limit | | 200 | | | mA |
| $T_{SS}$ | Soft-start time | | | 1 | | ms |
| C | Recommended output capacitor | | | 4.7 | | µF |
| **LDO2 (VNEG)** | | | | | | |
| $V_{NEG\_IN}$ | Input voltage range | | –17.85 | –17 | –16.15 | V |
| $V_{SET}$ | Output voltage set value | $V_{IN}$ = –17 V, $V_{NEG\_SET[2:0]}$ = 0x0h to 0x7h | –15.75 | –15 | –14.25 | V |
| $V_{INTERVAL}$ | Output voltage set resolution | $V_{IN}$ = –17 V | | 250 | | mV |
| $V_{NEG\_OUT}$ | Output voltage range | $V_{SET}$ = –15 V, $I_{LOAD}$ = –20 mA | –15.15 | –15 | –14.85 | V |
| $V_{OUTTOL}$ | Output tolerance | $V_{SET}$ = –15 V, $I_{LOAD}$ = –20 mA | –1% | | 1% | |
| $V_{DROPOUT}$ | Dropout voltage | $I_{LOAD}$ = 120 mA | | | 250 | mV |
| $V_{LOADREG}$ | Load regulation – DC | $I_{LOAD}$ = 10% to 90% | | | 1% | |
| $I_{LOAD}$ | Load current range | | | 120 | | mA |
| $I_{LIMIT}$ | Output current limit | | 200 | | | mA |
| $T_{SS}$ | Soft-start time | | | 1 | | ms |
| C | Recommended output capacitor | | | 4.7 | | µF |
| **LD01 (POS) AND LDO2 (VNEG) TRACKING** | | | | | | |
| $V_{DIFF}$ | Difference between VPOS and VNEG | $V_{SET}$ = ±15 V, $I_{LOAD}$ = ±20 mA, 0°C to 60°C | –50 | | 50 | mV |
| **VCOM DRIVER** | | | | | | |
| $V_{COM}$ | Accuracy | $V_{COM\_SET[7:0]}$ = 0x74h (–1.25 V) $V_{IN}$ = 3.4 V to 4.2 V, no load | –0.8% | | 0.8% | |
| | | $V_{COM\_SET[7:0]}$ = 0x74h (–1.25 V) $V_{IN}$ = 3.0 V to 6.0 V, no load | –1.5% | | 1.5% | |
| | Output voltage range | | –2.5 | | –0.3 | V |
| | Resolution | $V_{COM\_ADJ}$ = 1 V, 1 LSB | | 11 | 17 | mV |
| G | $V_{COM}$ gain ($V_{COM\_XADJ}/V_{COM}$) | $V_{COM\_ADJ}$ = 0 V | | 1 | | V/V |
| **VCOM SWITCH** | | | | | | |
| $T_{ON}$ | Switch ON-time | $V_{COM}$ = –1.25 V, $V_{COM\_PANEL}$ = 0 V $C_{VCOM}$ = 4.7 µF, $C_{VCOM\_PANEL}$ = 4.7 µF | | | 1 | ms |
| $R_{DS(ON)}$ | MOSFET ON-resistance | $V_{COM}$ = –1.245 V, $I_{COM}$ = 30 mA | | 20 | 35 | Ω |
| $I_{LIMIT}$ | MOSFET current limit | Not tested in production | | 200 | | mA |
| $I_{SWLEAK}$ | Switch leakage current | $V_{COM}$ = 0 V, $V_{COM\_PANEL}$ = –2.5 V | | | 8.3 | nA |
| **VIN3P3 TO V3P3 SWITCH** | | | | | | |
| $R_{DS(ON)}$ | MOSFET ON-resistance | $V_{IN3P3}$ = 3.3 V, $I_D$ = 2 mA | | 50 | | Ω |
| **CP1 (VDDH) CHARGE PUMP** | | | | | | |
| $V_{DDH\_IN}$ | Input voltage range | | 16.15 | 17 | 17.85 | V |
| $V_{FB}$ | Feedback voltage | | | 1 | | V |
| | Accuracy | | –3% | | 3% | |
| $V_{DDH\_OUT}$ | Output voltage range | $V_{SET}$ = 22 V, $I_{LOAD}$ = 2 mA | 21 | 22 | 23 | V |
| $I_{LOAD}$ | Load current range | | | | 10 | mA |
| $f_{SW}$ | Switching frequency | | | 560 | | KHz |
| $C_D$ | Recommended driver capacitor | | | 10 | | nF |
| $C_O$ | Recommended output capacitor | | | 4.7 | | µF |
| **CP2 (VEE) NEGATIVE CHARGE PUMP** | | | | | | |
| $V_{EE\_IN}$ | Input voltage range | | –17.75 | –17 | –16.15 | V |

## Electrical Characteristics (continued)

$V_{IN}$ = 3.7 V, $T_A$ = –10°C to 85ºC, Typical values are at $T_A$ = 25ºC (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{FB}$ | Feedback voltage | | | –1 | | V |
| | Accuracy | | –3% | | 3% | |
| $V_{EE\_OUT}$ | Output voltage range | $V_{SET}$ = –20 V, $I_{LOAD}$ = 3 mA | –21 | –20 | –19 | V |
| $I_{LOAD}$ | Load current range | | | | 12 | mA |
| $f_{SW}$ | Switching frequency | | | 560 | | KHz |
| $C_D$ | Recommended driver capacitor | | | 10 | | nF |
| $C_O$ | Recommended output capacitor | | | 4.7 | | µF |
| **THERMISTOR MONITOR**(1) | | | | | | |
| $A_{TMS}$ | Temperature to voltage ratio | Not tested in production | | –0.0158 | | V/°C |
| $Offset_{TMS}$ | Offset | Temperature = 0°C | | 1.575 | | V |
| $V_{TMS\_HOT}$ | Temp hot trip voltage (T = 50°C) | TEMP_HOT_SET = 0x8C | | 0.768 | | V |
| $V_{TMS\_COOL}$ | Temp hot escape voltage (T = 45°C) | TEMP_COOL_SET = 0x82 | | 0.845 | | V |
| $V_{TMS\_MAX}$ | Maximum input level | | | 2.25 | | V |
| $R_{NTC\_PU}$ | Internal pullup resistor | | | 7.307 | | KΩ |
| $R_{LINEAR}$ | External linearization resistor | | | 43 | | KΩ |
| $ADC_{RES}$ | ADC resolution | Not tested in production, 1 bit | | 8.75 | | mV |
| $ADC_{DEL}$ | ADC conversion time | Not tested in production | | 19 | | µs |
| $TMST_{TOL}$ | Accuracy | Not tested in production | –2 | | 2 | LSB |
| **LOGIC LEVELS AND TIMING CHARTERISTICS (SCL, SDA, nINT, PWR_GOOD, PWRx, WAKEUP)** | | | | | | |
| $V_{OL}$ | Output low threshold level | $I_O$ = 3 mA, sink current (SDA, nINT, PWR_GOOD) | | | 0.4 | V |
| $V_{IL}$ | Input low threshold level | | | | 0.4 | V |
| $V_{IH}$ | Input high threshold level | | 1.2 | | | V |
| $I_{(bias)}$ | Input bias current | $V_{IO}$ = 1.8 V | | | 1 | µA |
| $t_{low,WAKEUP}$ | WAKEUP low time | minimum low time for WAKEUP pin | 150 | | | ms |
| $f_{SCL}$ | SCL clock frequency | | | | 400 | KHz |
| **OSCILLATOR** | | | | | | |
| $f_{OSC}$ | Oscillator frequency | | | 9 | | MHz |
| | Frequency accuracy | $T_A$ = –40°C to 85°C | –10% | | 10% | |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SHTDWN}$ | Thermal trip point | | | 150 | | °C |
| | Thermal hysteresis | | | 20 | | °C |

(1) 10-kΩ Murata NCP18XH103F03RB thermistor (1%) in parallel with a linearization resistor (43 kΩ, 1%) are used at TS pin for panel temperature measurement.

## 8.6 Data Transmission Timing

$V_{BAT}$ = 3.6 V ±5%, $T_A$ = 25ºC, $C_L$ = 100 pF (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{(SCL)}$ | Serial clock frequency | | 100 | | 400 | KHz |
| $t_{HD;STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | SCL = 100 KHz | 4 | | | µs |
| | | SCL = 400 KHz | 600 | | | ns |
| $t_{LOW}$ | LOW period of the SCL clock | SCL = 100 KHz | 4.7 | | | µs |
| | | SCL = 400 KHz | 1.3 | | | |
| $t_{HIGH}$ | HIGH period of the SCL clock | SCL = 100 KHz | 4 | | | µs |
| | | SCL = 400 KHz | 600 | | | ns |
| $t_{SU;STA}$ | Set-up time for a repeated START condition | SCL = 100 KHz | 4.7 | | | µs |
| | | SCL = 400 KHz | 600 | | | ns |
| $t_{HD;DAT}$ | Data hold time | SCL = 100 KHz | 0 | | 3.45 | µs |
| | | SCL = 400 KHz | 0 | | 900 | ns |
| $t_{SU;DAT}$ | Data set-up time | SCL = 100 KHz | 250 | | | ns |
| | | SCL = 400 KHz | 100 | | | |
| $t_r$ | Rise time of both SDA and SCL signals | SCL = 100 KHz | | | 1000 | ns |
| | | SCL = 400 KHz | | | 300 | |
| $t_f$ | Fall time of both SDA and SCL signals | SCL = 100 KHz | | | 300 | ns |
| | | SCL = 400 KHz | | | 300 | |
| $t_{SU;STO}$ | Set-up time for STOP condition | SCL = 100 KHz | 4 | | | µs |
| | | SCL = 400 KHz | 600 | | | ns |
| $t_{BUF}$ | Bus free time between stop and start condition | SCL = 100 KHz | 4.7 | | | µs |
| | | SCL = 400 KHz | 1.3 | | | |
| $t_{SP}$ | Pulse width of spikes which mst be suppressed by the input filter | SCL = 100 KHz | n/a | | n/a | ns |
| | | SCL = 400 KHz | 0 | | 50 | |

## 8.7 Typical Characteristics

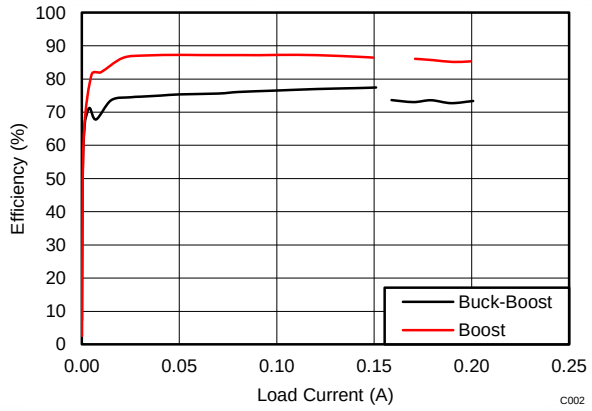



**Figure 1. Efficiency vs Load Current**

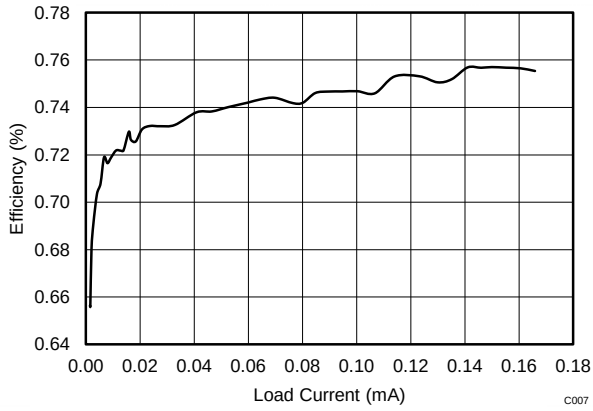



**Figure 2. Load Current vs Efficiency**

# 9 Detailed Description

## 9.1 Overview

The TPS6518x and TPS65181xB family of devices provides two adjustable LDOs, inverting buck-boost converter, boost converter, thermistor monitoring, and flexible power-up and power-down sequencing. The system can be supplied by a regulated input voltage ranging from 3 V to 6 V. The device is characterized across a –10°C to 85°C temperature range, best suited for personal electronic applications.

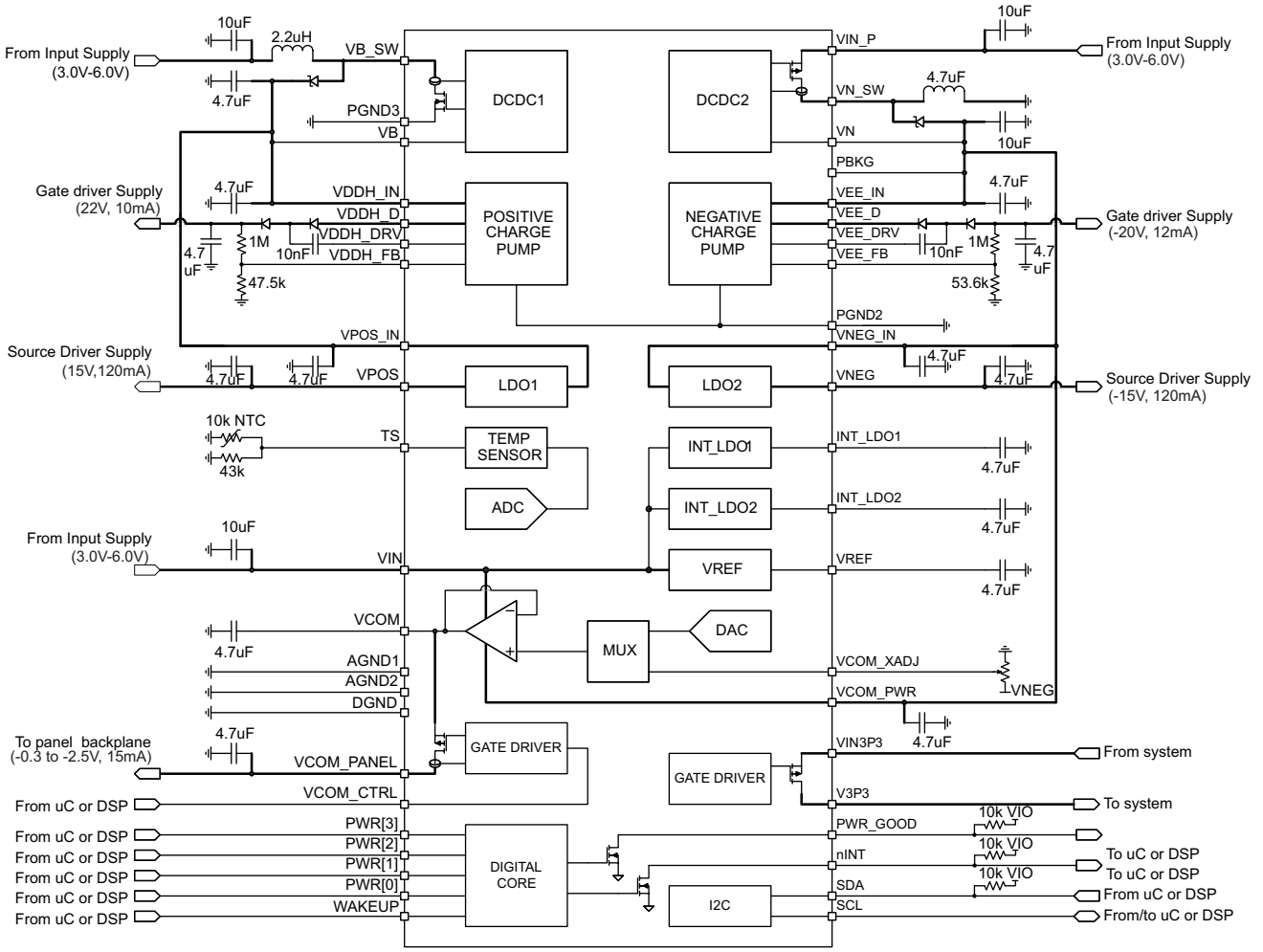
The $I^2C$ interface provides comprehensive features for using the TPS6518x and TPS65181xB family of devices. All rails can be enabled or disabled. Power-up and power-down sequences can also be programmed through the $I^2C$ interface, as well as thermistor and interrupt configurations. Voltage adjustment can also be controlled by the $I^2C$ interface. The adjustable LDOs can supply up to 120 mA of current. The default output voltages for each LDO can be adjusted through the $I^2C$ interface. LDO1 (VPOS) and LDO2 (VNEG) track each other in a way that they are of opposite sign but same magnitude. The sum of VLDO1 and VLOD2 is guaranteed to be less than 50 mV.

There are two charge pumps: VDDH and VEE 10 mA and 12 mA respectively. These charge pumps boost the DC-DC boost converters ±16-V rails to provide a gate channel supply. The power-good functionality is open-drain output, if any of the four power rails (CP1, CP2, LDO1, LDO2) are not in regulation, encounters a fault, or is disabled the pin is pulled low. PWR_GOOD remains low if one of the rails is not enabled by the host and only after all rails are in regulation PWR_GOOD is released to Hi-Z state (pulled up by external resistor).

The TPS6518x and TPS65181xB family of devices provides circuitry to bias and measure an external NTC to monitor the display panel temperature in a range from –10°C to 85°C with and accuracy of ±1°C from 0°C to 50°C. Temperature measurements are triggered by the controlling host and the last temperature reading is always stored in the TMST_VALUE register.

Interrupts are issued when the temperature exceeds the programmable HOT, or drops below the programmable COLD threshold, or when the temperature has changed by more than a user-defined threshold from the baseline value.

## 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Modes of Operation

The TPS6518x and TPS65181xB have three modes of operation, SLEEP, STANDBY, and ACTIVE. SLEEP mode is the lowest-power mode in which all internal circuitry is turned off. In STANDBY, all power rails are shut down but the device is ready to accept commands through PWR[3:0] pins and/or $I^2C$ interface. In ACTIVE mode one or more power rails are enabled.

**SLEEP** This is the lowest power mode of operation. All internal circuitry is turned off, registers are reset to default values and the device does not respond to $I^2C$ communications. TPS6518x and TPS65181xB enter SLEEP mode whenever WAKEUP pin is pulled low.

**STANDBY** In STANDBY all internal support circuitry is powered up and the device is ready to accept commands either through GPIO or $I^2C$ control but none of the power rails are enabled. To enter STANDBY mode the WAKEUP pin must be pulled high and all PWRx pins must be pulled low or the STANDBY bit of the ENABLE register must be set high. The device also enters STANDBY mode if input undervoltage lockout (UVLO), positive boost undervoltage (VB_UV), or inverting buck-boost undervoltage (VN_UV) is detected, or thermal shutdown occurs.

**ACTIVE** The device is in ACTIVE mode when any of the output rails are enabled and no fault condition is present. This is the normal mode of operation while the device is powered up. In ACTIVE mode, a falling edge on any PWRx pin shuts down and a rising edge powers up the corresponding rail.

### 9.3.2 Mode Transisitons

**SLEEP → ACTIVE** WAKEUP pin is pulled high (rising edge) with any PWRx pin high. Rails come up in the order defined by the PWR_SEQx registers.

**SLEEP → STANDBY** WAKEUP pin is pulled high (rising edge) with all PWRx pins low. Rails remain down until one or more PWRx pin is pulled high.

**ACTIVE → SLEEP** WAKEUP pin is pulled low (falling edge). Rails are shut down in the reverse power-up order defined by PWR_SEQ registers.

**ACTIVE → STANDBY** WAKEUP pin is high. All PWRx pins are pulled low (falling edge). Rails shut down in the order in which PWRx pins are pulled low. In the event of thermal shut down (TSD), undervoltage lockout (UVLO), positive boost or inverting buck-boost undervoltage (UV), or when STANDBY bit is set to 1, the device shuts down all rails in the reverse power-up order defined by the PWR_SEQx registers.

**STANDBY → ACTIVE** WAKEUP pin is high and any PWRx pin is pulled high (rising edge). Rails come up in the same order as PWRx pins are pulled high. Alternatively, if ACTIVE bit is set to 1, output rails power up in the order defined by the PWR_SEQx registers.

**STANDBY → SLEEP** WAKEUP pin is pulled low (falling edge) while none of the output rails are enabled.

## Feature Description (continued)

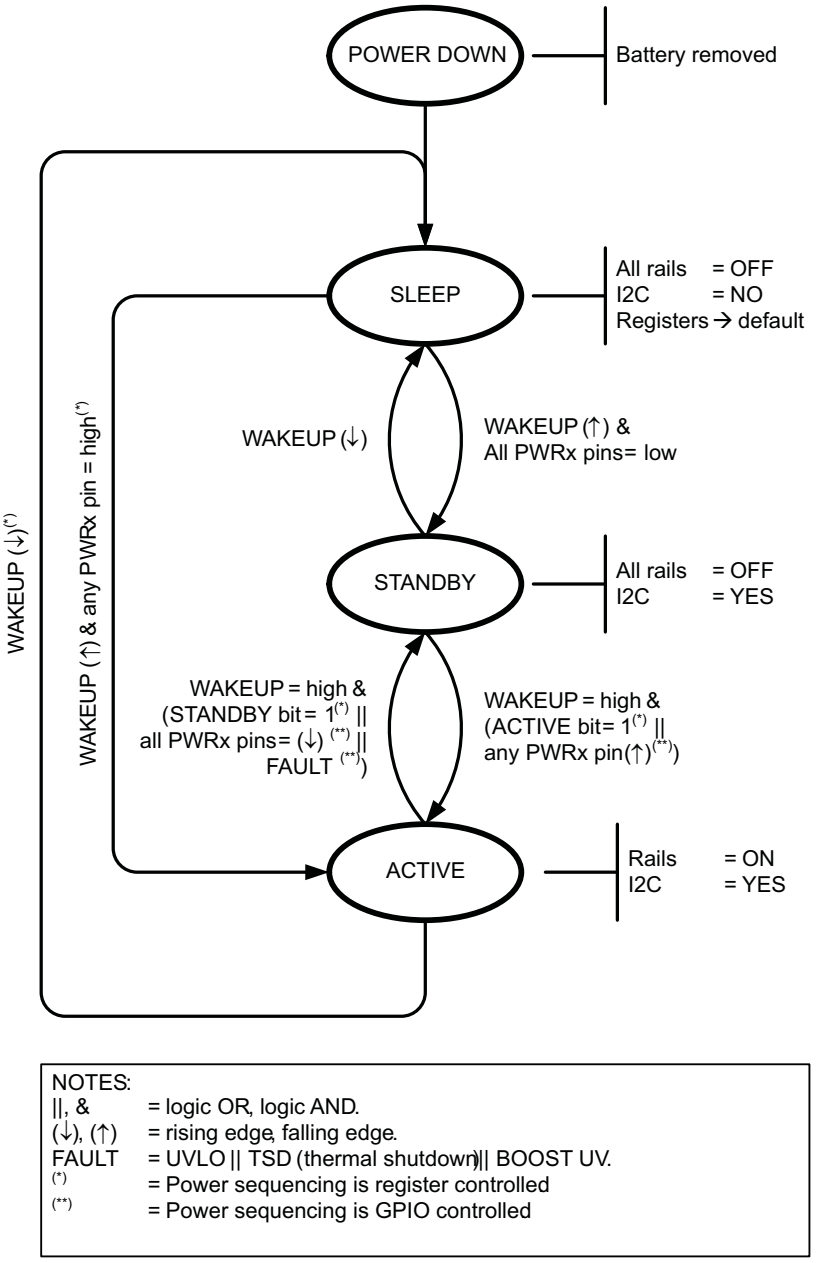



**Figure 3. Global State Diagram**

### 9.3.3 Wake-Up and Power Up Sequencing

The TPS6518x and TPS65181xB support flexible power-up sequencing through GPIO control using the PWR3, 2, 1, 0 pins or $I^2C$ control using the PWR_SEQ0, 1, 2 registers. Using GPIO control, the output rails are enabled/disabled in the order in which the PWRx pins are asserted or de-asserted, respectively, and the power-up timing is controlled by the host only.

In $I^2C$ control mode the power-up and power-down order and timing are defined by user register settings. The default settings support the E Ink Vizplex panel and typically do not need to be charged by the user.

## Feature Description (continued)

### 9.3.4 GPIO Control

Under GPIO control the system host in E Ink Vizplex panel module enables the TPS6518x and TPS65181xB output rails by asserting the PWR0, PWR1, PWR2, PWR3 signals and the host has full control over the order and timing in which the output rails are powered up and down. Rails are in regulation 2 ms after their respective PWRx pin has been asserted with the exception of the first rail, which takes 6 ms to power up. The additional time is needed to power up the positive and inverting buck-boost regulator which need to be turned on before any other rail can be enabled. When all rails are enabled and in regulation the PWR_GOOD pin is released (pin status = Hi-Z and power-good line is pulled high by external pullup resistor). The PWRx pins are assigned to the rails as follows:

- PWR0: LDO2 (VNEG) and VCOM
- PWR1: CP2 (VEE)
- PWR2: LDO2 (VPOS)
- PWR3: CP1 (VDDH)

Rails are powered down whenever the host de-asserts the respective PWRx pin, and when all rails are disabled the device enters STANDBY mode. The next step is then to de-assert the WAKEUP pin to enter SLEEP mode which is the lowest-power mode of operation.

It is possible for the host to force the TPS6518x and TPS65181xB directly into SLEEP mode from ACTIVE mode by de-asserting the WAKEUP pin in which case the device follows the power-down sequence defined by the PWR_SEQx registers before entering SLEEP mode.

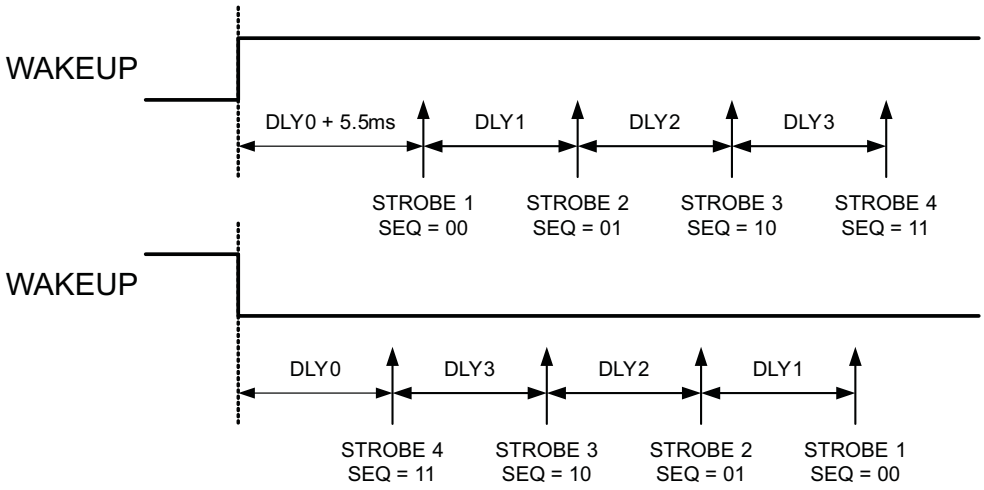
### 9.3.5 $I^2C$ Control

Under $I^2C$ control the power-up sequence is defined by the PWR_SEQx registers rather than through GPIO control. In SLEEP mode the TPS6518x and TPS65181xB are completely turned off, the $I^2C$ registers are reset, and the device does not accept any $I^2C$ transaction. Pull the WAKEUP pin high while all PWRx pins are held low and the device enters STANDBY mode which enables the $I^2C$ interface. Write to the PWR_SEQ0 register to define the order in which the output rails is enabled at power-up and to the PWR_SEQ1 and PWR_SEQ2 registers to define the power-up delays between rails. Finally, set the ACTIVE bit in the ENABLE register to 1 to execute the power-up sequence and bring up all power rails.

It is possible for the host to force the TPS6518x and TPS65181xB directly into ACTIVE mode from SLEEP mode by pulling the WAKEUP pin high while at least one of the PWRx pins is pulled high. In this case the default power-up sequence defined by the PWR_SEQx registers applies and the device starts powering up the rails 5.5 ms after the WAKEUP signal has been pulled high.

To power-down the device, set the STANDBY bit of the ENABLE register to 1 then the TPS6518x and TPS65181xB follows the reverse power-up sequence to bring down all power rails. While the sequencer is busy powering up the power rails, any activity on the PWRx pins is ignored. When all rails are up, any of the output rails can be disabled by applying a negative edge on the PWRx input pins, that is, if the host toggles the PWRx pin high-low or low-high-low, the respective rail is disabled regardless of how it has been enabled.

## Feature Description (continued)




**TOP: Power-up sequence is defined by assigning strobes to individual rails. STROBE1 is the first strobe to occur after WAKEUP has been pulled high and STROBE4 is the last event in the sequence. STROBES are assigned to rails in PWR_SEQ0 register and delays between states are defined in PWR_SEQ1 and PWR_SEQ2 registers.**
**BOTTOM: Power-down sequence follows reverse power-up sequence.**

**Figure 4. I²C Control**

## 9.4 Device Functional Modes

### 9.4.1 The FIX_RD_PTR Bit

The TPS65181 and TPS65181B devices support a special I²C mode, making them compatible with the EPSON Broadsheet S1D13521 timing controller. Standard I²C protocol requires the following steps to read data from a register:

1. Send device slave address, R/nW bit set low (write command)
2. Send register address
3. Send device slave address, R/nW set high (read command)
4. The slave responds with data from the specified register address.

The EPSON Broadsheet S1D13521 controller does not support I²C writes nor I²C reads from addressed registers (step 1. and 2. above) but needs to access the temperature data from the TPS65181 or TPS65181B TMST_VALUE register. To support Broadsheet based systems, the TPS65181 and TPS65181B automatically trigger temperature acquisition every 60s and stores the result in TMST_VALUE register. With the FIX_RD_PTR bit in the FIX_RD_POINTER register set to 1 the device responds to any I²C read command with data from the TMST_VALUE register. No write command with the register address is required and address auto increment feature is disabled in this mode. Therefore reading the temperature data is reduced to two steps:

1. Send device address, R/nW set high (read command)
2. Read the data from the slave. The slave responds with data from TMST_VALUE register address.

Write functionality is not affected by the FIX_RD_PTR bit and the main controller in the system maintains full control of the PMIC. Interrupts and error flags are issued and need to be handled the same way as for the TPS65180 and TPS65180B with two exceptions:

1. The FIX_RD_PTR bit in the FIX_RD_POINTER register needs to be set to 0 before the main controller can read any register different from the TMST_VALUE register.
2. Thermal Shutdown (TSD), positive boost undervoltage (VB_UV), inverting buck-boost undervoltage (VN_UV), and input undervoltage lockout (UVLO) interrupt bits do not have to be cleared before output rails can be re-enabled.

## Device Functional Modes (continued)

At system power-up the main processor sets up the PMIC by accessing the $I^2C$ registers and setting the control parameters as needed. When the system is setup correctly the main controller sets the FIX_READ_POINTER bit and the display controller can start accessing the temperature information. During normal operation the main controller can write to the PMIC at any time but before it can read access registers the FIX_READ_POINTER bit must be written 0.

## 9.5 Register Maps

**Table 1. Register Address Map**

| REGISTER | ADDRESS (HEX) | NAME | DEFAULT VALUE | DESCRIPTION |
|---|---|---|---|---|
| 0 | 0x00 | TMST_VALUE | N/A | Thermistor value read by ADC |
| 1 | 0x01 | ENABLE | 0001 1111 | Enable/disable bits for regulators |
| 2 | 0x02 | VP_ADJUST | 0010 0011 | Voltage settings for VPOS, VDDH |
| 3 | 0x03 | VN_ADJUST | 1010 0011 | Voltage settings for VNEG, VEE |
| 4 | 0x04 | VCOM_ADJUST | 0111 0100 | Voltage settings for VCOM |
| 5 | 0x05 | INT_ENABLE1 | 0111 0100 | Interrupt enable group1 |
| 6 | 0x06 | INT_ENABLE2 | 1111 1011 | Interrupt enable group2 |
| 7 | 0x07 | INT_STATUS1 | 0xxx xx00 | Interrupt status group1 |
| 8 | 0x08 | INT_STATUS2 | xxxx x0xx | Interrupt status group2 |
| 9 | 0x09 | PWR_SEQ0 | 1110 0100 | Power up sequence |
| 10 | 0x0A | PWR_SEQ1 | 0010 0010 | DLY0, DLY1 time set |
| 11 | 0x0B | PWR_SEQ2 | 0010 0010 | DLY2, DLY3 time set |
| 12 | 0x0C | TMST_CONFIG | 0010 0000 | Thermistor configuration |
| 13 | 0x0D | TMST_OS | 0011 0010 | Thermistor hot temp set |
| 14 | 0x0E | TMST_HYST | 0010 1101 | Thermistor cool temp set |
| 15 | 0x0F | PG_STATUS | 0000 0000 | Power-good status each rails |
| 16 | 0x10 | REVID | 0100 0001 | Device revision ID information |
| 17 | 0x11 | FIX_READ_POINTER | 0000 0000 | $I^2C$ read pointer control |

### 9.5.1 Thermistor Readout (TMST_VALUE) Register (Offset = 0x00h)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | TMST_VALUE[7:0] | | | | | | | |
| READ/WRITE | R | R | R | R | R | R | R | R |
| RESET VALUE | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

| FIELD NAME | BIT DEFINITION |
|---|---|
| TMST_VALUE[7:0] | Temperature read-out<br>1111 0110 – < -10°C<br>1111 0110 – -10°C<br>1111 0111 – -9°C<br>...<br>1111 1110 – -2°C<br>1111 1111 – -1 °C<br>0000 0000 – 0 °C<br>0000 0001 – 1°C<br>0000 0010 – 2°C<br>...<br>0001 1001 – 25°C<br>...<br>0101 0101 – 85°C<br>0101 0101 – > 85°C |

### 9.5.2 Enable (ENABLE) Register (Offset = 0x01h)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| **FIELD NAME** | ACTIVE | STANDBY | V3P3_SW_EN | VCOM_EN | VDDH_EN | VPOS_EN | VEE_EN | VNEG_EN |
| **READ/WRITE** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **RESET VALUE** | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

| FIELD NAME | BIT DEFINITION(1) |
|---|---|
| ACTIVE | STANDBY to ACTIVE transition bit<br>1 – Transition from STANDBY to ACTIVE mode. Rails power up as defined by PWR_SEQx registers.<br>0 – No effect<br>NOTE: After transition bit is cleared automatically. |
| STANDBY | ACTIVE to STANDBY transition bit<br>1 – Transition from ACTIVE to STANDBY mode. Rails power down as defined by PWR_SEQx registers.<br>0 – No effect<br>NOTE: After transition bit is cleared automatically. STANDBY bit has priority over AVTIVE. |
| V3P3_SW_EN | VIN3P3 to V3P3 switch enable<br>1 – Switch is ON<br>0 – Switch id OFF |
| VCOM_EN | VCOM buffer enable<br>1 – Enabled<br>0 – Disabled |
| VDDH_EN | VDDH charge pump enable<br>1 – Enabled<br>0 – Disabled |
| VPOS_EN | VPOS LDO regulator enable<br>1 – Enabled<br>0 – Disabled<br>NOTE: VPOS cannot be enabled before VNEG is enabled. |
| VEE_EN | VEE charge pump enable<br>1 – Enabled<br>0 – Disabled |
| VNEG_EN | VNEG LDO regulator enable<br>1 – Enabled<br>0 – Disabled<br>NOTE: When VNEG is disabled VPOS is also disabled. |

(1) Enable/disable bits for regulators are AND'd with PWRx signals.

### 9.5.3 Positive Voltage Rail Adjustment (VP_ADJUST) Register (Offset = 0x02h)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | Not used | VDDH_SET[2:0] | | | not used | VPOS_SET[2:0] | | |
| READ/WRITE | R | R/W | R/W | R/W | R | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

| FIELD NAME | BIT DEFINITION(1) |
|---|---|
| Not used | N/A |
| VDDH_SET[2:0] | VDDH voltage setting<br>000 – VDDH increase by 10%<br>001 – VDDH increase by 5%<br>010 – Nominal<br>011 – VDDH decrease by 5%<br>100 – VDDH decrease by 10%<br>101 – Reserved<br>110 – Reserved<br>111 – Reserved |
| Not used | N/A |
| VPOS_SET[2:0] | VPOS voltage setting<br>000 : \|VNEG\| - 0.75 V<br>001 : \|VNEG\| - 0.5 V<br>010 : \|VNEG\| - 0.25 V<br>011 : \|VNEG\|<br>100 : \|VNEG\| + 0.25 V<br>101 : \|VNEG\| + 0.5 V<br>110 : \|VNEG\| + 0.75 V<br>111 – Reserved<br>NOTE: For proper tracking of the VPOS and VNEG supply these bits must remain set at their default value of 011b. VPOS tracks VNEG automatically when VNEG_SET[2:0] bits of VN_ADJUST register are changed. |

(1) VDDH is decreased from set value defined by resistor divider. Decreased VDDH value must be within spec range.

### 9.5.4 Negative Voltage Rail Adjustment (VN_ADJUST) Register (Offset = 0x03h)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | VCOM_ADJ | VEE_SET[2:0] | | | Not used | VNEG_SET[2:0] | | |
| READ/WRITE | R/W | R/W | R/W | R/W | R | R/W | R/W | R/W |
| RESET VALUE | 1(1) | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

(1) TPS65180/TPS65180B: Bit defaults to 1; TPS65181/TPS65181B: Bit defaults to 0

| FIELD NAME | BIT DEFINITION |
|---|---|
| VCOM_ADJ | VCOM output adjustment method<br>0 – VCOM_XADJ pin<br>1 – $I^2C$ interface |
| VEE_SET[2:0](1) | VDDH voltage setting<br>000 – VEE decrease by 10%<br>001 – VEE decrease by 5%<br>010 – Nominal<br>011 – VEE increase by 5%<br>100 – VEE increase by 10%<br>101 – Reserved<br>110 – Reserved<br>111 – Reserved |
| not used | N/A |
| VNEG_SET[2:0] | VNEG voltage setting<br>000 – -15.75 V<br>001 – -15.50 V<br>010 – -15.25 V<br>011 – -15.00 V<br>100 – -14.75 V<br>101 – -14.50 V<br>110 – -14.25 V<br>111 – Reserved |

(1) VEE is decreased from set value defined by resistor divider. Decreased VEE value must be within spec range.

### 9.5.5 VCOM Adjustment (VCOM_ADJUST) Register (Offset = 0x04h)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | VCOM_SET[7:0] | | | | | | | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| VCOM_SET[7:0] | VCOM voltage adjustment<br>0000 0000 – 0 V<br>0000 0001 – 11 mV<br>0000 0010 – 22 mV<br>...<br>0111 0011 – 1239 mV<br>0111 0100 – 1250 mV<br>0111 0101 – 1261 mV<br>...<br>1111 1111 – 2750 mV<br>NOTE: step size is rounded to 11 mV. Theoretical step size is 2750 mV / 255 mV = 10.78 mV. Parametric performance is guranteed from -0.3 V to -2.5 V only. |

### 9.5.6 Interrupt Enable 1 (INT_ENABLE1) Register (Offset = 0x05h)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | Not used | TSD_EN | HOT_EN | TMST_HOT_EN | TMST_COOL_EN | UVLO_EN | Not used | Not used |
| READ/WRITE | R | R/W | R/W | R/W | R/W | R/W | R | R |
| RESET VALUE | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| Not used | N/A |
| TSD_EN | Thermal shutdown interrupt enable<br>1 – Enabled<br>0 – Disabled |
| HOT_EN | Thermal shutdown early warning enable<br>1 – Enabled<br>0 – Disabled |
| TMST_HOT_EN | Thermistor hot warning enable<br>1 – Enabled<br>0 – Disabled |
| TMST_COOL_EN | Thermistor hot escape interrupt enable<br>1 – Enabled<br>0 – Disabled |
| UVLO_EN | VIN undervoltage detect interrupt enable<br>1 – Enabled<br>0 – Disabled |
| Not used | N/A |
| Not used | N/A |

### 9.5.7 Interrupt Enable 2 (INT_ENABLE2) Register (Offset = 0x06h)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | VB_UV_EN | VDDH_UV_EN | VN_UV_EN | VPOS_UV_EN | VEE_UV_EN | not used | VNEG_UV_EN | EOC_EN |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R | R/W | R/W |
| RESET VALUE | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| VB_UV_EN | Positive boost converter undervoltage detect interrupt enable<br>1 – Enabled<br>0 – Disabled |
| VDDH_UV_EN | VDDH undervoltage detect interrupt enable<br>1 – Enabled<br>0 – Disabled |
| VN_UV_EN | Inverting buck-boost converter undervoltage detect interrupt enable<br>1 – Enabled<br>0 – Disabled |
| VPOS_UV_EN | VPOS undervoltage detect interrupt enable<br>1 – Enabled<br>0 – Disabled |
| VEE_UV_EN | VEE undervoltage detect interrupt enable<br>1 – Enabled<br>0 – Disabled |
| not used | N/A |
| VNEG_UV_EN | VNEG undervoltage detect interrupt enable<br>1 – Enabled<br>0 – Disabled |
| EOC_EN | ADC end of conversion interrupt enable<br>1 – Enabled<br>0 – Disabled |

### 9.5.8 Interrupt INT_STATUS1 (INT_STATUS1) Register (Offset = 0x07h)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| **FIELD NAME** | Not used | TSDN | HOT | TMST_HOT | TMST_COOL | UVLO | Not used | Not used |
| **READ/WRITE** | R | R | R | R | R | R | R | R |
| **RESET VALUE** | 0 | N/A | N/A | N/A | N/A | N/A | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| Not used | N/A |
| TSD | Thermal shutdown interrupt |
| HOT | Thermal shutdown early warning |
| TMST_HOT | Thermistor hot warning |
| TMST_COOL | Thermistor hot escape interrupt |
| UVLO | VIN undervoltage detect interrupt |
| Not used | N/A |
| Not used | N/A |

### 9.5.9 Interrupt Status 2 (INT_STATUS2) Register (Offset = 0x08h)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| **FIELD NAME** | VB_UV | VDDH_UV | VN_UV | VPOS_UV | VEE_UV | Not used | VNEG_UV | EOC |
| **READ/WRITE** | R | R | R | R | R | R | R | R |
| **RESET VALUE** | N/A | N/A | N/A | N/A | N/A | 0 | N/A | N/A |

| FIELD NAME | BIT DEFINITION(1) |
|---|---|
| VB_UV | Positive boost converter undervoltage detect interrupt |
| VDDH_UV | VDDH undervoltage detect interrupt |
| VN_UV | Inverting buck-boost converter undervoltage detect interrupt |
| VPOS_UV | VPOS undervoltage detect interrupt |
| VEE_UV | VEE undervoltage detect interrupt |
| not used | N/A |
| VNEG_UV | VNEG undervoltage detect interrupt |
| EOC | ADC end of conversion interrupt |

(1) Undervoltage detect bit is set if the corresponding rail does not come up 5 ms after it is enabled except for DCDC1 and 2 which are set 10 ms after they are enabled.

### 9.5.10 Power Sequence Register 0 (PWR_SEQ0) Register (Offset = 0x09h)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | VDDH_SEQ[1:0] | | VPOS_SEQ[1:0] | | VEE_SEQ[1:0] | | VNEG_SEQ[1:0] | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

| FIELD NAME | BIT DEFINITION(1) |
|---|---|
| VDDH_SEQ[1:0] | VDDH power-up/down order<br>00 – Power-up/down on STROBE1<br>01 – Power-up/down on STROBE2<br>10 – Power-up/down on STROBE3<br>11 – Power-up/down on STROBE4 |
| VPOS_SEQ[1:0] | VPOS power-up/down order<br>00 – Power-up/down on STROBE1<br>01 – Power-up/down on STROBE2<br>10 – Power-up/down on STROBE3<br>11 – Ppower-up/down on STROBE4 |
| VEE_SEQ[1:0] | VEE power-up/down order<br>00 – Power-up/down on STROBE1<br>01 – Power-up/down on STROBE2<br>10 – Power-up/down on STROBE3<br>11 – Power-up/down on STROBE4 |
| VNEG_SEQ[1:0] | VNEG power-up/down order<br>00 – Power-up/down on STROBE1<br>01 – Power-up/down on STROBE2<br>10 – Power-up/down on STROBE3<br>11 – Power-up/down on STROBE4 |

(1) Power-down sequence follows the reverse order of power-up.

### 9.5.11 Power Sequence Register 1 (PWR_SEQ1) Register (Offset = 0x0Ah)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | DLY1[3:0] | | | | DLY0[3:0] | | | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| DLY1[3:0] | DLY1 delay time set; defines the delay time from STROBE1 to STROBE2 during power-up and from STROBE2 to STROBE1 during power-down.<br>0000 – 0 ms<br>0001 – 1 ms<br>0010 – 2 ms<br>0011 – 3 ms<br>...<br>1110 – 14 ms<br>1111 – 15 ms |
| DLY0[3:0] | DLY0 delay time set; defines the delay time from WAKEUP high to STROBE1 during power-up and from WAKEUP low to STROBE4 during power-down.<br>0000 – 0 ms<br>0001 – 1 ms<br>0010 – 2 ms<br>0011 – 3 ms<br>...<br>1110 – 14 ms<br>1111 – 15 ms |

### 9.5.12 Power Sequence Register 2 (PWR_SEQ2) Register (Offset = 0x0Bh)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | DLY3[3:0] | | | | DLY2[3:0] | | | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| DLY3[3:0] | DLY3 delay time set; defines the delay time from STROBE3 to STROBE4 during power-up and from STROBE4 to STROBE3 during power-down.<br>0000 – 0 ms<br>0001 – 1 ms<br>0010 – 2 ms<br>0011 – 3 ms<br>...<br>1110 – 14 ms<br>1111 – 15 ms |
| DLY2[3:0] | DLY2 delay time set; defines the delay time from STROBE2 to STROBE3 during power-up and from STROBE3 to STROBE2 during power-down.<br>0000 – 0 ms<br>0001 – 1 ms<br>0010 – 2 ms<br>0011 – 3 ms<br>...<br>1110 – 14 ms<br>1111 – 15 ms |

### 9.5.13 Thermistor Configuration Register (TMST_CONFIG) (Offset = 0x0Ch)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| **FIELD NAME** | READ_ THERM | Not used | CONV_END | FAULT_QUE [1:0] | | FAULT_QUE _CLR | Not used | Not used |
| **READ/WRITE** | R/W | R | R | R/W | R/W | R/W | R | R |
| **RESET VALUE** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| READ_THERM | Read thermistor value<br>1 – Initiates temperature acquisition<br>0 – No effect<br>NOTE: bit is self-cleared after acquisition is completed |
| Not used | N/A |
| CONV_END | ADC conversion done flag<br>1 – Conversion is finished<br>0 – Conversion is not finished |
| FAULT_QUE [1:0] | Number of faults to detect before TMST_HOT interrupt is asserted<br>00 – 1 time<br>01 – 2 times<br>10 – 4 times<br>11 – 6 times |
| FAULT_QUE_CLR | Fault counter clear<br>1 – Clears fault counter<br>0 – Fault counter is cleared automatically if thermistor reading is less than TMST_HOT_SET[7:0] |
| Not used | N/A |
| Not used | N/A |

### 9.5.14 Thermistor Hot Threshold (TMST_OS) Register (Offset = 0x0Dh)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | TMST_HOT_SET[7:0] | | | | | | | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| TMST_HOT_SET[7:0] | Defined the thermistor HOT threshold<br>1000 0000 – Reserved<br>...<br>1111 0101 – Reserved<br>1111 0110 – -10°C<br>1111 0111 – -9°C<br>...<br>1111 1110 – -2°C<br>1111 1111 – -1°C<br>0000 0000 – 0°C<br>0000 0001 – 1°C<br>0000 0010 – 2°C<br>...<br>0001 1001 – 25°C<br>...<br>0011 0010 – 50°C<br>...<br>0101 0101 – 85°C<br>0101 0110 – Reserved<br>...<br>0111 1111 – Reserved |

### 9.5.15 Thermistor Cool Threshold (TMST_HYST) Register (Offset = 0x0Eh)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | TMST_COOL_SET[7:0] | | | | | | | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| TMST_HOT_SET[7:0] | Defined the thermistor HOT threshold<br>1000 0000 – Reserved<br>...<br>1111 0101 – Reserved<br>1111 0110 – -10°C<br>1111 0111 – -9°C<br>...<br>1111 1110 – -2°C<br>1111 1111 – -1°C<br>0000 0000 – 0°C<br>0000 0001 – 1°C<br>0000 0010 – 2°C<br>...<br>0001 1001 – 25°C<br>...<br>0010 1101 – 45°C<br>...<br>0101 0101 – 85°C<br>0101 0110 – Reserved<br>...<br>0111 1111 – Reserved |

### 9.5.16 Power-Good Status (PG_STATUS) Register (Offset = 0x0Fh)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | VB_PG | VDDH_PG | VN_PG | VPOS_PG | VEE_PG | Not used | VNEG_PG | Not used |
| READ/WRITE | R | R | R | R | R | R | R | R |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| VB_PG | Positive boost converter power-good |
| VDDH_PG | VDDH power-good |
| VN_PG | Inverting buck-boost power-good |
| VPOS_PG | VPOS power-good |
| VEE_PG | VEE power-good |
| not used | N/A |
| VNEG_PG | VNEG power-good |
| not used | N/A |

### 9.5.17 Revision and Version Control (REVID) Register (Offset = 0x10h)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | REVID[7:0] | | | | | | | |
| READ/WRITE | R | R | R | R | R | R | R | R |
| RESET VALUE | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| REVID [7:0] | 0101 0000 - TPS65180 1p1<br>0110 0000 - TPS65180 1p2<br>0111 0000 - TPS65180B (TPS65180 1p3)<br>1000 0000 - TPS65180B (TPS65180 1p4)<br>0101 0001 - TPS65181 1p1<br>0110 0001 - TPS65181 1p2<br>0111 0001 - TPS65181B (TPS65181 1p3)<br>1000 0001 - TPS65181B (TPS65181 1p4) |

### 9.5.18 I²C Read Pointer Control (FIX_READ_POINTER) Register (Offset = 0x11h) (TPS65181 and TPS65181B ONLY)

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | Not used | Not used | Not used | Not used | Not used | Not used | Not used | FIX_RD_PTR |
| READ/WRITE | R | R | R | R | R | R | R | R/W |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| Not used | N/A |
| Not used | N/A |
| Not used | N/A |
| Not used | N/A |
| Not used | N/A |
| Not used | N/A |
| Not used | N/A |
| FIX_RD_PTR | $I^2C$ read pointer control<br>1 – Read pointer is fixed to 0x00<br>0 – read pointer is controlled through $I^2C$ |

# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

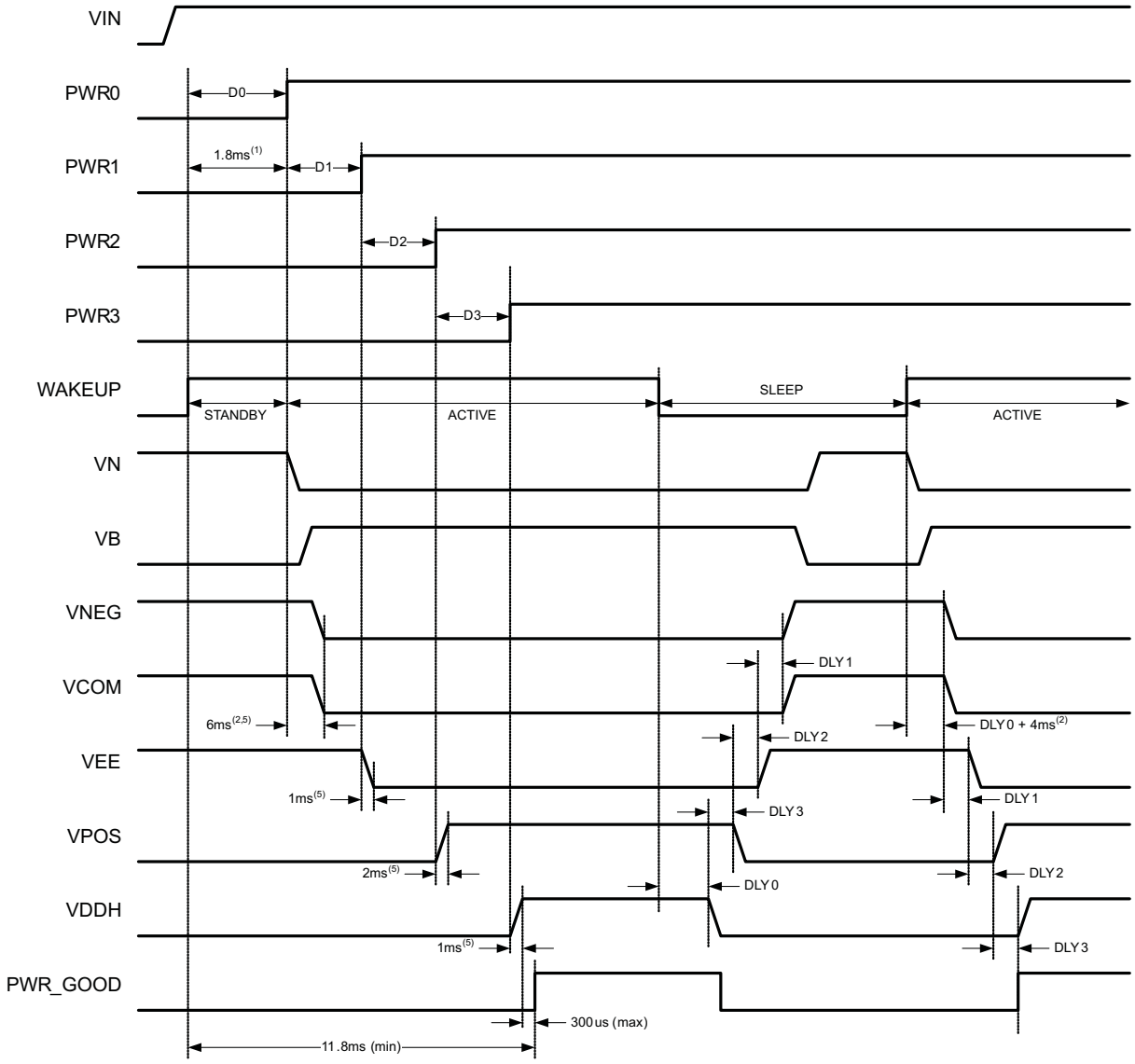
## 10.1 Application Information

### 10.1.1 Dependencies Between Rails

Charge pumps, LDOs, and VCOM driver are dependent on the positive and inverting buck-boost converters and several dependencies exist that affect the power-up sequencing. These dependencies are listed as follows:

1. Inverting buck-boost (DCDC2) must be in regulation before positive boost (DCDC1) can be enabled. Internally, DCDC1 enable is gated by DCDC2 power-good.
2. Positive boost (DCDC1) must be in regulation before LDO2 (VNEG) can be enabled. Internally LDO2 enable is gated DCDC1 power-good.
3. Positive boost (DCDC1) must be in regulation before VCOM can be enabled; Internally VCOM enable is gated by DCDC1 power-good.
4. Positive boost (DCDC1) must be in regulation before negative charge pump (CP2) can be enabled. Internally CP2 enable is gated by DCDC1 power-good.
5. Positive boost (DCDC1) must be in regulation before positive charge pump (CP1) can be enabled. Internally CP1 enable is gated by DCDC1 power-good.
6. LDO2 must be in regulation before LDO1 can be enabled. Internally LDO1 enable is gated by LDO2 power-good.
7. The minimum delay time between any two PWRx pins must be > 62.5 µs in order to follow the power up sequence defined by GPIO control. If any two PWRx pins are pulled up together (< 62.5 µs apart) or the sequencer tries to bring up the rails at the same time by assigning the same STROBE to rails in PWR_SEQ0 register, rails is staggered in a manner that an enable od the subsequent rail is gated by PG of a preceding rail. In this case, the default order of power-up is LDO2 (VNEG), CP2 (VEE), LDO1 (VPOS), and CP1(VDDH). If any two PWRx pins are pulled low together or the sequencer tries to bring down the rails at the same time by assigning the same STROBE to rails in PWR_SEQ0 register, then all rails goes down at the same time.

## Application Information (continued)




(1) Minimum delay time between WAKEUP rising edge and IC rady to accept I 2C transaction.
(2) It takes 2ms minimum for each internal boost regulator to start up before VNEG can be enabled .
(5) It takes up to 2ms for LDOs (VPOS,VNEG) and 1ms for charge pumps (VDDH,VEE), to reach their steady state after being enabled.
DLY 0-DLY 3 are power up/down delays defined in register PWR _SEQ 1 and PWR_SEQ2.

**In this example the first power-up sequence is determined by GPIO control (WAKEUP is pulled high while PWRx pins are low). Power-down and 2nd power-up sequence is controlled by register settings (WAKEUP pin is toggled with at least one PWR pin held high).**

**Figure 5. Power-Up and Power-Down Timing Diagram**

### 10.1.2 Soft-Start

Soft-start for DCDC1, DCDC2, LDO1, and LDO2 is accomplished by lowering the current limits during start-up. If DCDC1 or DCDC2 are unable to reach power-good status within 10 ms, the corresponding UV flag is set in the interrupt registers, the interrupt pin is pulled low, and the device enters STANDBY mode. LDO1, LDO2, positive and negative charge pumps have a 5-ms power-good timeout limit. If either rail is unable to power up within 5 ms after it has been enabled, the corresponding UV flag is set and the interrupt pin is pulled low. However, the device remains in ACTIVE mode in this case.

## Application Information (continued)

### 10.1.3 VCOM Adjustment

Through the I$^2$C interface the user can select between two methods of VCOM voltage adjustment:

1. Using the internal 8-bit DAC and register control.
2. Using an external voltage source (resistor divider) connected to the VCOM_XADJ pin.

### 10.1.4 VCOM Adjustment Through Register Control

By default the TPS65180x is setup for internal VCOM control through the I$^2$C interface. The default setting for the 8-bit DAC is 0x74h which results in 1.25 V ±0.8% for VCOM. VCOM can be adjusted up or down in steps of 11 mV (typical) by writing to the VCOM_ADJUST register. The output range for VCOM is limited to –0.3 V to –2.5 V.

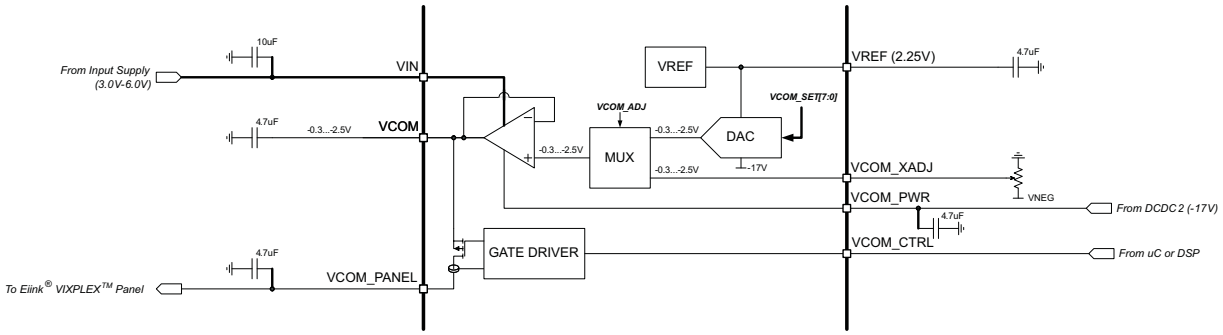



**Figure 6. Block Diagram of VCOM Circuit**

### 10.1.5 VCOM Adjustment Through External Potentiometer

VCOM can be adjusted by an external potentiometer by setting the VCOM_ADJ bit of the VN_ADJUST register to 0 and connecting a potentiometer to the VCOM_XADJ pin. The potentiometer must be connected between ground and a negative supply as shown in Figure 6. The gain from VCOM_XADJ to VCOM is 1 and therefore the voltage applied to VCOM_XADJ pin must range from –0.3 V to –2.5 V.

### 10.1.6 VPOS and VNEG Supply Tracking

LDO1 (VPOS) and LDO2 (VNEG) track each other in a way that they are of opposite sign but same magnitude. The sum of VLDO1 and VLOD2 is guaranteed to be < 50 mV. To ensure proper tracking of the supplies the VPOS_SET[2:0] bits of the VP_ADUST register must remain at the default setting of 010b. To adjust the VPOS and VNEG output voltage, write to the VN_ADJUST register only and keep the VPOS_SET[2:0] bits of the VP_ADUST register unchanged.

### 10.1.7 Fault Handling and Recovery

The TPS6518x and TPS65181xB monitor input and output voltages and die temperature and takes action if operating conditions are outside normal limits. Whenever the TPS6518x and TPS65181xB encounter:

- Thermal shutdown (TSD)
- Positive boost undervoltage (VB_UV)
- Inverting buck-boost undervoltage (VN_UV)
- Input undervoltage lockout (UVLO)

it shuts down all power rails and enter STANDBY mode. Shutdown follows the reverse power-up sequence defined by the PWR_SEQx registers. When a fault is detected, the PWR_GOOD and nINT pin are pulled low and the corresponding interrupt bit is set in the interrupt register.

Whenever the TPS6518x and TPS65181xB encounter undervoltage on VNEG (VNEG_UV), VPOS (VPOS_UV), VEE (VEE_UV) or VDDH (VDDH_UV) it shuts down the corresponding rail (plus any dependent rail) only and remain in ACTIVE mode, allowing the DCDC converters to remain up. Again, the PWR_GOOD and nINT pins is pulled low and the corresponding interrupt bit is set.

## Application Information (continued)

### 10.1.8 TPS65180 and TPS65180B Fault Handling

When a fault is detected, the TPS65180 and TPS65180B set the appropriate interrupt flags in the INT_STATUS1 and INT_STATUS2 registers and pull the INT pin low to signal an interrupt to the host processor. None of the power rails can be re-enabled before the host has read the INT_STATUSx bits and the fault has been removed. As the PWRx inputs are edge-sensitive, the host must also toggle the PWRx pins to re-enable the rails through GPIO control, that is, it must bring the PWRx pins low before asserting them again.

### 10.1.9 TPS65181 and TPS65181B Fault Handling

The TPS65181 and TPS65181 do not require the host processor to access the INT_STATUS registers before re-enabling the output rails. Rails can be re-enabled as soon as the fault condition has been removed. Again, as the PWRx inputs are edge-sensitive, the host must also toggle the PWRx pins to re-enable the rails through GPIO control, that is, it must bring the PWRx pins low before asserting them again.

### 10.1.10 Power-Good Pin

The power-good pin (PWR_GOOD) is an open-drain output that is pulled high when all four power rails (CP1, CP2, LDO1, LDO2) are in regulation and is pulled low if any of the rails encounters a fault. PWR_GOOD remains low if one of the rails is not enabled by the host and only after all rails are in regulation PWR_GOOD is released to Hi-Z state (pulled up by external resistor).

### 10.1.11 Interrupt Pin

The interrupt pin (nINT) is an open-drain output that is pulled low whenever one or more of the INT_STATUS1 or INT_STATUS2 bits are set. The nINT pin is released (returns to Hi-Z state) and fault bits are cleared when the register with the set bit has been read by the host. If the fault persists, the INT_pin is pulled low again after a maximum of 32 µs.

Interrupt events can be masked by re-setting the corresponding enable bit in the INT_ENABLE1 and INT_ENABLE2 register, that is, the user can determine which events cause the nINT pin to be pulled low. The status of the enable bits affects the nINT pin only and has no effect on any of the protection and monitoring circuits or the INT_STATUSx bits themselves.

Note that persisting fault conditions such as thermal shutdown can cause the nINT pin to be pulled low for an extended period of time which can keep the host in a loop trying to resolve the interrupt. If this behavior is not desired, set the corresponding mask bit after receiving the interrupt and keep polling the INT_STATUSx register to see when the fault condition has disappeared. After the fault is resolved, unmask the interrupt bit again.

### 10.1.12 Panel Temperature Monitoring

The TPS6518x and TPS65181xB provide circuitry to bias and measure an external negative temperature coefficient resistor (NTC) to monitor device temperature in a range from –10°C to 85°C with and accuracy of ±1°C from 0°C to 50°C. The TPS65180 and TPS65180B require the host to trigger the temperature acquisition through an $I^2C$ command whereas the TPS65181 and TPS65181B trigger the temperature acquisition automatically once every 60 s.

### 10.1.13 NTC Bias Circuit

Figure 7 below shows the block diagram of the NTC bias and measurement circuit. The NTC is biased from an internally generated 2.25-V reference voltage through an integrated 7.307-kΩ bias resistor. A 43-kΩ resistor is connected parallel to the NTC to linearize the temperature response curve. The circuit is designed to work with a nominal 10-kΩ NTC and achieves accuracy of ±1°C from 0°C to 50°C. The voltage drop across the NTC is digitized by a 10-bit SAR ADC and translated into an 8-bit two's complement by digital per Table 2.

## Application Information (continued)

**Table 2. ADC Output Value vs Termperature**

| TEMPERATURE | TMST_VALUE[7:0] |
|---|---|
| < –10°C | 1111 0110 |
| –10°C | 1111 0110 |
| –9°C | 1111 0111 |
| ... | ... |
| –2°C | 1111 1110 |
| –1°C | 1111 1111 |
| 0°C | 0000 0000 |
| 1°C | 0000 0001 |
| 2°C | 0000 0010 |
| ... | ... |
| 25°C | 0001 1001 |
| ... | |
| 85°C | 0101 0101 |
| > 85°C | 0101 0101 |

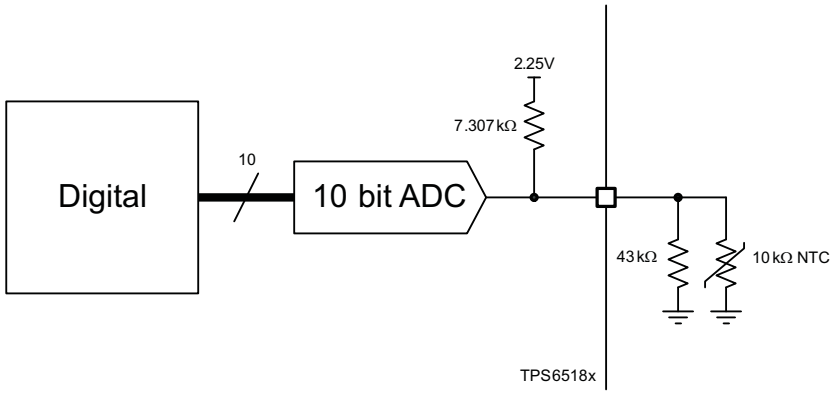



**Figure 7. NTC Bias and Measurement Circuit**

### 10.1.14 TPS65180 and TPS65180B Temperature Acquisition

The TPS65180 and TPS65180B require the host to trigger the temperature acquisition before reading the temperature value from register TMST_VALUE. A standard temperature measurement involves the following steps:

1. The host sets the READ_THERM bit of the TMST_CONFIG register to 1. This enabled the NTC bias circuit and internal ADC.
2. The analog to digital conversion is automatically started after a fixed 250-µs delay. While the conversion is in progress the CONV_END bit of the TMST_CONFIG register is held low and returns to 1 after the conversion result is available.
3. After the conversion is complete the READ_THERM bit is automatically reset, the EOC bit of the INT_STATUS2 register is set, and the interrupt pin (nINT) is pulled low.
4. The host services the interrupt by reading the INT_STATUS2 register. This clears the interrupt pin (nINT pin returns high). The host sees the EOC bit set and knows that the temperature data is available in the TMST_VALUE register.
5. The host reads the temperature data from the TMST_VALUE register.

### 10.1.15 TPS65181 and TPS65181B Temperature Acquisition

The TPS65181 and TPS65181B trigger temperature acquisition once every 60s to reduce the number of required $I^2C$ writes. The host or display timing controller can read the temperature at any time by accessing the TMST_VALUE register without having to set the READ_THERM bit first. However, the host can always trigger an additional temperature reading the same way as for the TPS65180 and TPS65180B.

**NOTE**

At the end of each temperature acquisition, the EOC interrupt is set and an interrupt is issued. Although the interrupt is automatically cleared, the nINT pin is pulled low for a short amount of time (6 µs). To avoid seeing the EOS interrupt every 60s, TI recommends to mask the EOC interrupt by setting the EOC_EN bit of the INT_ENABLE2 register to 0.

### 10.1.16 Overtemperature Reporting

The user has the option of setting HOT and COOL (not HOT) temperature thresholds as well as controlling interrupt behavior as the NTC exceeds HOT and cools down below COOL (not-HOT) threshold.

By default, TPS6518x and TPS65181xB compare the temperature conversion result to the HOT threshold after each conversion. If the NTC temperature is above the HOT threshold, the TMST_HOT bit in the INT_STATUS1 register is set to 1 and the interrupt pin (nINT) is pulled low. HOT temperature threshold is set by the host by writing to the TMST_OS register and the HOT interrupt can be disabled by setting the HOT_EN bit of the INT_ENABLE1 register to 0.

When the device has detected that the NTC is above the HOT threshold it compares subsequent temperature acquisitions against the COOL threshold and pull the interrupt pin low when the NTC temperature drops below the COOL threshold. However, the interrupt is issued only if the host has unmasked the COOL interrupt by setting TMST_COOL_EN bit of INT_ENABLE1 register to 1. The COOL threshold is set by the host by writing to the TMST_HYST register.

To use the full functionality of the HOT/COOL interrupts the following actions are required:

1. The host sets the HOT and COOL (not HOT) thresholds by writing the TMST_OS and TMST_HYST registers.
2. (2) For TPS65180 and TPS65180B only: The host sets the READ_THERM bit of the TMST_CONFIG register to 1. This initiates the temperature acquisition.
3. TPS6518x and TPS65181xB compare the result against the TMST_OS threshold and pulls the nINT pin low if the NTC temperature exceeds the HOT threshold.
4. If the TPS6518x and TPS65181xB report a HOT condition, the host unmasks the TMST_COOL_EN bit by setting it to 1 (INT_ENABLE1 register).
5. The host initiates a new temperature conversion by setting the READ_THERM bit of the TMST_CONFIG register to 1. If the new temperature is still above the HOT threshold, a new HOT interrupt is issued. If the temperature is below HOT but above COOL threshold, no interrupt is issued (except for EOC which is issued at the end of each conversion). If the temperature is below COOL threshold, a COOL interrupt is issued.
6. After the temperature drops below the COOL threshold the host must set the TMST_COOL_EN bit in the INT_ENABLE1 register to 0 to mask additional COOL interrupts after subsequent temperature acquisitions.

### 10.1.17 Overtemperature Fault Queuing

The user can specify the number of consecutive HOT temperature reads required to issue a HOT interrupt. The user can set the FAULT_QUE[1:0] bits of the TMST_CONFIG register to specify 1, 2, 4, or 6 consecutive reads that all must be above the HOT threshold before a HOT interrupt is issued. The fault queue is reset each time the acquired temperature drops below the HOT threshold and can also be reset by the host by setting the FAULT_QUE_CLR bit 1. Only if the specified number of readings have been detected which all need to be above the HOT threshold, a HOT interrupt is issued. This function is useful to reduce noise in the temperature measurements.

### 10.1.18 TPS65181 and TPS65181B Temperature Sensor

The TPS65181 and TPS65181B automates the temperature monitoring process and is specifically designed to operate in multi-host systems where one of the I²C hosts, for eaxmple, the display controller, has limited I²C capability. Standard I²C protocol requires the following steps to read data from a register:

1. Send device and register address, R/nW bit set low (write command).
2. Send device address, R/nW set high (read command).
3. The slave responds with data from the specified register address.

Some display controllers support I²C read commands only and need to access the temperature data from the TPS65181 and TPS65181B TMST_VALUE register. To support these systems the TPS65181 and TPS65181B automatically trigger temperature acquisition every 60s (for other acquisition intervals contact the factory) and stores the result in TMST_VALUE register. With the FIX_RD_PTR bit in the FIX_RD_POINTER register set to 1 the device responds to any I²C read command with data from the TMST_VALUE register. No write command with the register address is required and address auto increment feature is disabled in this mode. Therefore reading the temperature data is reduced to two steps:

1. Send device address, R/nW set high (read command).
2. Read the data from the slave. The slave responds with data from TMST_VALUE register address.

Write functionality is not affected by the FIX_RD_PTR bit and the main controller in the system maintains full control of the PMIC. Interrupts and error flags are issued and need to be handled the same way as for the TPS65180 and TPS65180B with two exceptions:

1. The FIX_RD_PTR bit in the FIX_RD_POINTER register needs to be set to 0 before the main controller can read any register different from the TMST_VALUE register.
2. Thermal shutdown (TSD), positive boost undervoltage (VB_UV), inverting buck-boost undervoltage (VN_UV), and input undervoltage lockout (UVLO) interrupt bits do not have to be cleared before output rails can be re-enabled.

At system power-up the main processor sets up the PMIC by accessing the I²C registers and setting the control parameters as needed. When the system is set up correctly, the main controller sets the FIX_READ_POINTER bit and the display controller can start accessing the temperature information. During normal operation the main controller can write to the PMIC at any time but before it can read access registers the FIX_READ_POINTER bit must be written 0.

The temperature range and representation of the temperature data is the same between the TPS65180 and TPS65180B or the TPS65181 and TPS65181B.

### 10.1.19 I²C Bus Operation

The TPS6518x and TPS65181xB host a slave I²C interface that supports data rates up to 400 kbps and auto-increment addressing and is compliant to I²C standard 3.0.

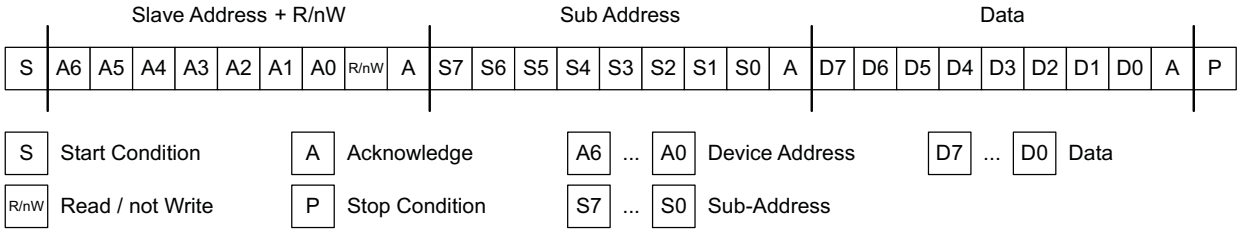



**Figure 8. Subaddress in I²C Transmission**

Start – Start condition

G(3:0) – Group ID: Address fixed at 1001.

A(2:0) – Device Address: Address fixed at 000.

R/nW – Read / not Write Select Bit

ACK – Acknowledge

S(7:0) – Subaddress: defined per register map.

D(7:0) – Data; Data to be loaded into the device.

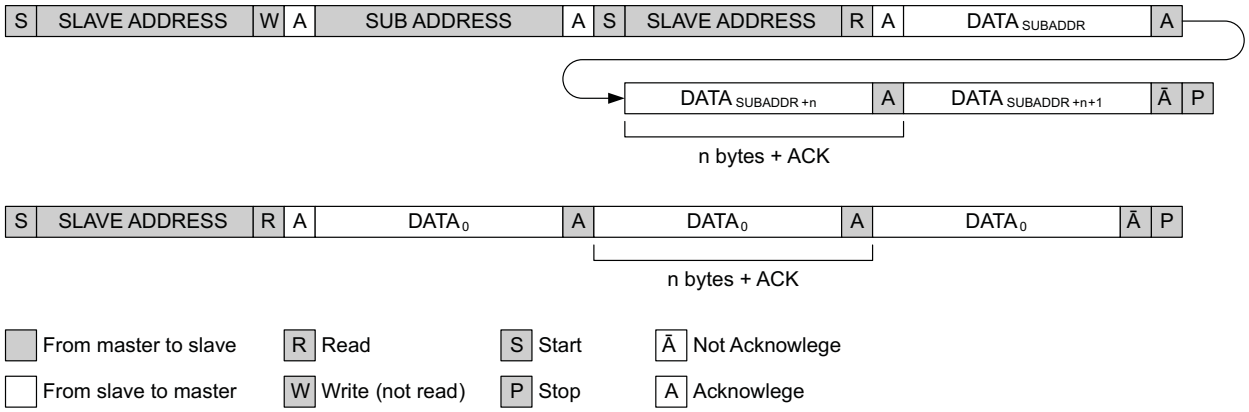
Stop – Stop condition

The I²C Bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bidirectional for data communication between the controller and the slave terminals. Each device has an open-drain output to transmit data on the serial data line. An external pullup resistor must be placed on the serial data line to pull the drain output high during data transmission.

Data transmission is initiated with a start bit from the controller as shown in Figure 10. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device receives serial data on the SDA input and check for valid address and control information. If the appropriate group and address bits are set for the device, then the device issues an acknowledge pulse and prepare the receive subaddress data. Subaddress data is decoded and responded to as per the *Register Maps* section of this document. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, sub-address and data words. The I²C interface auto-sequences through register addresses, so that multiple data words can be sent for a given I²C transmission. Reference Figure 10.

**NOTE**

Auto-increment is not supported when the FIX_RD_PTR bit is set (TPS65181/TPS65181B only).




A. Top: Standard I²C READ data transmission with address auto-increment.
Bottom: I²C READ data transmission with FIX_RD_PTR bit set for EPSON Broadsheet support.
Only address 0x00h can be read. FIX_RD_PTR bit has no impact on WRITE transaction.

**Figure 9. Standard I²C READ Data Transmission With Address Auto-Increment or With FIX_RD_PTR Bit Set for Epson Broadsheet Support**

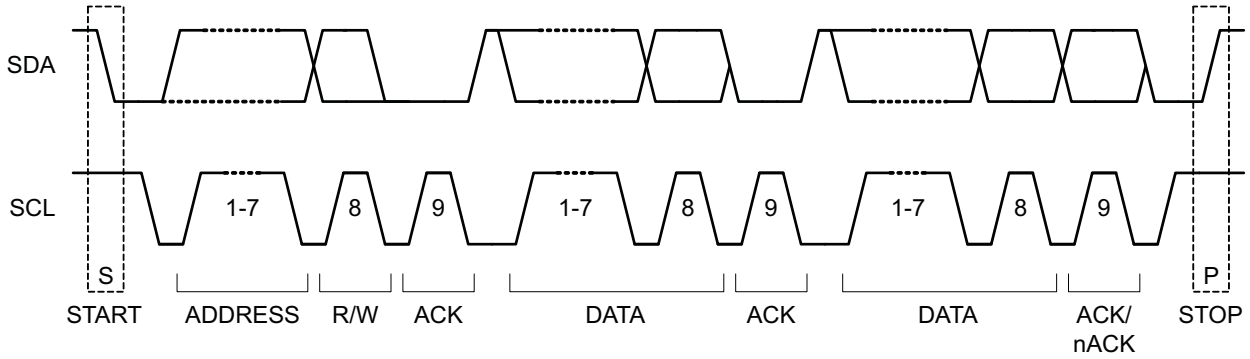



**Figure 10. I²C Start, Stop, and Acknowledge Protocol**

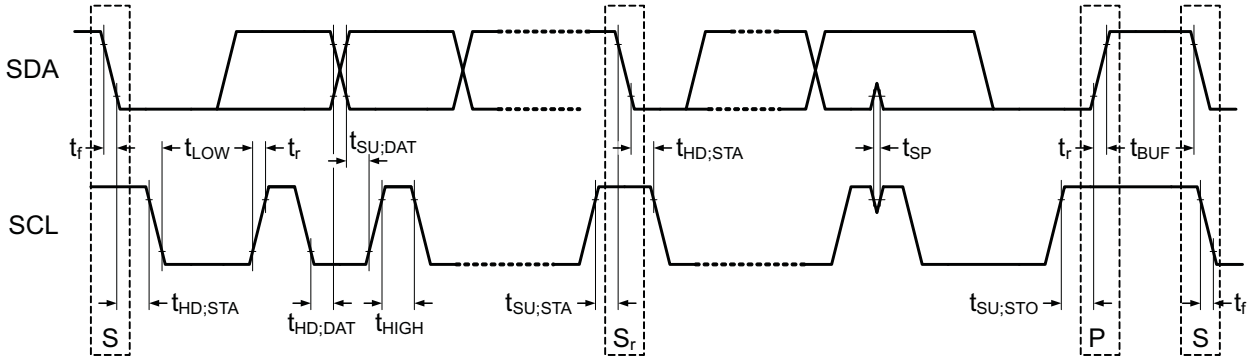



**Figure 11. I²C Data Transmission Timing**

## 10.2 Typical Application

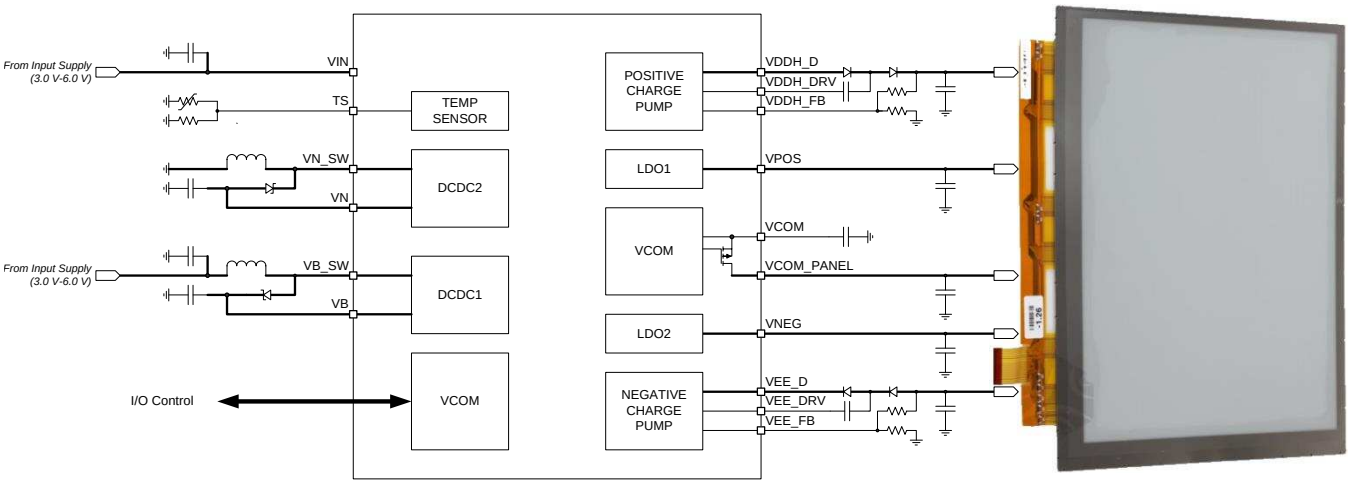



**Figure 12. Typical Application**

### 10.2.1 Design Requirements

For this design example, use the parameters listed in Table 3.

**Table 3. Design Parameters**

| | VOLTAGE | SEQUENCE (STROBE) |
|---|---|---|
| VNEG (LDO2) | –15 V | 1 |
| VEE (Charge pump 2) | –20 V | 2 |
| VPOS (LDO1) | 15 V | 3 |
| VDDH (charge pump 1) | 22 V | 4 |

### 10.2.2 Detailed Design Procedure

For the positive boost regulator (DCDC1) a 10-µF capacitor can be used as the input capacitor value; two 4.7-µF capacitor are used as output capacitors to reduce ESR along with a 2.2-µH inductor. For the inverting buck-boost regulator (DCDC2) an 10-µF capacitor can be used at the input capacitor value; A 10-µF and 4.7-µF capacitor are used as output capacitors to reduce ESR, with a 4.7-µH inductor. Capacitor ESR for all capacitors should be around 20 mΩ, and ceramic X5R material. These are the typical the values used, additional inductor and capacitor values can be used for improved functionality, but the parts should be rated the same as the recommended external components listed in Table 4.

**Table 4. Recommended External Components**

| PART NUMBER | VALUE | SIZE | MANUFACTURER |
|---|---|---|---|
| **INDUCTORS** | | | |
| LQH44PN4R7MP0 | 4.7 µH | 4.00 mm × 4.00 mm × 1.65 mm | Murata |
| VLS252012T-2R2M1R3 | 2.2 µH | 2.00 mm × 2.50 mm × 1.20 mm | TDK |
| **CAPACITORS** | | | |
| GRM21BC81E475KA12L | 4.7-µF, 25-V, X6S | 805 | Murata |
| GRM32ER71H475KA88L | 4.7-µF, 50-V, X7R | 1210 | Murata |
| All other caps | X5R or better | | |
| **DIODES** | | | |
| BAS3010 | | SOD-323 | Infineon |
| MBR130T1 | | SOD-123 | ON-Semi |
| **THERMISTOR** | | | |
| NCP18XH103F03RB | 10 kΩ | 603 | Murata |

### 10.2.3 Application Curves

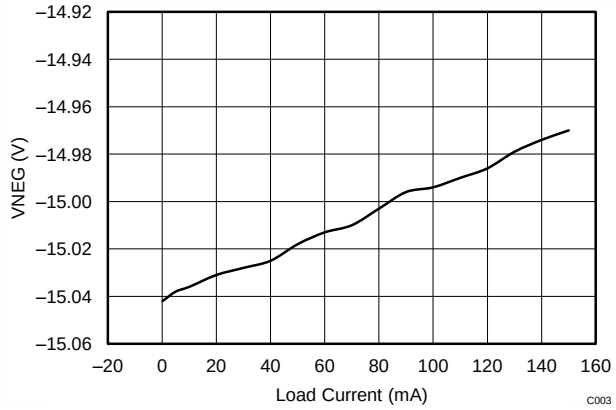



**Figure 13. Load Current vs VNEG**

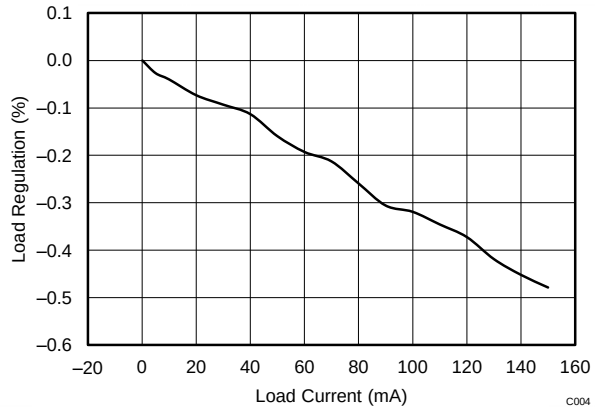



**Figure 14. Load Current vs Load Regulation**

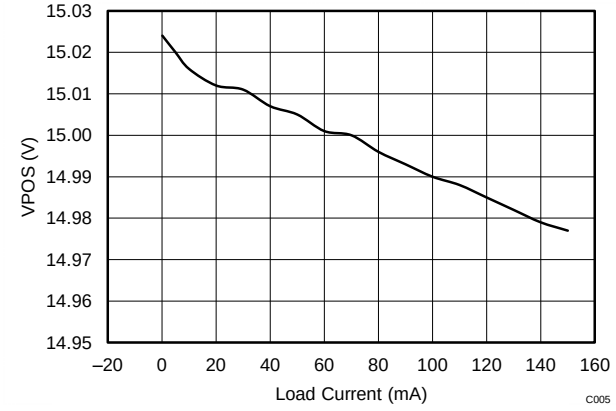



**Figure 15. Load Current vs VPOS**

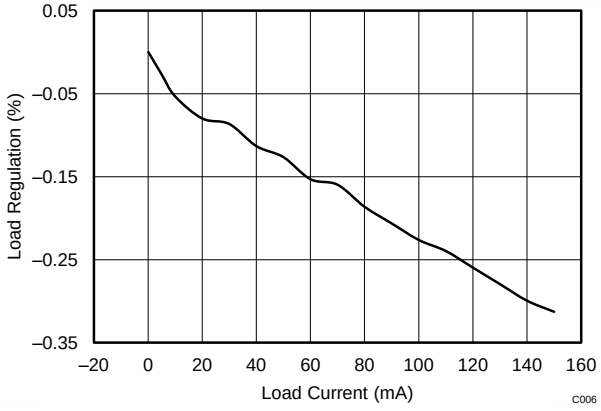



**Figure 16. Load Current vs Load Regulation**

## 11 Power Supply Recommendations

The device is designed to operate with an input voltage supply range from 3 V to 6 V. This input supply can be from a externally regulated supply. If the input supply is located more than a few inches from the TPS6518x and TPS65181xB, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 10 µF is a typical choice.

# 12 Layout

## 12.1 Layout Guidelines

The layout guidelines are listed as follows.

- PBKG die substrate must connect to VN (–16 V) with short, wide trace. Wide copper trace improves heat dissipation.
- The PowerPAD is internally connected to PBKG and must be connected to ground, but connected to VN with a short, wide copper trace.
- Inductor traces must be kept on the PCB top layer free of any vias.
- Feedback traces must be routed away from any potential noise source to avoid coupling.
- Output caps must be placed immediately at output pin.
- VIN pins must be bypassed to ground with low-ESR ceramic bypass capacitors.

## 12.2 Layout Example

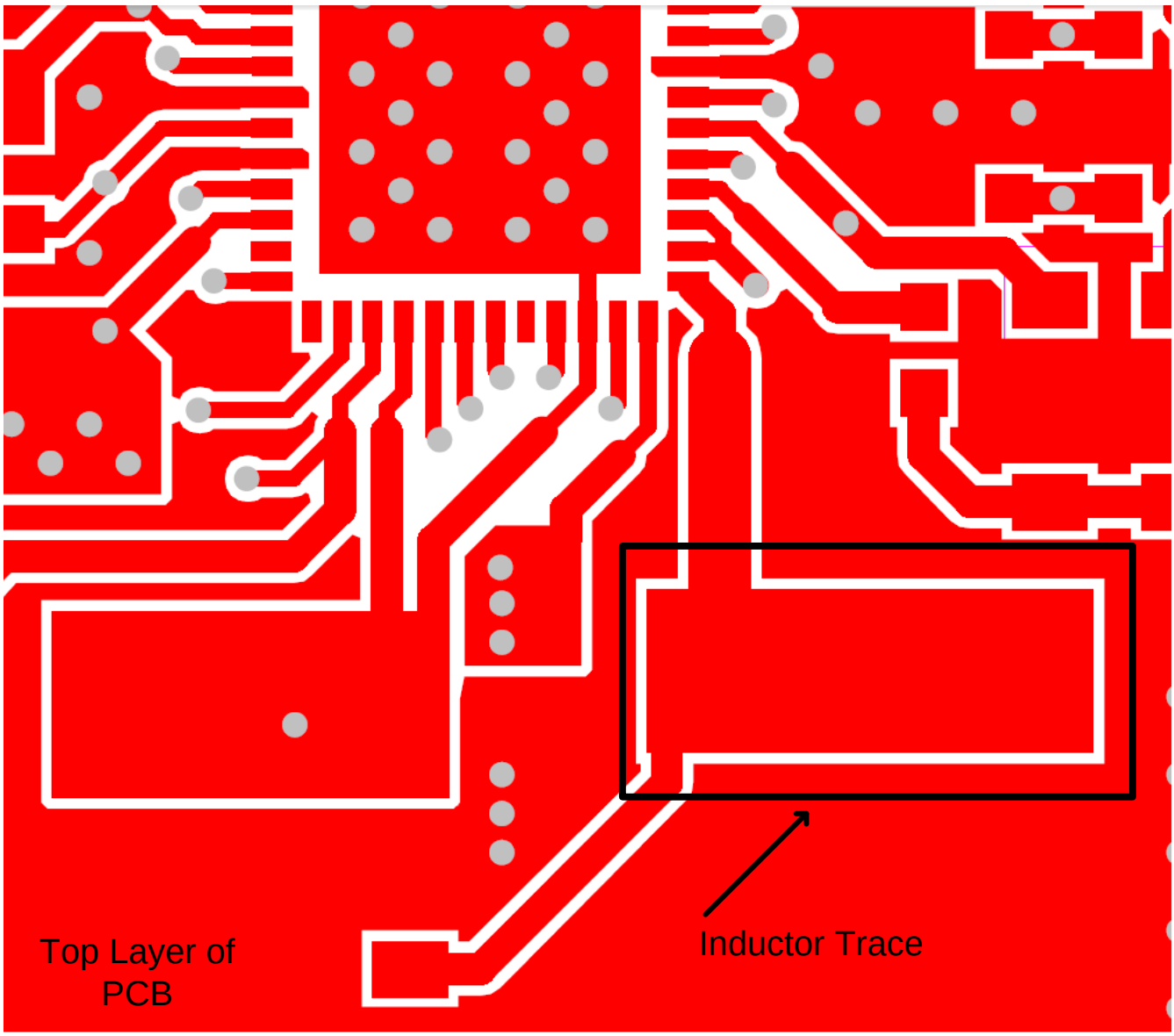



**Figure 17. Layout Top Layer**

## Layout Example (continued)

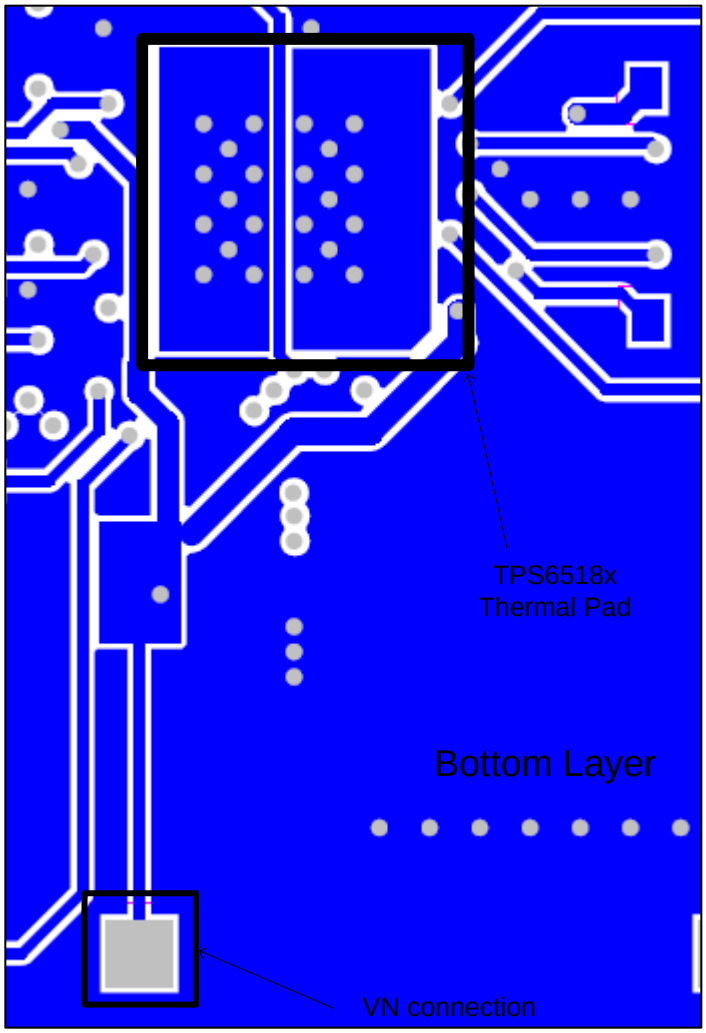



**Figure 18. Layout Bottom Layer**

# 13 Device and Documentation Support

## 13.1 Device Support

### 13.1.1 Third-Party Products Disclaimer

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## 13.2 Documentation Support

### 13.2.1 Related Documentation

For related documentation, see the following:

- *Basic Calculation of a Boost Converter's Power Stage*, SLVA372
- *Basic Calculation of a Buck Converter's Power Stage*, SLVA477

## 13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 5. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TPS65180 | Click here | Click here | Click here | Click here | Click here |
| TPS65181 | Click here | Click here | Click here | Click here | Click here |
| TPS65180B | Click here | Click here | Click here | Click here | Click here |
| TPS65181B | Click here | Click here | Click here | Click here | Click here |

## 13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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E Ink is a registered trademark of E Ink Corporation.
EPSON is a registered trademark of Seiko Epson Corporation.
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## 13.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65180BRGZR | ACTIVE | VQFN | RGZ | 48 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -10 to 85 | E INK TPS65180B | Samples |
| TPS65180BRGZT | ACTIVE | VQFN | RGZ | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -10 to 85 | E INK TPS65180B | Samples |
| TPS65181BRGZR | ACTIVE | VQFN | RGZ | 48 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -10 to 85 | E INK TPS65181B | Samples |
| TPS65181BRGZT | ACTIVE | VQFN | RGZ | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -10 to 85 | E INK TPS65181B | Samples |
| TPS65181RGZR | NRND | VQFN | RGZ | 48 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -10 to 85 | E INK TPS65181 | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

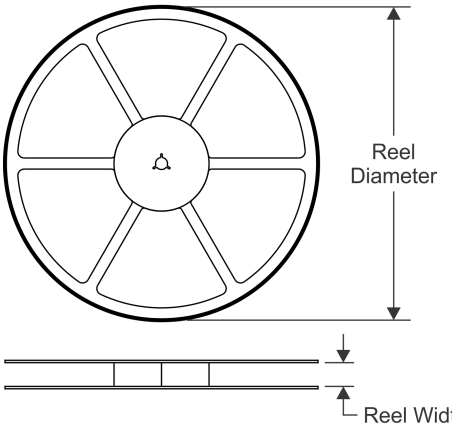
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

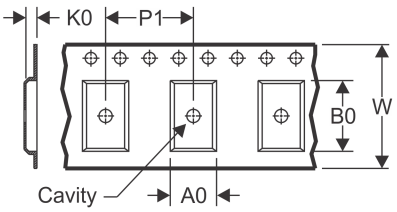
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

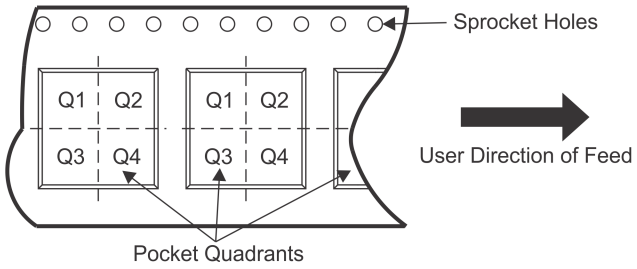



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

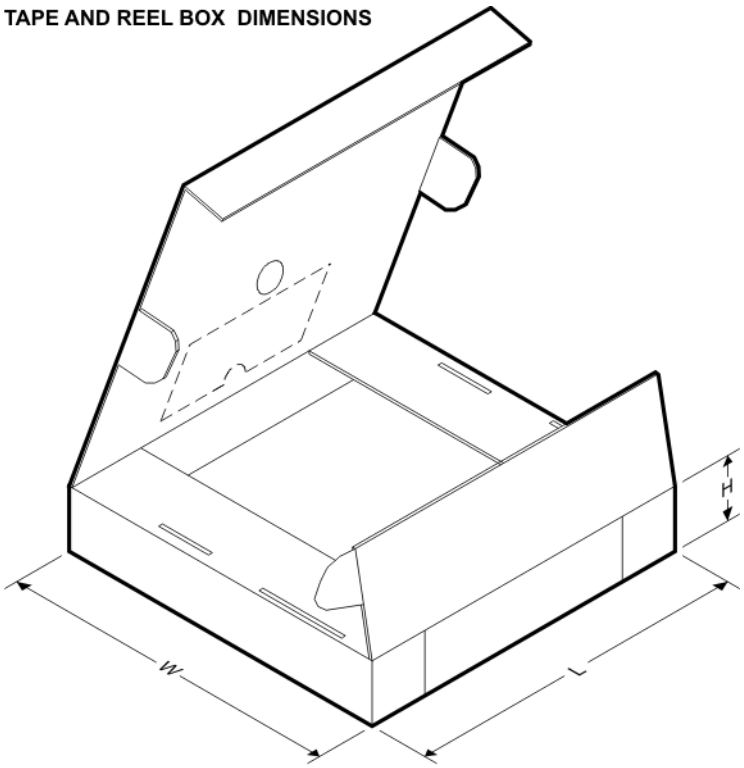
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65180BRGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65180BRGZT | VQFN | RGZ | 48 | 250 | 180.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65181BRGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65181BRGZT | VQFN | RGZ | 48 | 250 | 180.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65181RGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS65180BRGZR | VQFN | RGZ | 48 | 2500 | 367.0 | 367.0 | 38.0 |
| TPS65180BRGZT | VQFN | RGZ | 48 | 250 | 210.0 | 185.0 | 35.0 |
| TPS65181BRGZR | VQFN | RGZ | 48 | 2500 | 367.0 | 367.0 | 38.0 |
| TPS65181BRGZT | VQFN | RGZ | 48 | 250 | 210.0 | 185.0 | 35.0 |
| TPS65181RGZR | VQFN | RGZ | 48 | 2500 | 367.0 | 367.0 | 38.0 |

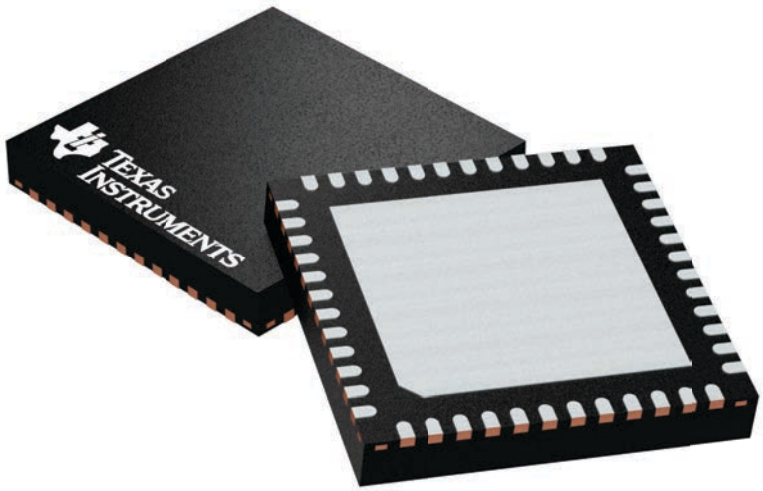
# GENERIC PACKAGE VIEW

## RGZ 48

## VQFN - 1 mm max height

**7 x 7, 0.5 mm pitch**

PLASTIC QUADFLAT PACK- NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

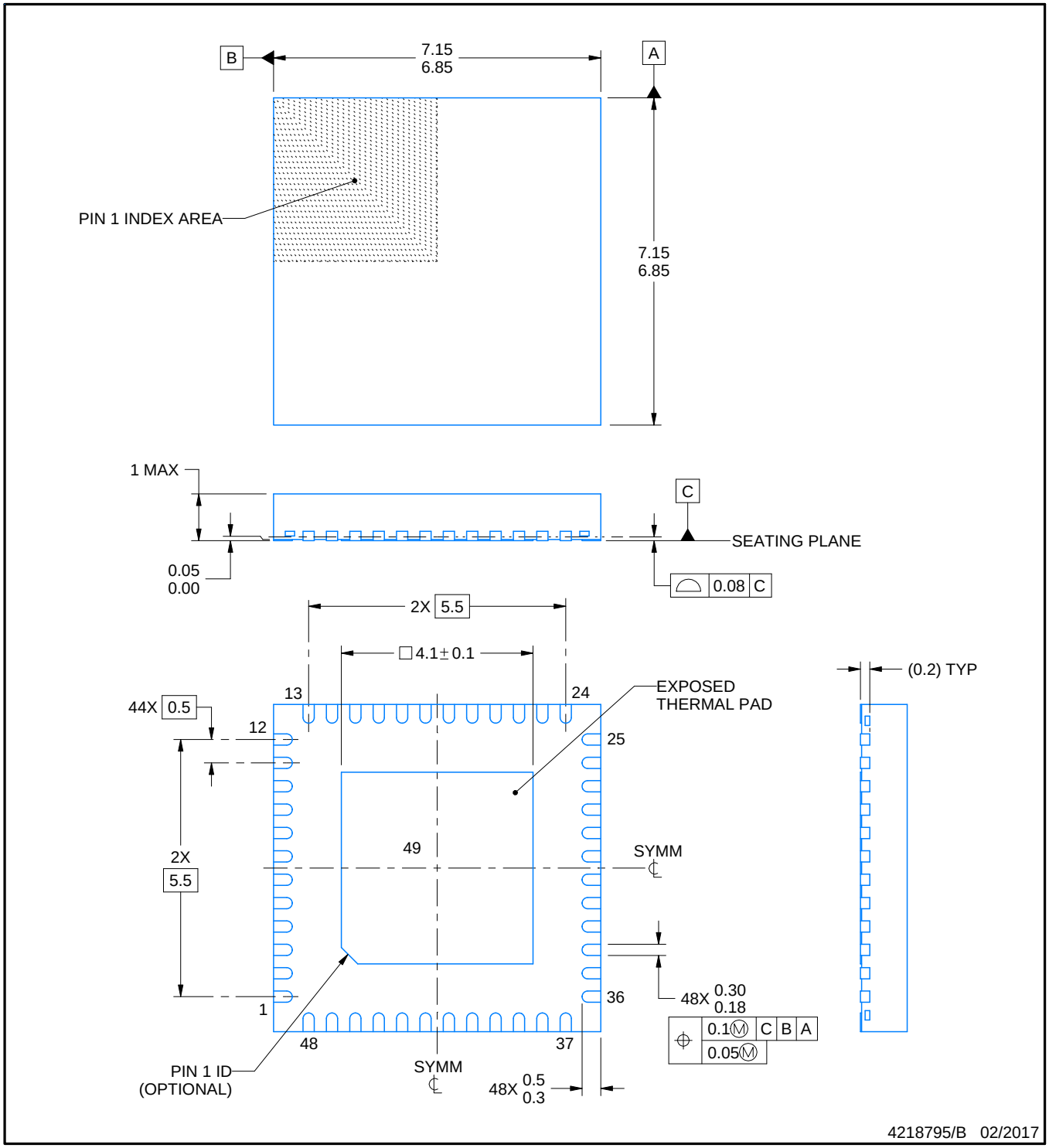
4224671/A

# RGZ0048B

# PACKAGE OUTLINE

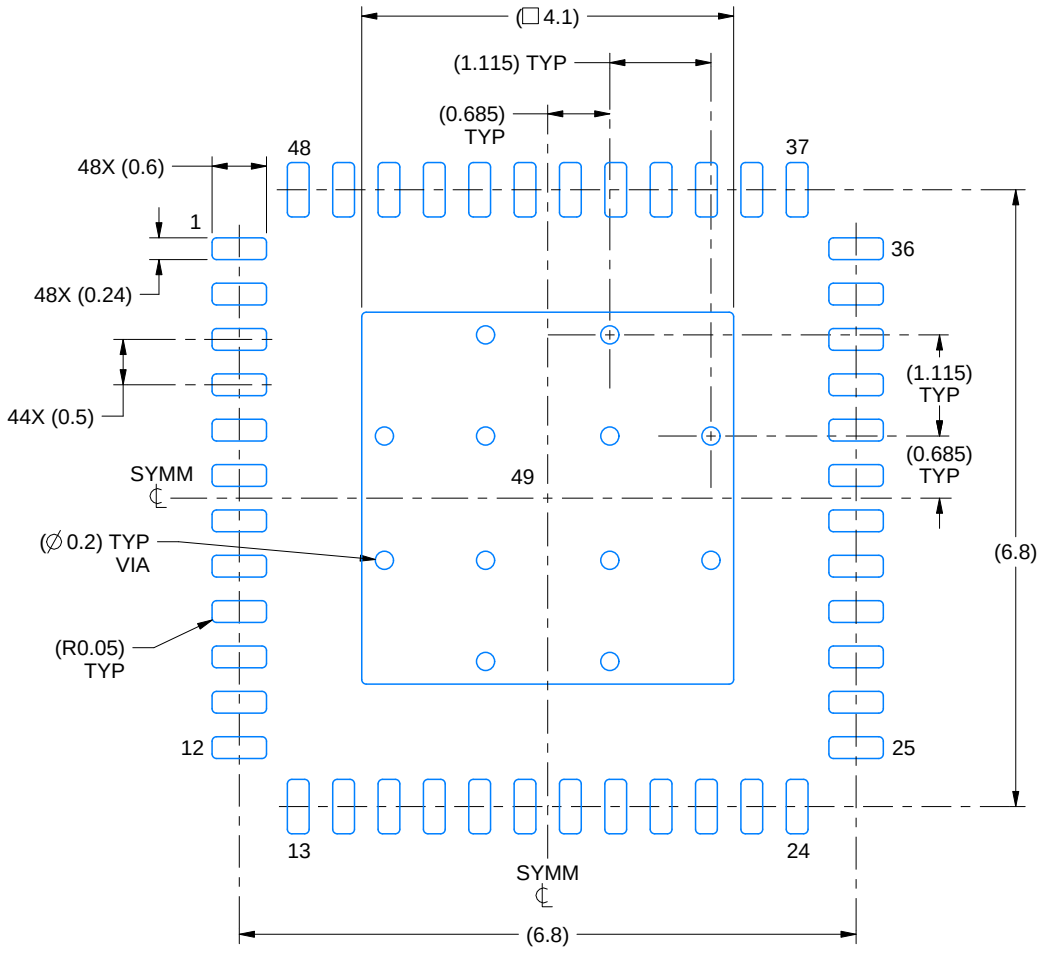
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

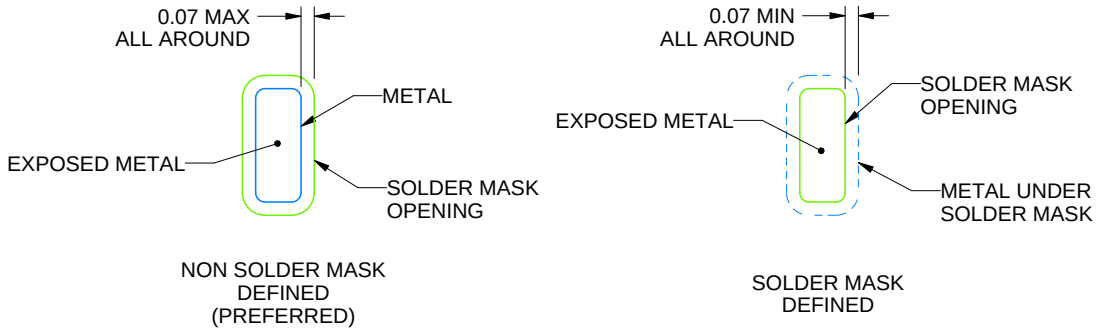



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

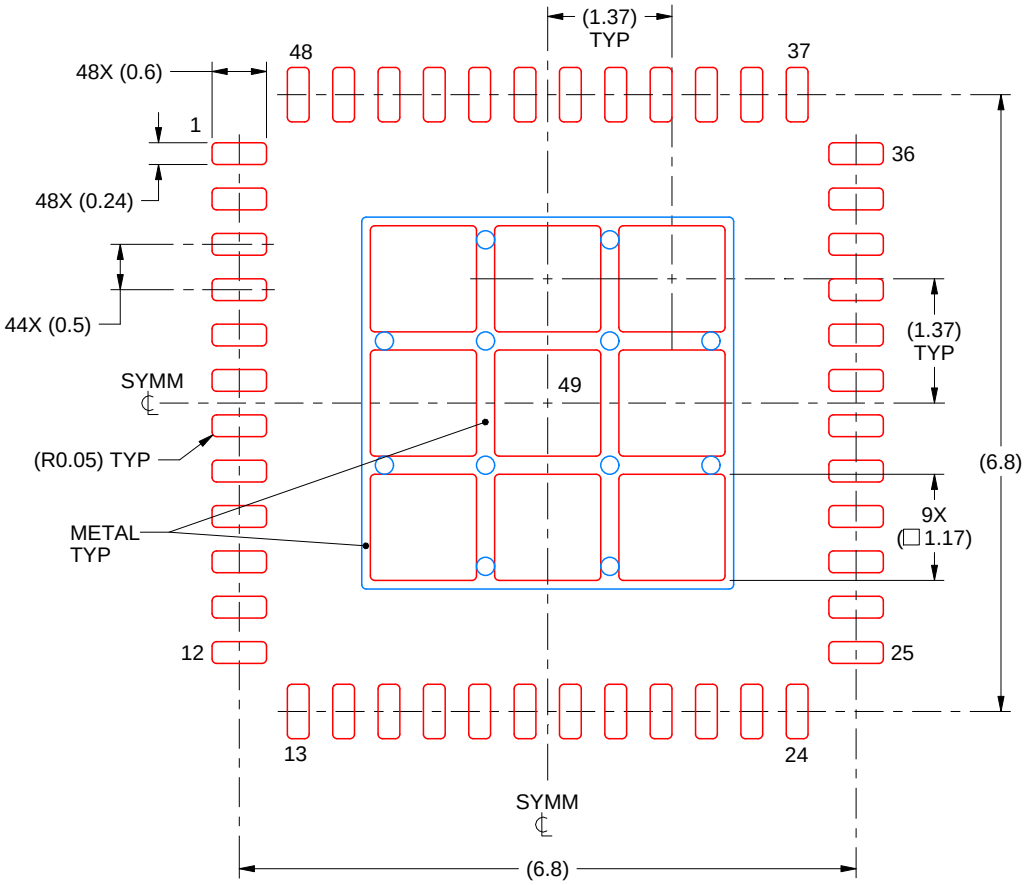



SOLDER MASK DETAILS

4218795/B 02/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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